CONFERENCE PROCEEDINGS

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1997 INTERNATIONAL CONFERENCE ON

INDIUM PHOSPHIDE AND RELATED MATERIALS

IPRM
Est. 1989

11 - 15 MAY 1997

TARA HYANNIS HOTEL AND RESORT
HYANNIS, CAPE COD, MASSACHUSETTS, USA

Errata

14 January 1998

Defense Technical Information Center
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Dear Sir/Madam:

In accordance with Grant No. N00014-97-1-0876, Performance Reports and/or Proceedings, Section A and B, Attachment Number 1, please find enclosed one (1) copy of the Conference Proceedings for the 1997 International Conference on Indium Phosphide and Related Materials. A completed "Report Documentation Page" (SF-298) is also included as instructed.

Thank you for your support of this conference.

Sincerely,

Samantha H. Padilla
IEEE/LEOS Conference Activities Manager

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REPORT DOCUMENTATION PAGE

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1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE 14-January-1998	3. REPORT TYPE AND DATES COVERED Final

4. TITLE AND SUBTITLE
Conference Proceedings for the 1997 International Conference on Indium Phosphide and Related Materials
IPRM'97

5. FUNDING NUMBERS
G
N00014-97-1-0876

6. AUTHORS
Multiple

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Institute of Electrical and Electronics Engineers, Inc.
445 Hoes Lane, P.O. Box 1331
Piscataway, NJ 08855-1331

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Office of Naval Research
Ballstron Centre Tower One
800 North Quincy Street
Arlington, VA 22217-5660

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

14. SUBJECT TERMS
InP

15. NUMBER OF PAGES
692

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL

1997 INTERNATIONAL CONFERENCE ON

INDIUM

PHOSPHIDE

AND

RELATED

MATERIALS

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HYANNIS, CAPE COD, MASSACHUSETTS, USA

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ACKNOWLEDGEMENT

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iv

TABLE OF CONTENTS

MONDAY, 12 MAY 1997

Plenary Session

MA: Power Devices

MB: Vertical Cavity Lasers and Optoelectronic Devices

Poster Session

Epitaxy

TABLE OF CONTENTS

TABLE OF CONTENTS

TUESDAY, 13 MAY 1997

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

TuF: Integrated Receivers and Detectors

WEDNESDAY, 14 MAY 1997

WA: Electronic Device Processing Technology

WB: Characterization & Control II

WC: Epitaxy: New Sources

THURSDAY, 15 MAY 1997

TABLE OF CONTENTS

Monday

12 May 1997

Plen   Plenary Session

MA   Power Devices

MB   Vertical Cavity Lasers and Optoelectronic Devices

MP   Poster Session :   Epitaxy

New Materials and Quantum Structures

Optoelectronics

Characterization and Control

Processing

Electron Devices

MC   HEMTs

MD   Joint Session: Bulk/NMQS

Monday Paper Withdrawn

MC3   High Speed Double-sided-doped InAlAs/InGaAs MODFETs with a Thin InAs Layer in the Channel

InP - Based Components for Telecom Systems in Europe   PLEN1

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Abstract

The technological potential of InP-based optoelectronics for telecom systems is now strongly focused to the needs of existing and upcoming broadband services and network architectures. The paper describes present and evolving system applications and some exemplary component developments in Europe.

I. Introduction

Until a few years ago, the major real application of optoelectronics was in long-haul transmission where fiber-optics provided drastic performance and cost advantages. Now, with the dramatic increase of Internet, on-line services and research networks, and their demand for broadband extension, together with new TV distribution services, fiber-optics spread out into the access area and require new performances in the core network.

II. Long haul transport systems

The trend and necessity for higher speed and longer link length continues. This is due to increased traffic by new interactive services and due to the shift from large numbers of smaller network nodes to small numbers of large nodes for reasons of cost reduction for operation and maintenance. The breakthrough with fiber amplifiers and the proof of longterm stability of 980nm pump lasers by IBM have solved the issue of link loss. Thus R&D work has concentrated on limiting factors of fiber dispersion induced by laser chirp. This issue was even more important because for landline systems the use of standard single mode fibres became a must.

As a basic laser structure Alcatel has chosen the BRS (buried ridge stripe) structure, Fig.1, originally developed by CNET /1/, which allows a very high reproducibility in the manufacturing process combined with high reliability.

Flexible adaption of the directly modulated 1.55μm BRS DFB lasers for various SDH system applications is achieved mainly by the design of the vertical laser structure (highly compressive strained quantum wells, grating coupling strength and waveguide layer design). The lateal structure has to be optimized for minimum parasitics.

For low cost 1550 nm STM4 systems (622Mb/s)
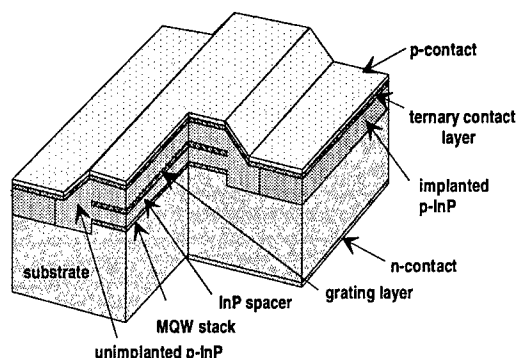
fig. 1: BRS laser structure

high temperature operation of the DFB laser with a limited current consumption is required /2/. Using an optimised QW design, low DFB coupling strength (κL product around 1.7) and AR/HR facet coating, lasers with low threshold currents (<20mA) and high quantum efficiency (>0.2W/A) at 75°C are obtained allowing system operation across 188km with only 0.2dB BER penalty. For shorter-range 1300 nm systems hp obtained sufficient laser operation up to 85°C without applying facet coating /3/. Siemens has used a loss coupled grating to increase the singlemode yield of DFB lasers from the usual 50 to 60% up to 90% at moderate emission power. This has been attained without essential reduction of CW performance /4/.

For STM16 systems (2.5Gb/s) with 200km link length, low transient and adiabatic chirp of the laser is a key requirement. With a 6QW design, a medium-range κL product of 2.5 and no facet coatings, high relaxation frequency in excess of 10GHz and suppressed transient chirp /2/ has been achieved.

For STM64 (10Gb/s) standard fiber links the strong chirp of directly modulated lasers reduces the unrepeatered length to below 10km.

Two alternatives have been shown successful for overcoming the dispersion limitation:

1) With a butt-joint integrated laser/modulator (ILM) the chirp cannot only be reduced to the minimum of the signal band width (allowing for $\approx$ 50 km), but by generation of a negative prechirp the unrepeatered length could be extended to above 100km. /5/.

2) Applying the dispersion supported transmission (DST) scheme /6/ the overall dispersion of the link is used to restore the chirped signal by FM to AM conversion. A live 10Gb/s standard fiber link of 123km between the two radio/TV studios in Stuttgart and Baden-Baden in Germany was installed in May 1995. 2.5Gb/s-type BRS lasers as described above do fulfil the bandwidth requirements for this system! They are suitable even for 20Gb/s systems across 46km, using four-level DST.

WDM systems with nx2.5Gb/s have now wide spread application specifically in USA due to their flexibility in bitrate increase and service add-on. STM16 BRS lasers are also well suited for this application as the manufacturing process allows for a precise control of the emission wavelengths, with a variation over the 2" wafer within $\pm$ 1nm.

Even larger transmission distances in WDM systems can be verified with integrated laser/modulators for which the same precision of wavelength control is achieved. Record distances with standard fiber (one channel) are above 1250km for 2.5Gb/s /7/. With regard to submarine systems transmission of 8*2.5Gb/s data across 6000km straight line dispersion shifted fiber has been shown using ILM's /8/.

In-line optical amplification by fiber amplifiers so far was largely restricted to the 1.55μm transmission window. In the 1.3μm window strained layer semiconductor based optical amplifiers (SOA) have been optimised to give similar amplification and polarisation insensitivity as fiber amplifiers. 10Gb/s 1.3μm transmission with 38km SOA repeater distance has been verified by Philips /9/.

In the 1.55μm wavelength region SOA's have been optimised by use of integrated taper structures enabling fiber-to-fiber gain in excess of 25dB and polarisation effects below 1dB. Together with their compactness and a low noise figure of 5.2dB they are well suited for optical preamplification in hybrid SOA-PIN receiver frontends /10/.

III. Access systems

In 1993-95 in the New Countries of Germany passive optical networks for TV distribution to the buildings (OPAL /11/) comprising 1550 nm EDFA's were installed requiring extremely linear lasers /12/ and detectors for the multichannel analog signal transmission. The same kind of devices is used in the Berlin field trial for interactive broadband services. The digital channels are transmitted through the hybrid fiber coax access network within the hyperband (300-450Mhz) via fiber-optic feeders with a length up to 47km /13/. With respect to 1300 nm TV distribution networks Philips has demonstrated performance of gain clamped SOA's for the analog signal amplification /14/.

For digital interactive services in Germany the regular installation of fiber to the curb with a maximum bitrate of 140Mb/s is under way, supplying up to 2.56Mb/s (later 20Mb/s) to the subscriber. BRS-laser chips as described above allow for operation up to 85°C (without Peltier cooler), and thus enabling the necessary low cost packaging concepts.

For full service deployment to both residential and business customers hybrid-fiber mm-wave systems with radio frequencies of 25GHz to 63GHz are envisaged to complement hybrid-fiber-copper networks. The optical heterodyne mixing approach with centralised mm-wave generation and transport over fiber lengths above 30km to remote radio base stations requires an optical mm-wave source which delivers two optical frequencies with high degree of phase coherency and highly efficient ultra-high speed optoelectronics converters. With double sideband modulation based on external Mach-Zehnder modulators /15/, injection locked lasers /16/, dual mode lasers /17/, and monolithically integrated dual laser transmitter /18/, mm-wave frequencies up to 60GHz have been generated. Ultra-high speed, highly efficient waveguide photodetectors with bandwidths >45GHz and power handling capability in excess of +8dBm have been realised /19/. Monolithically integrated PIN-HEMT photoreceiver on InP offers more than 27GHz bandwidth, sufficient for both mm-wave and 20Gb/s operation /20/. Field experiments have demonstrated transport of FSK modulated MPEG video and of 140Mb/s ASK signals over 46km installed standard fibre, distribution to remote antennas, and radiation to pico-radio cells at 60 GHz /15/.

IV. Future high-speed transmission and routing

Interactive broadband services will need much higher capacity in the access and core network. Research networks (e.g. JANET in UK and DFN in Germany) have dramatic bitrate increases. In European and national research programs (e.g. ACTS Highway/ Keops/Open; Photonik II in Germany) system demonstrators and test beds are being developed - including the necessary components - for high bitrates (40 to 160 Gb/s) and new capabilities such as optical add/drop, mux/demux, and photonic routing and switching to overcome existing and future limitations imposed by speed and complexity of electronics. Use of wavelength and optical time division multiplexing are approaches for flexibility and capacity increase of optical networks. In order to accomodate these advanced photonic functionalities the combination of different optical functional elements and their monolithic integration on InP is mandatory for optimum performance, flexibility and cost.

Examples of key devices mostly applying monolithic integration of different optical functional blocks are, for optical time divison multiplex systems:

- monolithic mode locked pulse lasers for generation of pulse streams up to 40Gb/s and optical clock recovery on the receiver side incorporating segments for optical amplification, wavelength selective reflection and wavelength tuning (DBR grating), and modulation /21/
- high speed electroabsorption devices /22, 23/ for data modulation
- integrated interferometers (consisting of SOA's, passive waveguides and combiners / splitters) for add/drop and mux/demux (e.g. 40 to 10Gb/s) applications /22,24,25/
- ultra fast edge receiving waveguide detectors, some of them with integrated electronic preamplification /19, 20/.

The wavelength domain helps to increase the bitrate per fiber and supports routing and switching:

- passive optical waveguide devices (silica based; with first approaches also in InP /26/) combine (mux/add) and separate (demux/drop) data streams of different wavelengths.
- switching to other wavelengths is possible in an efficient way by interferometric all optical

wavelength converters (AOWC, fig.2) specifically needed for routing through optical crossconnects and LAN's. MZI (Mach-Zehnder Interferometer) devices /27,28/ provide signal regeneration by increase of the extinction ratio, thus balancing signal deterioration occuring when active devices are cascaded (e.g. in larger crossconnects).Michelson interferometer based AWOC's /29/ have the potential of higher speed but need a narrowband optical filter at the output port.

Similar integrated waveguide structures allow for 2x2 space switches and higher order matrices /30,31/. Silica matrices with incorporated InP gates, e.g. based on gain clamped SOA's, are a promising alternative /26/. A monolithically integrated access node space switch matrix comprising 5 MZI's on a wafer size of only $4 \times 24 \text{mm}^2$ was realised by ETH Zurich, providing add/drop functionality at 3 Gb/s /32/.
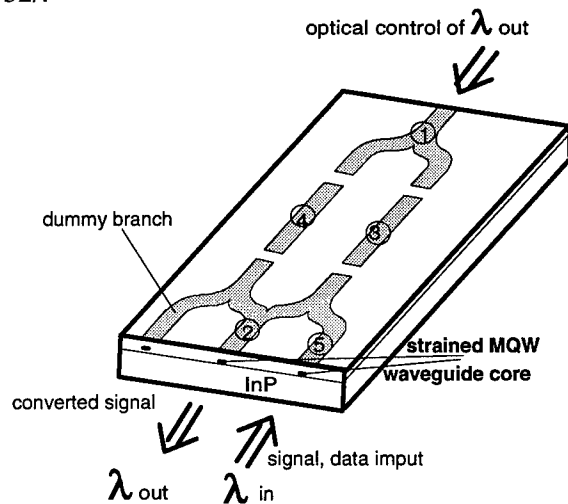
fig. 2: monolithic three-port MZI AOWC

V. Conclusion

For todays system applications, sources and receivers are largely discrete devices (lasers and detectors) adapted and optimised for the specific system needs. For future networks with higher speed and new functionalities, such as add/drop and routing, monolithic integration will become a must for performance and cost reasons. The kind of required components and their degree of integration depends on the competitiveness of optics versus other network techniques (e.g. coax and radio) in terms of total system cost and of their interoperability in hybrid access networks.

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Advances in InP-Based Optoelectronic Devices and Circuits PLEN2
for Optical Communication, Interconnection
and Signal Processing

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Abstract

Integration technology is indispensable for improving device performance, functionality and cost reduction. Recent progress of monolithic and hybrid integration in InP-based optolectronics for applications to telecommunication, interconnection and signal-processing systems is described. Towards further increases of system throughput in the 21st century, novel device principles are desired to be explored by a variety of physics in InP-based materials. An approach to develop ultrafast optoelectronic devices for Terabit/sec systems is discussed.

1. Background

In the rapidly growing information society, the volume of information is increasing exponentially at a rapid rate, 34%/year according to Japanese statistics.[1] The throughput of tele-communication systems has supported this volume mostly by optical-communication technology, which greatly relies on InP-based optoelectronic devices. Towards the multimedia era in the 21st century, the throughput of telecommunication and signal-processing systems is required to exceed 1 Tb/s by circa 2010.

2. Requirements of devices

Integration technology is very powerful for improving the functions and performance as well as reducing cost. A number of prior developments are now being transferred to system demonstrations, as can be seen in low-cost FTTH devices, wavelength-division multiplexing (WDM) devices and optical parallel interconnection links.

To achieve 1 Tb/s system throughput, however, the improvement in the performance and cost issues of existing devices seems to be insufficient. However, a generation of cost-effective, highly functional optical components by introducing new device principles is required.

Also, in order to realize system throughput well exceeding 1 Tb/s, the use of a mix of all possible dimensions, such as space, time and wavelenghth, would be most plausible. In contrast with the other two, InP-based optoelectronic devices for ultrafast operation have been slightly less developed until now. For operation above 100 Gb/s, novel devices must be designed by extensively using physics which can overcome the carrier lifetime governed speed limit in the presently existing devices.

In the following, recent progress concerning integration technology in InP-based optoelectronics is reviewed. Then, approaches to novel device principles are described by introducing various efforts for ultrafast optoelectronic devices, including the MITI-AIST project on Femtosecond Technology.[2, 3]

3. Integrated devices and circuits

An advantage of reliable optical coupling of monolithic, photonic integration has been used in modulator

integrated lasers for high bitrate sources.[4, 5] Recent demonstrations have achieved extremely long-distance transmission at a bit rate of 10 Gb/s, due to controlled blue chirp by integrating a strain-compensated quantum-well waveguide modulator.[6]

Another practically important example of integration is mode-converter integrated lasers for easy-to-couple elements for FTTH modules.[7-9] A coupling efficiency in the range of 1.2 dB - 3.5 dB has been achieved by butt coupling to a single-mode fiber by the extensive use of a selective-area MOCVD growth technique.[10] This growth technique has a wide variety of applications, due to its controllability of the thickness and quantum energy of the grown quantum well layer in the area defined by the growth mask. The same technique has been used in multiple wavelength sources[11] and is expected to be applied to various WDM devices, including receiver circuits.

On the receiver side, the waveguide structure PIN detectors and their integration in photonic circuits have been demonstrated, as important elements for low-cost modules. [12]

A new approach for improving the avalanche photodiode (APD) is found in a recent report on an InGaAs/Si wafer-bonded structure exhibiting a gain bandwidth of 315 GHz, owing to the extremely high electron ionization rate in Si.[13] This has shown the achievement of an electronically clean interface. The wafer-bonding technique is very attractive, since it widens the material choice for integration. This technique has been applied to GaAs/InP double-fused VCSELs [14] and InP lasers on a Si substrate.[15]

Circuit integration for receivers is most active in the area of optoelectronic integrated circuits (OEICs) owing to its advantage of low noise, fast speed, simplified packaging and cost reduction. Chip-processing techniques are being improved by using process-compatible structures based on PIN and MSM photodiodes combined with

HEMT[16] and HBT[17] circuits. The bandwidth is now over 20 Gb/s, and a reasonable bit error rate has been measured at 10 Gb/s.

Photonic integrated circuits (PICs) on InP substrates are useful for a variety of devices for the stability of wavelength registration. A grating wavelength router has been demonstrated.[18]

In contrast with such monolithic integration, a hybrid integration technique is even more useful for the short-term development of practical devices, and is being used in assembling a variety of modules. A high-speed receiver comprising an APD and a GaAs HBT or Si bipolar amplifier circuit is a typical example.[19] Recently, simple photonic circuits for FTTH, such as 1.3-/1.5-µm optical modules, are being actively developed by using silica planar optical circuits made on glass substrates for low-cost modules.[20]

3. Optical interconnection

Parallel optical links are expected to play an important role in interconnecting frames in supercomputers, multiple-processor machines and high-throughput transmission and switching systems.

Many collaborative developments are preceeding worldwide, and a throughput near to 10 Gb/s has been achieved by using arrays of up to twelve-channel InP-based quantum-well lasers and photodiodes combined with hybrid integration technology.[21-24] Highly uniform characteristics, represented by a threshold current variance of 1.6 mA $\pm$ 0.3 mA, have been obtained in an array of quantum-well lasers grown by MOCVD.[24, 25]

Simple and reliable packaging technology is a prerequisite for low-cost modules, and much effort is being devoted to this area, including a passive alignment between an array of devices and a fiber ribbon.[21] a twelve-channel parallel link [24] is already a commercial product, and a multiple-processor system demonstrator RWC-1 interconnected by optical parallel links

is being investigated in the Real World Computing project of MITI.[26]

Optical interconnections will be required to eventually include switching and routing functions in widening system applications. For the space-division realization of these functions, two-dimensional integrability of VCSELs and receivers is useful. A 16 x 16 OEIC receiver array with address-selection circuits has been demonstrated.[27]

4. Future InP-based opto-electronic devices and circuits

Looking to the future, ultrafast devices breaking through the present speed limit of below 100 Gb/s will become indispensable, since only the use of WDM or SDM would not be able to fulfill the ultimate system throughput beyond 1 T b/s. This leads to a strong desire for devices and circuits operable in the femtosecond time range.

Light sources operating at this speed range need an ultrashort pulse width and ultrahigh repetition. Monolithically integrated modelocked semiconductor lasers are being improved concerning their pulse width and repetition. A 3.5 ps FWHM of a transform limited pulse [28] and a repetition rate of 1.54 THz have been obtained.[29] Further improvements will necessitate a novel saturable absorber with an ultrafast recovery and a useful technique to control the group-velocity dispersion within a device structure.

At the receiver end of this high bitrate, ordinary photoreceivers cannot be used. Instead, all-optical switching devices are prerequisite for multiplexing, demultiplexing, switching and routing functions. Interferometer structures for all-optical switching devices have been studied.[30-32] Demultiplexing operation for 40 Gb/s signals has been demonstrated by monolithic Mach-Zehnder [30] and Michelson [31] switch structures, and a pulse width of 800 fs has already been reported for a GaAs-based Mach-Zehnder device.[32]

Another all-optical switch has vertical multilayer structures. They use either the ultrafast carrier lifetime in a low-temperature grown InAlAs/InGaAs-based GT interferometer[33], or ultrafast spin relaxation combined with exciton absorption saturation in an MQW etalon.[34] The demonstration of 350 fs switching[33] and the implication of 850 fs FWHM[35] have been reported for InP-based devices and materials.

The development of these ultrafast devices requires the introduction of novel physics in InP-based materials, which are expected to overcome the present carrier lifetime-governed speed limit in existing devices.

Figure 1 shows key devices required for Tb/s systems, basic techniques for device design and fabrication and physics and microstructures which are expected to enable the control of ultrafast relaxation and nonlinearity in InP-based materials.[2, 3]

5. Conclusions

Recent trends in integration technology indicate a most promising feature in both improving the performance and functions, and in reducing the number of components for low-cost modules. On the other hand, in order to support future system throughput beyond 1 Tb/s, the development of novel devices is indispensable, as is clear concerning ultrafast devices. The merging of integration technology and novel device physics based on InP-related materials will create key components for Tb/sec communication, interconnection and signal processing systems.

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Category	Basic Ultrafast Functions			
	Generation	Transmission	Control	Distribution
Key Devices	FS-Lasers	FS-Regenerator / Ultrafast detectors / Pulse shaping devices / Dispersion Control Devices	FS-optical switches / Optical delays & memories / Optical frequency converters & filters	
	Ultra-low dispersion waveguides & couplers			
Basic Techniques	Spontaneous/Stimulated emission control / Dispersion control	Mode-locking / Fourier optics	Relaxation control / Nonlinearity enhancement	
	Control of radiation field and quantum state			
Physics	Microcavity Photonic Band	Quantum Effect (Dots & Wires) Quantum Coherence	Exciton-Polariton	Intersubband Transition Spin Relaxation Tunneling

Fig.1 Diagram showing key ultrafast optoelectronic devices, techniques and physics.

10

UNIPOLAR MID-INFRARED SEMICONDUCTOR LASERS

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Introduction

The quantum cascade (QC) laser is an excellent example of how quantum engineering can be used to design new laser materials and related light sources.[1] It is based on intersubband transitions between excited states of coupled quantum wells and on resonant tunneling as the pumping mechanism. The population inversion between the states of the laser transition is designed by tailoring the electron intersubband scattering times. This design of scattering rates adds an important dimension to quantum engineering. In QC lasers, unlike all other semiconductor lasers, the wavelength is essentially determined by quantum confinement, i.e. by the layers' thickness of the active region rather than by the bandgap of the material. As such it can be tailored over a very wide range using the same heterostructure material. Since the initial report of QC lasers in 1994 (Ref. 1) QC laser wavelengths in the 4 to 11μm range using AlInAs/GaInAs heterostructures grown by MBE lattice matched to InP have been demonstrated.[2] In the original QC laser[3] the optical transition is between states centered in adjacent quantum wells, i.e. with reduced spatial overlap (diagonal or photon assisted tunneling transition). Although this design strongly reduces tunneling of electrons from the upper excited state of the laser transition into the continuum, a penalty is paid in terms of increased threshold current. This is because the width of the luminescence spectrum is broadened by the additional interface roughness scattering associated with the diagonal transition. To circumvent this problem a QC laser was designed with double quantum well active regions in which the optical transition occurs between excited states with strong spatial overlap in one well.[5]

Dramatic performance improvements have been obtained with vertical transition QC lasers in pulsed operation.[5] The threshold current density was substantially reduced (~ a factor in excess of 2), primarily as a result of the reduced luminescence width, leading to higher operating temperatures. In addition, the peak optical power is also greatly enhanced and the lasers can operate in continuous wave (cw). Cw operation of these lasers at wavelengths of 4-5μm and 7.5-8.5μm up to heat sink temperatures in excess of 100K has been achieved.[6-8] An important factor in achieving cw operation has been the use of the InP substrate as the lower waveguide cladding region rather than an AlInAs layer since the latter alloy has a ~20 times lower thermal conductivity than InP. For operation at longer wavelengths (7-8.5μm) the confinement factor of the waveguide was enhanced using the anomalous dispersion of the refractive index near the plasma frequency (plasmon enhanced waveguide).[7,9,10]

More recently the design of vertical transition QC lasers has been further improved (Fig. 1(a)), and has led to pulsed room temperature operation at $\lambda \cong 5\mu m$.[8] These are the first mid-infrared semiconductor lasers to operate at room temperature. Compared with previous lasers based on a *vertical* transition, i.e. characterized by a strong overlap of the upper- and lower-state wavefunctions of the lasing transition, this new design has an additional 0.9nm thick GaInAs quantum well coupled to the active region by a 1.5nm barrier which selectively enhances the amplitude of the wavefunction of level 3 in the 5.0nm injection barrier (see Fig. 1(a)). This maximizes the injection efficiency by increasing the overlap between the n=3 wavefunction and the ground state wavefunction g of the injector while reducing that of the latter with the n=2 and n=1 states. This minimizes injection into these states by elastic or inelastic scattering. However, in contrast to QC structures based on a diagonal transition (Fig. 1(a)), the presence of this additional 1.0nm well does not reduce the matrix element of the lasing transition (z_{32}=1.6nm). Note that the energy separation between states n=2 and n=1 is by design made equal or very close to the optical phonon energy (~35meV) to minimize the electron lifetime in the n=2 state. This design feature is characteristic of QC lasers[3-11] and greatly facilitates population inversion

The chirped superlattice of the relaxation/injection region acts as a Bragg reflector to suppress the escape of electrons from the n=3 excited state into the continuum while allowing their extraction from the lower state (n=1) into the miniband of the relaxation region. The width of this "miniband" decreases, towards the 5.0nm barrier to minimize injection into the active region of electrons thermally excited to higher states of the miniband (Fig. 1(a)). In essence the activation energy for thermionic emission

over the injection barrier is increased. This has the effect of funneling more electrons directly into the ground state g of the relaxation/injection region via resonant tunneling, thus increasing the injection efficiency at room temperature and above.

For the best high-temperature performance, the energy difference Δ between the quasi-Fermi energy in the ground state of the injector g and the lowest state (n=2) of the lasing transition (see Fig. 1(a)) was designed to be relatively large (Δ~110meV) and the sheet density of the n-type doped injection region is kept to a low value $(n_g=1.2\times10^{11}cm^{-2})$, to minimize the number of electrons thermally activated from the relaxation region into level 2 (Ref. 5). The above design changes, together with the substitution of the top AlInAs cladding region of the waveguide with an InP layer, regrown by MBE in a separate chamber (Fig. 1(b)), of much higher thermal conductivity (sample D2122), has led to the room temperature high peak power (~200mW) pulsed operation of QC lasers at λ = 5.2μm (Fig. 2).[8] In sample D2160 the top cladding layer is of AlInAs (Fig. 1(a)) which leads to lower optical powers at 300K and above (inset of Fig. 2). Continuous wave single mode operation has also been achieved up to 140K (Fig. 3).[8]

Room temperature pulsed operation at λ=8.5μm, with 15mW of peak power using a vertical transition QC laser has also been recently reported (Fig. 4).[10] For waveguiding the twenty five period AlInAs/GaInAs active region was cladded by a top AlInAs layer and by the InP substrate. QC lasers with wavelengths as long as 11μm have also been demonstrated.[11] Fig. 5 summarizes the experimental results in terms of QC laser wavelength and operating temperature (heat sink temperature) for cw and pulsed operation. It is important to note that this broad wavelength range was covered using the same heterostructure material. QC lasers are a very promising substitute to lead-salt-based lasers[12] in the mid-infrared because the materials used (III-V semiconductors for high speed electronics and near infrared optoelectronics) are much more reliable and easier to process than lead salts. In addition, the operating temperature, power levels and single mode behavior are superior compared to lead salt lasers. The overall performance of QC lasers makes them excellent candidates for military applications such as countermeasures, infrared scene projection and sensors for the detection of toxic gases, as well as commercial ones such as environmental sensing and pollution monitoring in the 3-5μm and 8 to 13μm atmospheric windows.

a)

b)

InGaAs	n = 1x10^20	10
graded	n = 7x10^18	30
	n = 7x10^18	1200
AlInAs	3x10^17	700
	2x10^17	600
graded	n = 2x10^17	30
InGaAs	n = 1x10^17	300
Active region (25x)		1200
InGaAs	n = 1x10^17	300
graded	n = 2x10^17	25
InP	n = 1x10^18	

c)

	n = 7x10^18	1300
InP	2x10^17	1500
	5x10^17	20
graded	n = 2x10^17	30
InGaAs	n = 1x10^17	400
Active region (25x)		1200
InGaAs	n = 1x10^17	400
graded	n = 2x10^17	25
InP	n = 2x10^17	
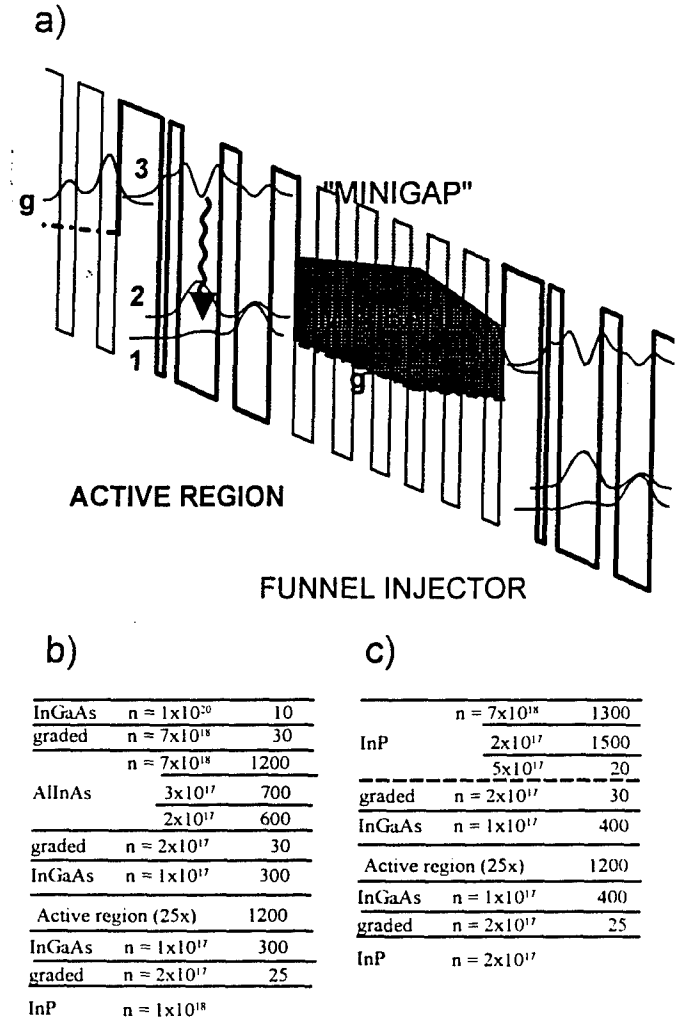
Fig. 1. (a) Calculated conduction band diagram of one period (active region plus injector) of a quantum cascade laser with vertical transition designed for room temperature operation. The laser comprises 25 periods. The applied electric field is 7.6x104V/cm. The layer sequence of one period of the $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ structure, in nanometers, left to right and starting from the injection barrier is (5.0/0.9), (1.5/4.7), (2.2/4.0), (3.0/2.3), (2.3/2.2), (2.2.2.0), (2.0/2.0), (2.3/1.9), (2.8/1.9). (b) Layer structure of the waveguide of sample D-2160. The dashed line indicates the interface where the growth was interrupted. (c) Layer structure of the waveguide of sample D-2122.
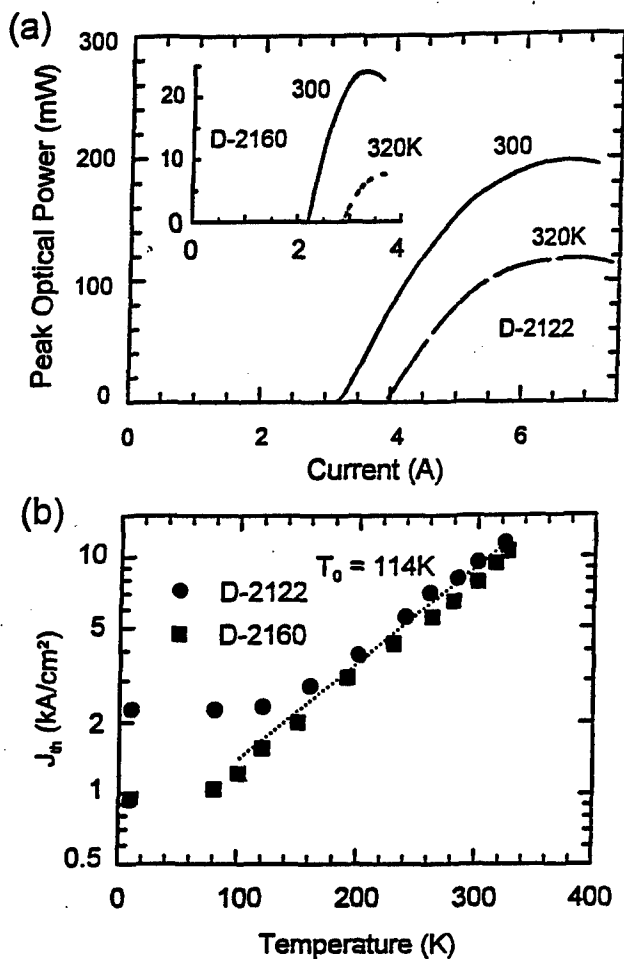
Fig. 2. Pulsed performance of QC lasers with vertical transition and funnel injector emitting at 5.2μm. (a) Collected pulsed optical power from a single facet versus injection current for heat sink temperatures of T=300K and T=320K and for the InP cladded sample D-2122 (dimensions 14μm × 2.9mm). The collection efficiency is estimated to be ≅ 70%. Inset: same characteristics for sample D-2160 (9μm×3mm). (b) Threshold current density in pulsed operation for both samples as a function of temperature. The dotted line indicates the range over which the temperature dependence is exponential exp(T/T₀).
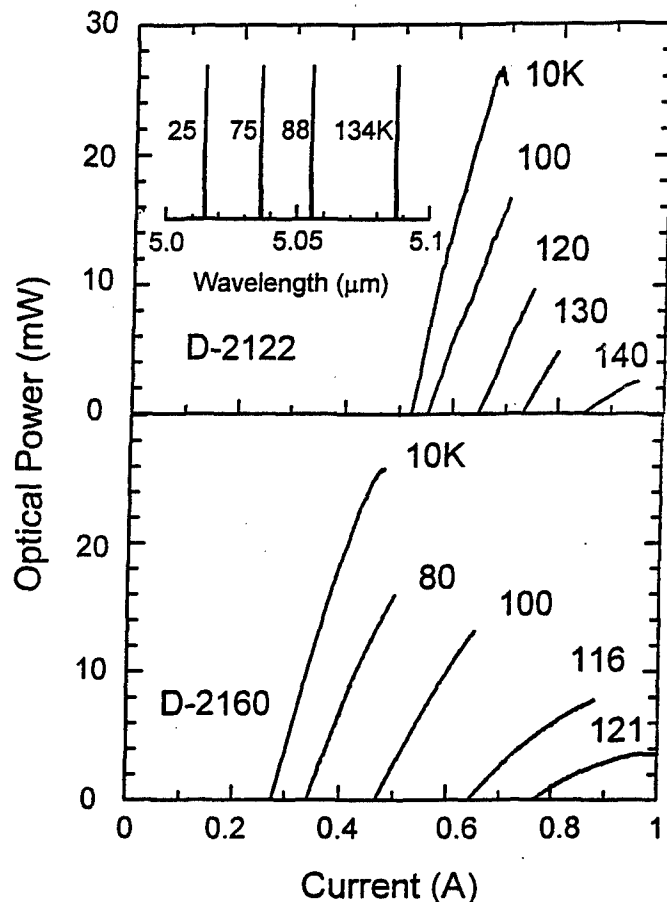
Fig. 3. Collected continuous optical output power from single facet of the 5.2μm QC laser versus injection current for various heat sink temperatures: (a) Sample D-2122 (7μm×2.9mm).(b) Sample D-2160 (9μm×3mm). Single mode high resolution spectra are shown in the inset. The collection efficiency of the apparatus is η≅0.5.
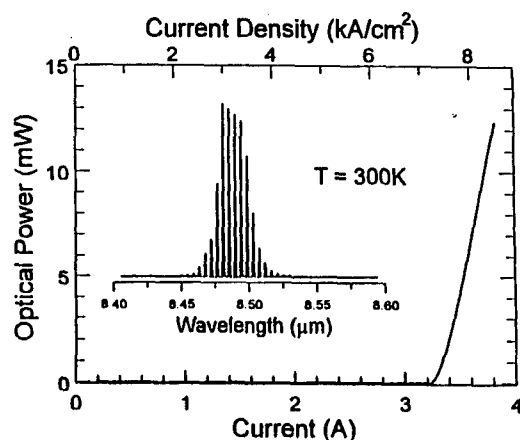
Fig. 4. Pulsed characteristics and multimode spectrum at room temperature of quantum cascade laser emitting at λ=8.5μm.

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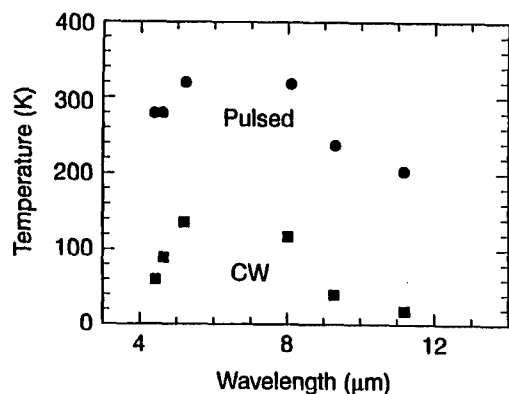
Fig. 5. Maximum operating temperatures in pulsed mode (circles) and cw mode (squares) at different QC laser wavelengths.

14

Bandgap Engineered InP-Based Power Double Heterojunction Bipolar Transistors

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The bandgap engineering of InP-based DHBTs for power applications is demonstratred using chirped superlattices grown by GSMBE. The transport properties of electrons depend on the design parameters of the CSL and strongly affect the performance of the device. Excellent performance has been achieved. In the present paper, we describe device structure optimization, fabrication process and power performance of InP-based DHBTs at S, X, and K bands.

I. Introduction

Hetrojunction bipolar transistors (HBT) are very attractive for microwave power applications [1, 2]. HBTs are advantageous due to the high speed and large power density achievable with these devices [3]. In recent years, much effort has been devoted to the design and fabrication of high-performance microwave amplifiers, which are required to have both high output power and high power-added-efficiency (PAE), using GaAs-based single heterojunction bipolar transistors (SHBT). Today GaAs/AlGaAs HBTs play an important role in many mobile communications system. From a materials perspective, InP and the lattice-matched alloys $Al_{0.48}In_{0.57}As$ and $Ga_{0.47}In_{0.53}As$ form an even more attractive system for high-performance devices. In comparison to GaAs, InP has higher peak and saturated electron velocities, higher breakdown field, and higher thermal conductivity. The speed advantage of InP-based HBTs have been well demonstrated; they have the highest f_T and f_{max} for bipolar transitors [4-6] today. However, higher speed is usually obtained at the expense of the base-collector (BC) breakdown voltage. Since the capability to withstand high voltage and current, in addition to speed, is critical for microwave applications which demand high output power density, the narrow bandgap InGaAs alloy is not a favorable material for the collector. Double heterojunction bipolar transistors (DHBT) with an InP collector and lattice-matched GaInAs base offer a much more attractive choice for power devices. However, a common problem with DHBTs is the presence of the conduction band edge discontinuity ΔE_c at the base-collector heterointerface which can result in a current-blocking potential barrier. Consequently, DHBTs whose base-collector junction is not properly designed can exhibit larger turn-on and saturation voltages and gain compression at lower current densities than SHBTs with a similar structure. In our current work, we report a novel bandgap-engineered DHBT that (i) eliminates the current-blocking potential barrier between the base and the collector, and (ii) injects hot electrons into the collector at room temperature. Power performance of InP-based DHBTs at S-, X-, and K- bands will be presented.

II. Device Design

Our principal concern in the design of the InP-based DHBT is the ΔE_c, about 250 meV at room temperature, between the base and the collector, which could cause a significant degradation in the performance of the device. It is well known that in principle one can tailor either E_c or E_v to any arbitrary profile by an appropriate combination of both compositional grading and doping [7]. For instance, the band offsets can be eliminated by a parabolic compositional grading profile with the corresponding uniform doping profile in the interfacial region as employed by Schubert et al. [8]. We proposed an easier scheme to remove the discontinuity which involves a *linear* bandgap variation (which requires essentially a linear variation in composition) for the interfacial region and two *delta doping* layers of the same concentration at the ends of the region. The ionized impurities create a dipole which cancels the band offset [9]. The areal doping concentration σ, the conduction band offset ΔE_c, and the thickness L of the linearly graded region are related via the following condition,

$$\sigma = \frac{\varepsilon_s \Delta E_c}{q^2 L}$$

For the base-collector junction of the DHBT, the linear-delta region is formed by grading from the smaller bangap base to the larger bandgap collector. The donor delta doping sheet is at the collector end, and the acceptor sheet at the base end. Clearly, the donor delta doping sheet can also be replaced by a thin, heavily doped layer such that the integrated impurity concentration per unit area is maintained, and the heavily doped base automatically provides the acceptor sheet for the dipole. The linear-delta design therefore allows more tolerance in the growth of the DHBT structure. Recently, this scheme has also been employed by other workers [10, 11].

There is a constraint on the length L of the transition layer and the breakdown voltage of the base-collector junction. As indicated in the above equations, a shorter grade requires a higher electrostatic field (supported by the doping dipole). For *electrons* this field is canceled by the quasi-electric field in the conduction band. In the valence band, the electrostatic field and the quasi-electric field (due to the spatial dependence of the valence band edge) acting on *holes* are in the same direction. Electrons in the conduction band feel only the electrostatic field created by ionized impurities as in a homojunction whereas

holes in the valence band experience the sum of the electrostatic field and quasi-electric field arising from the grading of the bandgap. The force felt by the holes in the transition layer is greater than the force felt by the electrons at the same position by an amount equal to ΔE_g /L, where ΔE_g is the bandgap difference. Therefore, thinner transition layer results in higher impact ionization initiated by holes.

For InP-based DHBTs, the graded interfacial region is composed of an AlInAs/GaInAs chirped superlattice (CSL) for reasons that will be discussed in the next section. The interfacial region is divided into a number of periods of equal thickness. Each period consists of a GaInAs layer and an AlInAs bandgap layer. The relative thicknesses of these layers were chosen so that the composition averaged over the period corresponds to that of an alloy with the desired value for the energy gap. The introduction of the CSL adds additional considerations that need to be addressed in the design of the device.

III. Materials Growth and Device Fabrication

The epitaxial device structure was grown on 3" semi-insulating InP substrates in a Varian Mod Gen II gas-source MBE system. Arsine and phosphine were used for group V sources. Elemental solid sources were used for group-III elements. Conventional Si and Be sources were used for n- and p- type doping respectively. Typical operating pressure was 2×10^5 Torr during growth for a growth rate of 1 μm/hr.

The growth conditions were kept nominally identical for all structures reported here. Following the oxide desorption at 540°C, the n+-InGaAs subcollector was grown. The InP collector was 1.0 μm thick and doped at 1.4×10^{16} cm^{-3} for X- and S-band devices and 0.5 μm thick and doped at 2.5×10^{16} cm^{-3} for K-band devices. The substrate temperature during the growth of the InP collector was approximately 450°C. This growth temperature was determined to be a good compromise between surface morphology and compositional purity. The level of unintentional As incorporation in our GSMBE system at this growth temperature is less than 0.5% which results in a strain below 10^{-4}.

Fig. 1: Common-emitter characteristics of two devices with period thicknesses of 1.5 and 2.5 nm. The device with thicker period exhibited oscillatory behaviors.

Electron transport from the base to the collector depends sensitively on the thickness of the CSL period. A thinner period results in wider minibands which reduces the transit time through the CSL. Thicker periods correspond to narrower minibands and can result in an oscillatory IV characteristic due to resonant transport between the minibands which is not desirable for power devices (Fig. 1). However, it is easier to grow CSL with a thicker periods. We have empirically determined the optimal period thickness to be 1.5 nm [12].

Fig. 2: TEM images of (a) InGaAs/InP CSL and (b) AlInAs/InGaAs CSL.

A CSL and a doping dipole were grown between the InGaAs base and the InP collector. We investigated both InP/InGaAs and AlInAs/InGaAs CSLs. From a material growth

perspective, the InP/InGaAs CSL is much more difficult to grow. We observed significant interfacial strain which built up as the number of InP/InGaAs interfaces increased. The strain was caused by the intermixing of group-V elements at the interfaces, especially of As in InP. Such interfacial strain would result in less reliable devices (Fig. 2a). Using an all-arsenide AlInAs/InGaAs CSL, we could avoid the interfacial mixing of As and P and the resultant strain. As shown in the TEM micrographs of Fig. 2, the AlInAs/InGaAs CSL, in contrast to the InP/InGaAs CSL, has sharp interfaces with no observable strain. An additional benefit of using the AlInAs/InGaAs CSL is that it can be conveniently designed to form a hot electron launcher at the base-collector junction. This type of CSL has been adopted for all of our baseline power DHBTs.

The base consisted of a 60 nm InGaAs layer doped at $p = 3 \times 10^{19}$ cm^{-3} and two 5 nm InGaAs spacer layers doped at $p = 2 \times 10^{18}$ cm^{-3}. The spacer layers were intended to accommodate any out diffusion of Be. The entire base was grown at 450°C. We found that this growth temperature is sufficiently high to result in DC current gain exceeding 40 without appreciable Be diffusion as analyzed by SIMS. We used AlInAs for the emitter. The structure of the emitter followed Hughes standard design previously reported [13].

The InP-based DHBTs were fabricated using a triple mesa process. The emitter metal contact, Ti/Pt/Au, also served as the mask for the base-emitter mesa definition by wet chemical etch. The Ti/Pt/Au base contact was self-aligned to the emitter. Collector contact was formed by alloyed AuGe/Ni/Au [14]. Polyimide was used for device planarization and electrical isolation. The power cell consisted of multiple 2×30 µm^2 which were connected together by a ~3.5 µm thick Au air-bridge. Besides providing a low resistance connection for the emitter fingers, the air-bridge also served as a thermal shunt. It is well known that bipolar power transistors (both Si BJT and HBT) with multiple fingers are prone to thermal runaway causing the so-called current collapse. Using a Au air-bridge, we were able to reduce the temperature difference among the emitter fingers of the power cell to improve the thermal stability of the cell.

IV. Electrical Characteristics

As discussed earlier, the behaviors of the device depend sensitively on the parameters of the CSL. Fig. 3 shows the common-emitter characteristics of two devices with different CSL period thicknesses, but otherwise identical. The device with a 2.5 nm period exhibited an oscillatory behavior whereas the one with a 1.5 nm period showed a smooth characteristic indistinguishable from that of a SHBT. The turn-on characteristic of our DHBTs is excellent with an offset voltage of less than 50 meV, which is even better than that of SHBTs. The ideality factors of

the base and collector currents determined from the Gummel plots are 1.1 and 1.0 respectively for these devices. CSL DHBTs designed for S- and X-bands have base-collector breakdown voltages greater than 35 V, and V_{CBO} of K-band devices was 15 V.
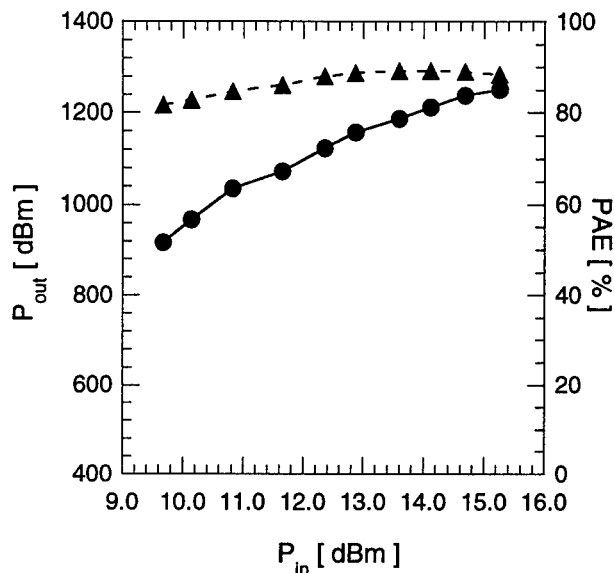
Fig. 3: Power performance of a InP-based DHBT at 2 GHz.

The small-signal RF characteristics of the device was determined by on-wafer S-parameter measurements. For single-finger (2×30 µm^2) with a 1.0 µm InP collector, designed for applications at S- and X-bands, we obtained a peak f_τ of 70 GHz at $V_{CE} = 1.5$ V and $J_c = 5.4 \times 10^4$ A/cm^2. The peak f_{max} of these devices was 87 GHz at $V_{CE} = 2.0$ V and J_c 5.0×10^4 A/cm^2. All K-band devices exhibited peak fT and fmax above 100 GHz at collector current densities of approximately 7.5×10^4 A/cm^2.

Microwave power performance was characterized using multiple-finger power cells which were fabricated on the same wafers. Each power cell consisted of 10 or 12 (2×30 µm^2) emitter fingers. Both DC and RF characteristics of these power cells are very uniform across the wafer. On-wafer active load-pull measurement was performed at 2 and 9 GHz for devices with 1.0 µm collector and at 18 GHz for devices with 0.5 µm collector.

At 2 GHz, we biased the device in class C with -1.0 V base voltage. The high breakdown voltage of the CSL DHBT enabled it to operate at 19 V collector voltage. Figure 3 shows the output power and PAE as a function of input drive. The peak PAE was 90% at 3 dB compression. The corresponding output power was 1.2 W with a power density of 2.0 mW/µm^2. The associated gain was 16.7 dB. In contrast to GaInP/GaAs DHBT [15], both output power and PAE of the InP-based CSL DHBT increased with increasing collector bias voltage. As the collector voltage was raised from 12 V to 19 V, the peak PAE increased from 85% to 90% and the output power of the device at the peak PAE increased from 0.5 W to 1.2 W. The same

17

behavior was observed at 9 and 18 GHz. However, the collector bias voltage was thermally limited at higher frequencies because of lower efficiencies and more heat dissipated.
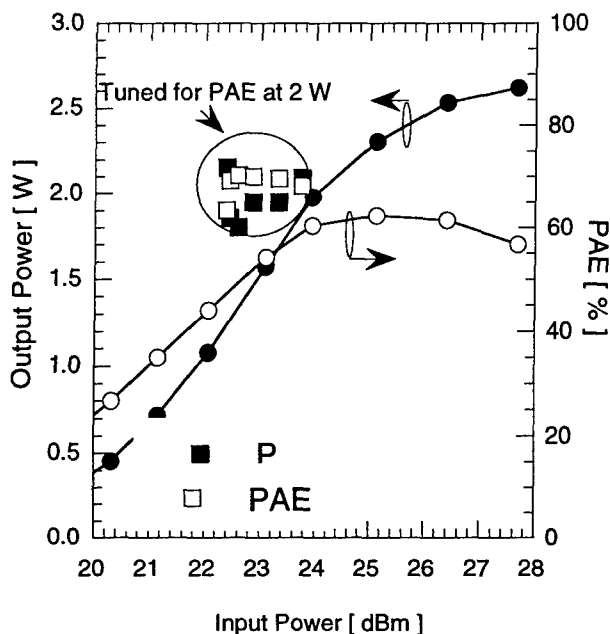
Fig. 4: On-wafer load-pull measurement at 9 GHz.
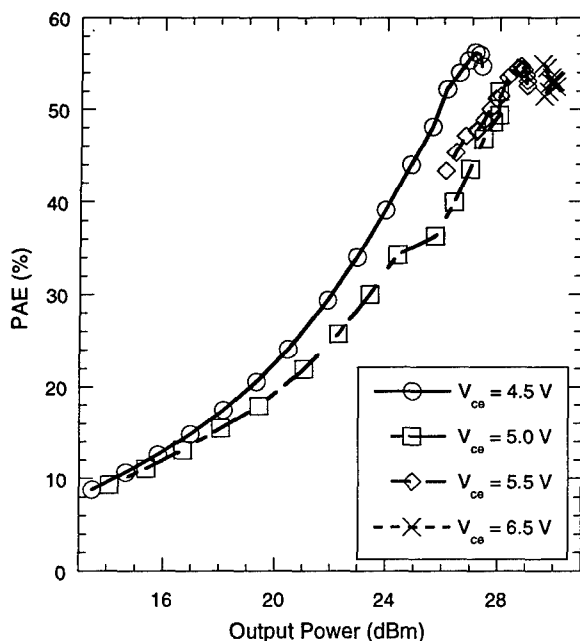
Fig. 5: PAE vs. P_{out} of an 8-finger device at 18 GHz

Figure 4 shows the output power and PAE of a 12-finger power cell biased for class B operation which was measured on-wafer with unthinned substrate. When the load was tuned for high PAE at 2 W output power, a peak PAE of 71% was achieved, which already surpassed

the recently reported performance of GaAs-based HBT power cells [16-19]. Figure 5 shows the PAE versus output power for a 8-finger power cell at 18 GHz. A combination of 52% PAE and 1.0 W of output power was obtained at 6.5 V collector bias. The device suffered from current collapse due to thermal runaway at higher collector voltages. We expect to be able to enhance the power performance of the device significantly using ballast resistors and operating the device at higher voltages.

V. Conclusions

We have demonstrated that using bandgap engineering we can completely eliminate the current-blocking barrier arising from the conduction band offset of InGaAs/InP DHBT while retaining the advantages of the InGaAs base and InP collector. Digital grading, particularly the all-arsenide InGaAs/AlInAs CSL, represents a good compromise between performance and manufacturability. Excellent power performance at S-, X-, and K-bands clearly indicate the potential of InP-based DHBTs for microwave power applications.

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0.9W/mm, 76% P.A.E. (7GHz) GaInAs/InP Composite Channel HEMTS

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Abstract

The power performance of $Ga_{0.47}In_{0.53}As$/InP composite channel HEMTs at 7GHz is presented. Devices with gate width of 300µm exhibit 0.9W/mm and 76% power-added-efficiency (P.A.E.) at 7GHz with two-terminal breakdown voltage of 13.3V.

Introduction

The advantage of the GaInAs/InP composite channel power HEMTs over GaInAs single channel power HEMTs lies in the ability to achieve high power densities (utilizing the high peak and saturation velocities in GaInAs and InP, respectively[1]) while achieving high breakdown voltages (due to the energy quantization[2] and high breakdown field in GaInAs and InP, respectively). This paper reports a record combination of power output density (0.9W/mm) and power added efficiency (76%) at 7GHz together with high two-terminal breakdown voltage (-13.3V).

Device Structure

The device structure studied is the double-doped GaInAs/InP composite
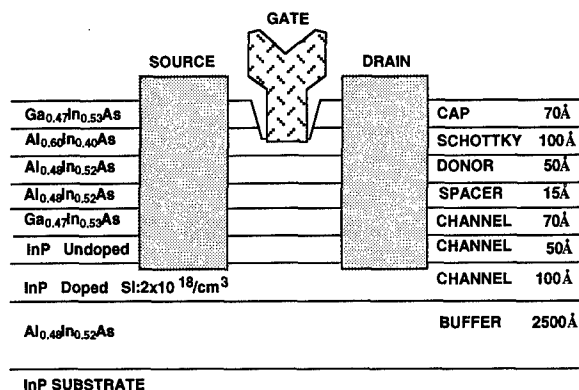
Figure 1. Layer structure of the GaInAs/InP composite channel power HEMT.

channel HEMT with a 70 Å GaInAs channel and partially-doped sub-channel as shown in Figure 1. The hall charge and mobility was measured to be 8600 cm^2/Vs and 3.3×10^{12} cm^{-2}, respectively.

The layers were grown using a gas source Varian Gen II molecular beam epitaxy (MBE) machine. The Al-content in the upper Schottky layer is 60% for the purpose of improving the gate Schottky barrier[3]. The InP sub-channel consists of 100Å InP and is uniformly-doped at 2×10^{18} cm^{-3} (Si). A 50Å InP channel spacer layer is inserted between the doped InP and the GaInAs channel layer.

The HEMTs were fabricated using a planar process. Source and drain

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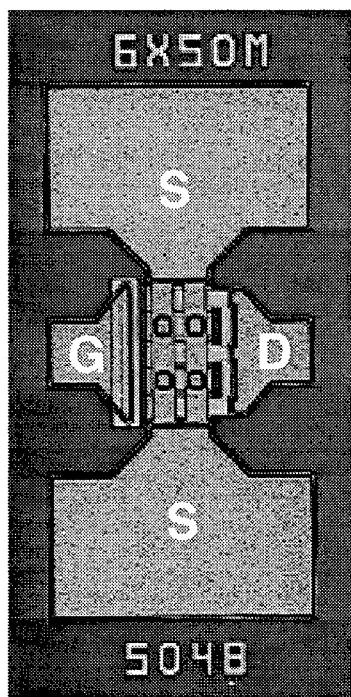
Figure 2. Topography of the 300μm (6-finger, 50μm-unit finger width) GaInAs/InP composite channel HEMT.

ohmic contacts were formed using Ag/AuGe/Ni/Au alloyed at 330°C for 35sec. The measured sheet resistance and specific contact resistance from TLM measurements are 230Ω/square and 0.25Ω-mm, respectively. A study of the ohmic contact characteristics for various composite channel structures is given elsewhere[4,5].

Boron ion implantation was used for device isolation. A 0.15μm T-shaped gate was deposited after adjusting the threshold voltage via a wet recess etch. The unit finger width of the HEMTs whose power performance is studied was 50μm as shown in device layout (see Figure 2). The devices were passivated with 1000Å of SiN. The wafer was

thinned to 2-mils, then the vias etched, followed by the backside metallization. Finally, the devices were die-attached on a copper carrier for testing.

DC Characterization

The peak transconductance is 720mS/mm with a full channel current (at Vgs=+0.5V) over 520mA/mm. The pinch-off voltage was approximately 1V as shown in the Ids/Gm-Vgs characteristic in Figure 3.

Devices with gatelength of 0.15 μm exhibit two-terminal and three-terminal gate-drain breakdown voltages of -10.4 and -13.3V, respectively (see Figure 4). The advantage of the composite channel device (with a 0.15μm gatelength) for power applications is clearly seen as the two-terminal breakdown voltage is nearly double the 7V two-terminal breakdown voltage of a GaInAs single channel device (with 0.2μm gatelength)[6].
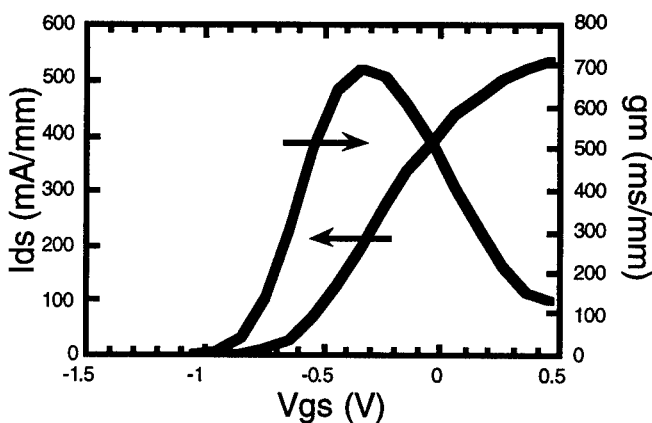
Figure 3. Normalized drain current and transconductance (both per gate width) versus gate voltage at Vds=1.5V.

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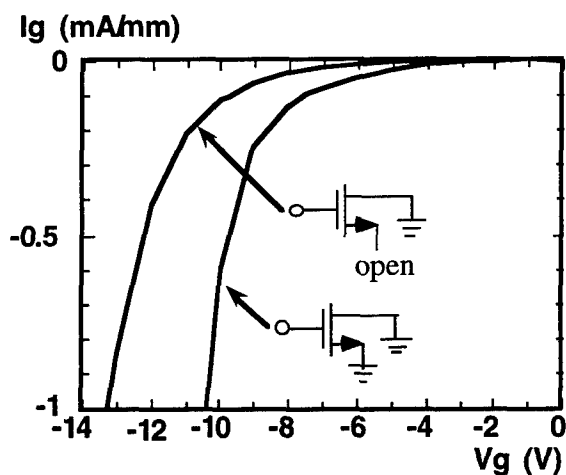
Figure 4. Two-terminal and three-terminal gate-drain breakdown characteristic.

Small-Signal Characterization

The small signal s-parameters were measured versus both gate ($^-$1.0 to $^+$0.5V) and drain ($^+$0.25 to $^+$2.0V) bias The peak F_T exceeds 150 GHz over the drain bias from $^+$1.0 to $^+$2.0V as shown in Figure 5. The F_{max} was measured at 2.5V (Vds) where it exceeded 200 GHz. The peak small-signal transconductance
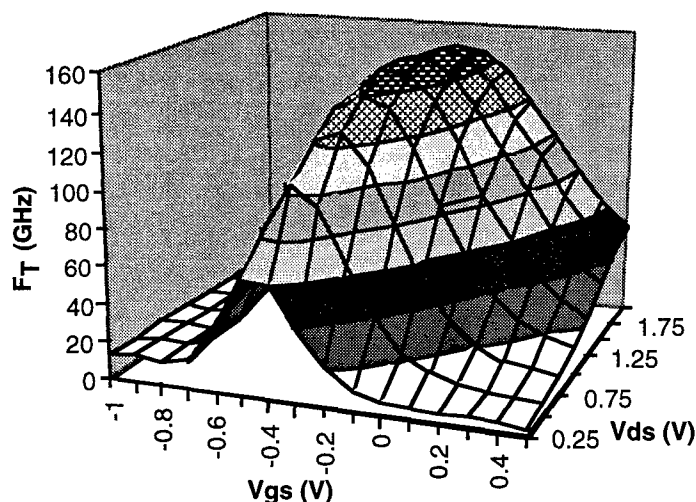
Figure 5. Measured current gain cut-off frequency of the 0.15µm gatelength (300µm-wide) GaInAs/InP composite channel HEMT versus gate and drain bias.

Vd=5.0V Vg=-.44V Id=70mA

POWER OUT vs POWER IN
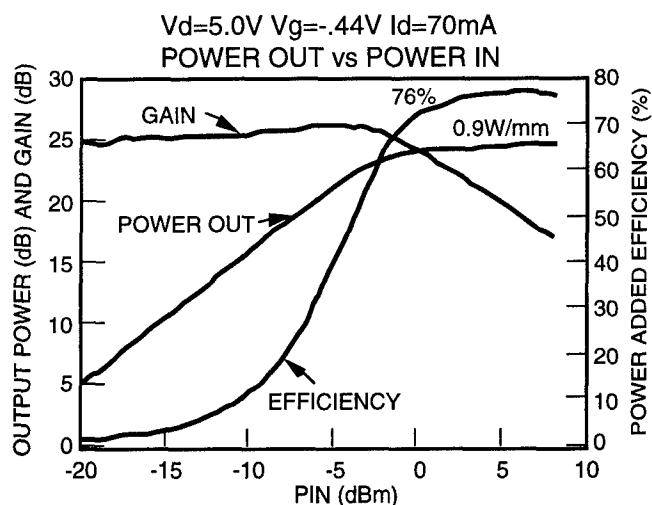
FREQUENCY: 7.00 GHz
Vd 5.001V
Vg -.440V
BIAS #:1
SOURCE STATE: 1 # 102
SOURCE IMP: .70 96.2
LOAD STATE: 1 # 372
LOAD IMP: .42 98.0

Pout @ 1 dB: 23.912
GAIN @ 1 dB: 24.619
EFF @ 1 dB: 70.683
Pout @ 3 dB: 24.318
GAIN @ 3 dB: 22.327
EFF @ 3 dB: 75.713

Figure 6. Measured Load Pull Characteristics of the 0.15µm x 300µm GaInAs/InP HEMT at 7GHz.

exceeded 830 mS/mm for ≥ 0.5V. The small-signal output conductance was 25mS/mm at a Ids=300mA/mm and Vds=2V.

Power Performance

The power transfer characteristics (see Figure 6) from devices with 300µm total gate periphery were measured using an on-wafer load-pull system at 7GHz. The devices were biased nominally at Vgs=-0.50V and Vds=+5.0V. The load was tuned only at the fundamental

22

GaInAs/InP Composite Channel Power HEMTs
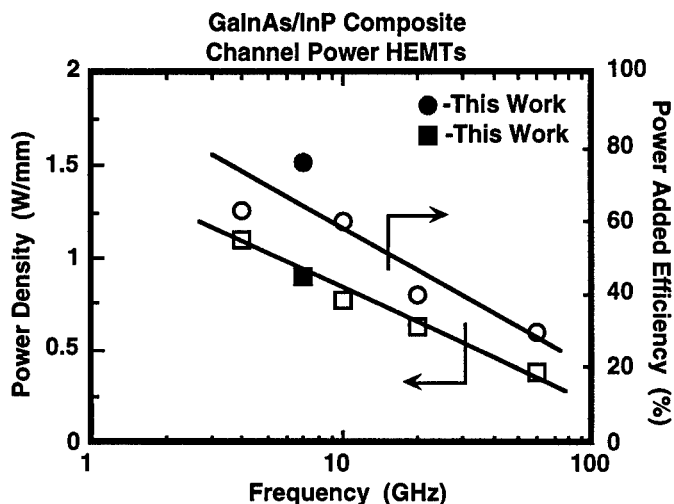
Figure 7. Comparison of power performance of GaInAs/InP composite channel HEMTs.

frequency. The quiescent drain current (with RF off) for the 300μm device was typically 230mA/mm. At the 1-dB compression point, the power output is 23.9 dBm (0.8W/mm) with 70% PAE and 24 dB gain. At the 3-dB compression point, the power output is 24.3 dBm (0.9W/mm) with 76% PAE and 22 dB gain. The load gamma magnitude (angle) for the 300μm device was 0.42 (98°). Power densities (P.A.E.) of 1.1W/mm (63%), 0.77W/mm (60%), 0.62W/mm (40%), and 0.38W/mm (30%) at 4GHz[7], 10GHz[8], 20GHz[9] and 60GHz[10], respectively have recently been reported for GaInAs/InP composite channel HEMTs (see Figure 7).

Conclusion

The utilization of the composite channel enables a high breakdown voltage while achieving excellent power

performance. A record combination of breakdown voltage, power density, and power added efficiency has been presented at 7GHz.

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23

HIGH POWER InAlAs/InGaAs/InP-HFET GROWN BY MOVPE

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Introduction

InAlAs/InGaAs Heterostructure Field-Effect Transistors (**HFET**) lattice matched to InP substrate show superior high frequency performance at shortest gate lengths [1] due to excellent material properties. But consequently, with reduced geometrical dimensions a significant lower breakdown voltage is observed. Recently, there is a great interest to improve the breakdown performance with special respect to high speed power applications [2]. Different types of breakdown (buffer [3], on-state impact ionisation [4], off-state gate-drain field [5]) have been identified. Novel HFET layer stacks with improved wide-band gap material [6,7], modified doping schemes [8] and gate-recess technology [9] have been developed. In this study we focus on the impact of an extended lateral gate-recess process in order to reduce the high electric field at the drain end of the gate and finally to improve the breakdown performance. In the first part we focus on HFET fabricated by optical lithography (L_g = 0.7 µm). The influence of various gate recess procedures on both, the breakdown voltage and the drain saturation current is studied for various thickness of the barrier and supply layer, respectively. High power class A amplifier exhibiting DC- (RF-) power capabilities in the range of 4-6 W/mm (0.5-0.75 W/mm) are presented. In the second part we introduce a hybrid lithography process combining both, optical and electron beam lithography. This way a shorter gate (L_g= 0.35 µm) is asymmetrically positioned in an extended lateral gate recess which enables both, high breakdown voltage and increased cut off frequency, respectively.

I. Material Growth and Device Fabrication

On s.i. InP:Fe substrate lattice matched modulation-doped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ heterostructures were grown by low-pressure metal-organic vapour-phase epitaxy (LP-MOVPE) [7]. The layer sequence and growth conditions in this study are summarised in fig. 1. The growth starts with a composite buffer (30 nm InP, 30 nm InAlAs). The epitaxial InP-layer was found to improve the layer quality, but to the expense of some conductance at the InP/InAlAs interface. This conductance was checked to have no impact on the HFET output conductance. But for a better device isolation we recommend to etch away the InP-buffer during the mesa etch. A low background concentration in the InAlAs layer is achieved at both, high growth temperature and high V/III-ratio [10]. In order to take care of sharp interfaces and good transport properties in the 20 nm $In_{0.53}Ga_{0.47}As$ channel layer the growth temperature was fixed at 680 °C while the V/III-ratio was switched from 900 in the InAlAs to 20 in the InGaAs. On the InAlAs spacer layer (3 nm) various thickness of both, the InAlAs supply- and barrier layer were realised while the sheet carrier concentration in the channel was kept constant (n_s = 2.8 - 2.9 cm^{-2}). The layer stack of all

fabricated HFET finished with a 10 nm thick undoped InGaAs cap layer.
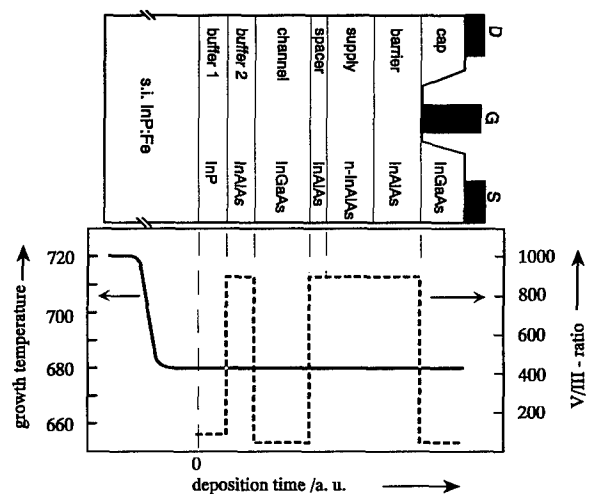
Fig. 1: Layer sequence and MOVPE growth parameters of the investigated InP-based HFET

We have grown various samples of the above described type. In the following we will focus on two typical

structures named sample A, B. The layer- and Hall- data of these samples are given in table 1.

Table 1: Layer and transport data of HFET A, B

	$d_{sup.}$ nm	$d_{bar.}$ nm	μ_n cm^2/Vs		n_s 10^{12} cm^{-2}	
			300K	77K	300K	77K
A	10	10	12,100	59,900	2.3	2.3
B	20	20	12,500	61,700	2.9	2.9

Device technology starts with wet chemical mesa etching using a H_2SO_4:H_2O_2:H_2O (1:1:40) etchant followed by a dip in HCl:H_2O (1:3) etchant in order to remove the InP buffer. A succinic based material selective etchant $C_4H_6O_4$:H_2O_2:NH_3 (20:4:1) is used exhibiting etch rates in InGaAs of 0.5 nm/s and in InAlAs of 0.007 nm/s with a corresponding selectivity of better than 1:70. This etchant is used for the mesa sidewall recess of InGaAs channel in order to reduce the gate leakage [11] and for the lateral gate recess. Ohmic contacts (Ge/Pt/Au) with a drain to source spacing of about 3.5 μm were evaporated and subsequently alloyed in a RTA at 410°C for 10 s. The contact resistance is about 0.2 Ωmm and the sheet resistance is about 200 Ω/sq deduced from TLM measurements. Finally, the gate was realised using a one step recess based on the succinic acid described above followed by a Pt/Ti/Pt/Au metallization. Using this highly material selective etchant enables a wide and symmetric recess trench on both sides of the metal gate. We developed a hybrid gate lithography process which combines both, optical patterning and ebeam-lithography. After the described optical patterning and etching of the 0.7 μm wide recessed trench the AZ-resist was removed. The ebeam process starts with the definition of the gate footprint using a two layer PMMA/MAA resist resulting in 0.35μm triangular shaped gates.

II. Analysis of Breakdown-Behaviour

A. Off-State Breakdown

The off-state breakdown voltage is determined by the measurement of the gate current I_G in reversed mode in dependence of the gate drain voltage V_{GD} using a open source circuit. The high material selectivity of the succinic based etchant results in a progressing lateral recess of the InGaAs cap in the range of 100 - 400 nm while the Schottky layer thickness remains high enough. The higher surface potential of the InAlAs results in a surface depletion of the recess trench which allows an lateral extension of the gate-drain space charge region and consequently an improved breakdown voltage as high as $V_{GDB,off}$ > 20V (I_G = - 300 μA). On the other hand this surface depletion and to some extend the reduced Schottky barrier thickness increases the access resistance

which is especially important on the source side of the gate.
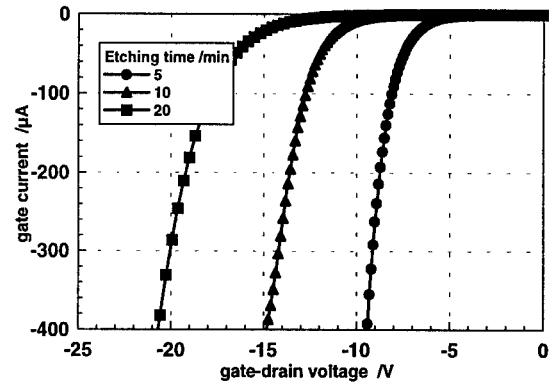
Fig. 2 $I_G(V_{GD})$ at reversed bias conditions (sample A) in dependence of the lateral etching time (W_G =30 μm)

B. On-State Breakdown

In correspondence with the increased off-state breakdown voltage an improved on-state breakdown voltage $V_{DSB,on}$ is expected. The catastrophic breakdown $V_{DSB,on}$ is determined by the measurement of the output characteristics at the highest available drain bias before irreversible breakdown at V_{GS} = 0.6 V. According to fig. 2 the corresponding IV-curves with different lateral gate recess were measured. As a result, $V_{DSB,on}$ impressively increased from 8 V over 15 V up to 28 V. Fig. 3 shows the output characteristics of the fabricated HFET. A with the most extended etching time of the gate recess of 20 min.
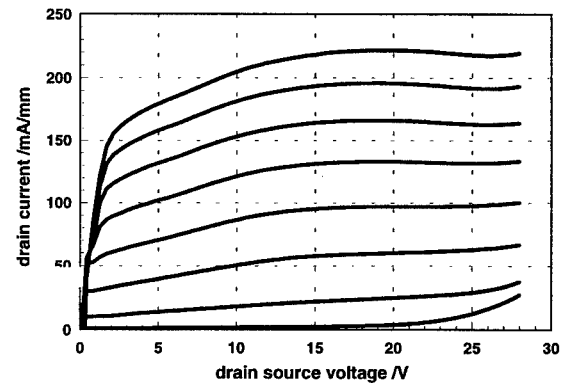
Fig. 3 Output characteristics $I_D(V_{DS}, V_{GS})$ of sample A, 20 min etching time, $V_{GS,start}$ = -0.1 V, $V_{GS,stop}$ = 0.6 V, $V_{GS,step}$ = 0.25 V

The fabricated device are suitable for a class A amplifier on InP allowing operation at a DC- (RF-) power as high as 6.3 W/mm (0.75 W/mm). Due to the remaining InAlAs etching, we observed a shift of the threshold voltage V_T to more positive values and simultaneously a decrease of the drain saturation current I_D. Consequently, we adjusted both, the supply and the barrier layer thickness for a predefined threshold voltage V_T. In

comparison to the layer structure of sample A, both, the barrier and supply layer thickness in case of sample B was increased to 20 nm while the carrier concentration in the channel was kept constant. Due to the thicker InAlAs layers in sample B the influence of the surface and Schottky potential is modified. In order to compare both samples we have extended in sample B the etch time to 40 min until a comparable threshold voltage is obtained. Under this condition the breakdown behaviour is comparable to sample A with 5 min etching time (fig. 4).
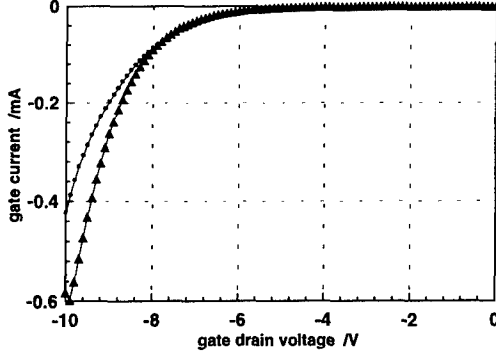
Fig. 4 Comparison of the reversed biased gate drain diode characteristics of sample A and B

This behaviour was confirmed by measuring the output characteristics of these both devices (fig. 5).
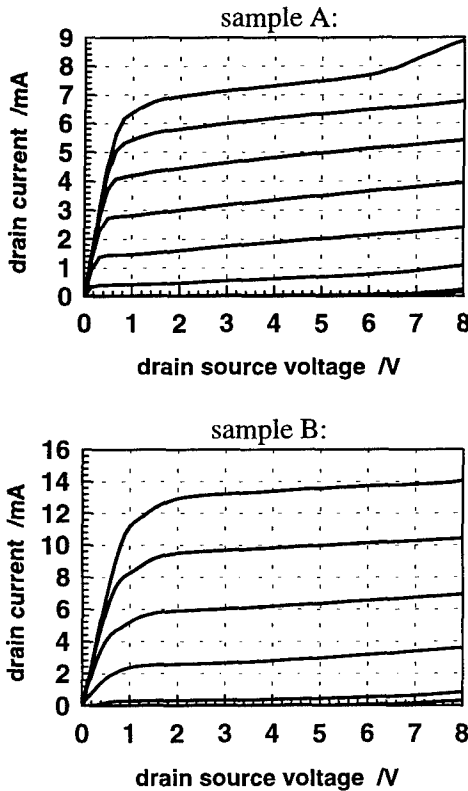
Fig. 5 output characteristics I_D (V_{DS}, V_{GS}) of sample A: $V_{GS,start}$ =-0.5V, $V_{GS,stop}$ = 0.6 V, $V_{GS,step}$ = 0.15 V and of sample B: $V_{GS,start}$ =-0.8V, $V_{GS,stop}$ = 0.7 V, $V_{GS,step}$ = 0.3 V

As can be seen, in contrast to sample A, sample B exhibits both, high drain saturation current I_D and significant negative threshold voltage V_T. In spite of nearly doubling the available drain current at V_{GS} = 0.4 V the same on-state breakdown voltage as high as $V_{DSB,on}$ = 8 V can be obtained. These investigations point out that with respect to the high power capability of the grown material the properties of the transistors can be influenced in terms of both, available drain current and breakdown voltages, as desired.

III. RF-Results

A. Optical Lithography

In this section the high frequency properties of the fabricated devices will be discussed. The gate length of the investigated HFET is L_G = 0.7µm. S-paramter measurements were performed at room temperature from 45 MHz - 45 GHz. Fig. 6 demonstrate the high frequency capability in terms of both, the cut-off frequency f_T = 18 GHz and maximum frequency of oscillation f_{max} of 116 GHz at extreme high drain bias of V_{DS} = 12 V.
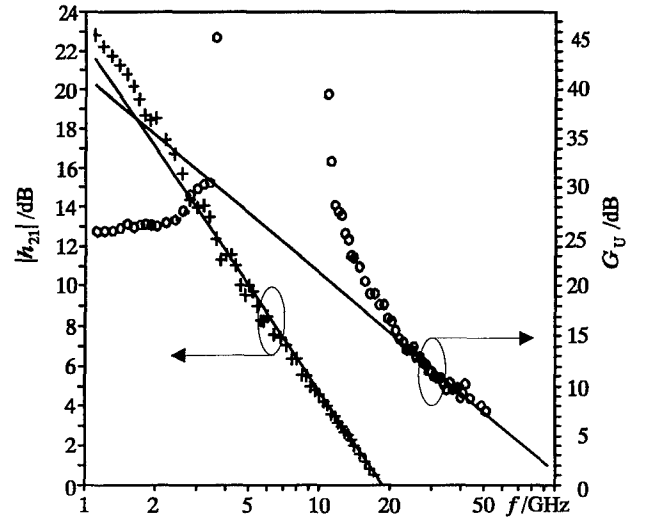
Fig. 6 Current gain $|h_{21}|$ and unilateral gain G_U versus frequency f at V_{DS} = 12 V (L_G = 0.7 µm, W_G = 80 µm)

The quite low value of f_T is not attributed to the high voltage operation but to the extreme wide gate recess trench towards the source resulting in a unavoidable high source resistance of R_S = 22 Ω. The extended space-charge region towards the drain substantially reduces the feedback capacitance and enables an extremely large f_{max}/f_t = 6.4 which is 2-3 times higher than in conventional InP-HFET.

B. EBEAM-Lithography

The gate length of high-breakdown HFET is reduced by support of electron beam lithography down to 0.35 µm. The gate is asymmetrically placed in the recessed trench exhibiting both, a reduced source resistance (R_S =12 Ω)

and simultaneously a wide recessed trench towards the drain preventing the loss of high breakdown voltages. This HFET device of type B exhibits a drain current of 600 mA/mm up to 6 V. The RF-performance of this sample B HFET is measured up to 3 V with the tendency that f_t increases from 1 to 3 V drain bias. Fig. 7 shows the improved cut-off frequency of f_T = 73 GHz and a maximum frequency of oscillation of f_{max} = 137 GHz. A further increase in the f_{max}/f_t is expected up to the highest allowable drain bias.
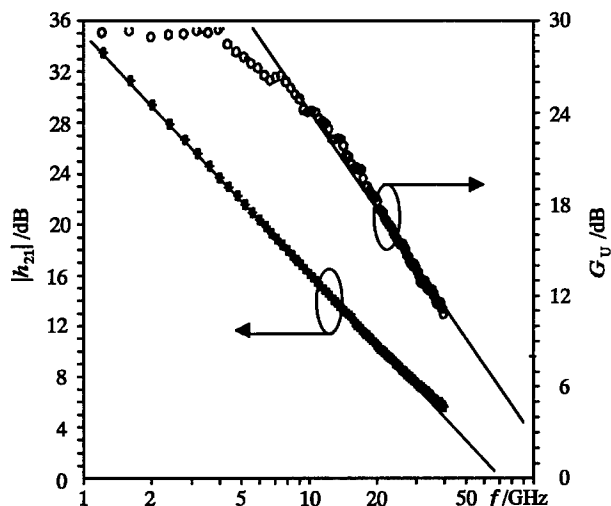
Fig. 7: current gain $|h_{21}|$ and unilateral gain G_U versus frequency f at V_{DS} = 3 V (L_G = 0.35 µm, W_G=80 µm)

IV. Conclusions

The impact on lateral gate recess technology is investigated for InP-based HFET´s. Extremely high breakdown voltages in excess of 25 V are achievable if a surface depletion besides the gate allow a lateral extension of the gate-drain space charge region. The combination of high power and high speed requires a reduction of the source resistance which is a consequence of the surface depletion in the gate-source region. For this purpose a lateral etch process is combined with a asymmetrically positioned short gate fabricated by a hybrid optical/ebeam lithography. This way class A-amplifiers may become feasible in the 0.75 W/mm range operating in the millimeter-wave regime.

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InP/InGaAs DOUBLE HBTs
WITH HIGH CW POWER DENSITY AT 10 GHz

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Abstract

High-performance InP/InGaAs double HBTs operating in common-emitter mode with 7.5 W/mm output power density at 10 GHz are reported. A total output power of 600 mW was achieved with five-finger cells having total emitter areas of 176 μm^2. Their f_T and f_{max} values are 74 GHz and 89 GHz, respectively. These cells exhibit small-signal maximum stable power gains of 17 dB and Mason's unilateral power gains of 20 dB at 10 GHz.

I. Background

HBTs are being developed for high-power microwave applications owing to their high power density, high efficiency and high breakdown voltage capabilities. These characteristics make them as well suitable for high-speed digital circuits operating at high power levels such as drivers for diode lasers, semiconductor optical amplifiers and optical switches. Due to the high junction temperatures at elevated power densities, the ultimate performance of high-power HBTs is thermally limited. Compared to GaAs HBTs, InP double HBTs (DHBTs) have the advantage of higher substrate thermal conductivity and of reduced temperature sensitivity of the current gain. These transistors are therefore expected to operate reliably at higher power densities than their GaAs counterparts. To date, CW power densities as high as 6 W/mm at 9 GHz have been reported for AlInAs/InGaAs/InP DHBTs (1) as well as an output power of 1 W at 9 GHz with 60 % power-added efficiency (PAE) (2).

This paper reports high-performance InP/InGaAs DHBTs capable of operation at high power densities. These DHBTs are similar to previous ones employed in digital driver circuits for laser diodes and optical switches (3). A detailed characterization of these transistors including the DC, small-signal and the large-signal RF-performance is reported in the following sections.

II. Device Structure and Fabrication

The main features of the DHBT structure, which is shown in Fig. 1., include a 87 nm base (Zn: $3.5 \cdot 10^{19}$ /cm^3) and a 600 nm collector (Si: $2.5 \cdot 10^{16}$ /cm^3). These relatively thick layers were chosen to achieve high power gains at high frequencies as well as to obtain high breakdown voltages. Since power transistors are operated at high currents, a thick

subcollector (total thickness 1250 nm) with low sheet resistance (5 Ω/sq.) was employed to reduce collector charging times and voltage drops in the subcollector and consequential saturation effects. The major part of the subcollector consists of InP, as InGaAs has an unacceptably low thermal conductivity (4). The epitaxial layer structure was grown by MOVPE. Details to the layer structure and to the fabrication process were reported in (3). The multifinger power DHBTs have emitter finger with areas of 2.2 x 16 μm^2. Each finger has an emitter ballasting resistor of 1.0 Ω. For thermal resistance reduction, the wafers were thinned to 150 μm and soldered with Indium onto heat-sinks. All measurements were performed on-wafer.

Layer	Material	Thickness [nm]	Doping [cm^{-3}]
Cap	InGaAs	300	Sn: $2 \cdot 10^{19}$
Emitter	InP	200	Si: $4 \cdot 10^{17}$
Spacer	InGaAs	5	none
Base	InGaAs	87	Zn: $3.5 \cdot 10^{19}$
Spacer	InGaAs	35	none
Delta doping	InP	15	Si: $1 \cdot 10^{18}$
Collector	InP	600	Si: $2.5 \cdot 10^{16}$
Subcollector	InGaAs	300	Sn: $1 \cdot 10^{19}$
Subcollector	InP	950	Si: $1 \cdot 10^{19}$

Fig. 1   InP/InGaAs DHBT epitaxial layer structure.

III. HBT Characteristics

The common-emitter I-V curves of a five-finger DHBT are shown in Fig. 2. Maximum collector current density J_C reaches values up to $2.0 \cdot 10^5$ A/cm^2. The DHBTs exhibit a maximum small-signal current gain $\beta = 23$ and a breakdown voltage $BV_{CEO} = 13.0$ V. The knee voltage is 0.8 V at a collector current density $J_C = 1.0 \cdot 10^5$ A/cm^2. The collector-emitter voltage offset is as low as 95 mV.
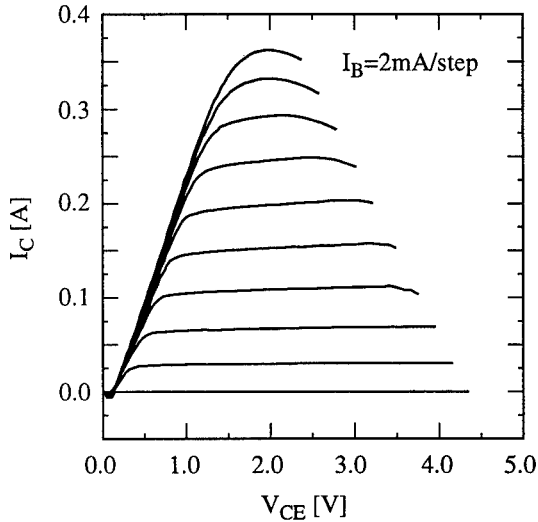
Fig. 2 InP/InGaAs power DHBT common-emitter characteristics I_C-V_{CE}. Emitter area is $5 \times 2.2 \times 16$ μm^2.

The small-signal cutoff frequencies obtained from S-parameter measurements from 0 to 40 GHz for transistors with different emitter areas are shown in Fig. 3.
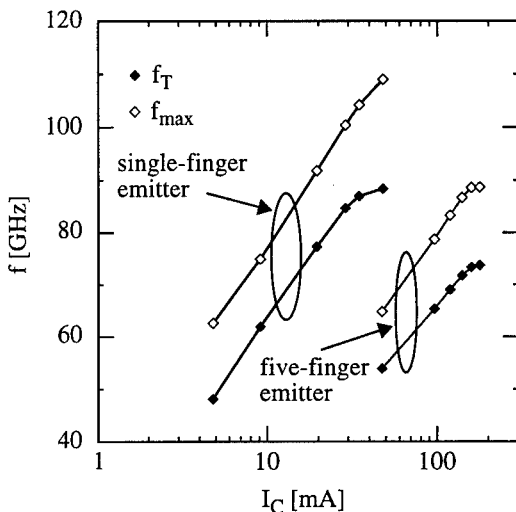
Fig. 3 Current gain and power gain cutoff frequencies, f_T and f_{max}, versus collector current I_C of two InP/InGaAs DHBTs, one with single-finger structure (2.2×16 μm^2 emitter area) at $V_{CE} = 1.8$ V, and the other with five-finger structure ($5 \times 2.2 \times 16$ μm^2 emitter area) at $V_{CE} = 2.5$ V.

Single-finger DHBTs with emitter sizes of 2.2×16 μm^2 have maximum f_T and f_{max} values of 88 GHz and 109 GHz, respectively. The corresponding values for five-finger DHBTs are 74 GHz and 89 GHz. The lower cutoff frequencies for the multifinger DHBTs are a result of the larger parasitics and the presence of ballasting resistors. The small-signal current and power gains versus frequency for a DHBT with five emitter fingers are shown in Fig. 4. At 10 GHz the values for the maximum stable gain (MSG) and Mason's unilateral gain (U) are 17 dB and 20 dB, respectively. Small-area DHBTs with 0.8×8 μm^2 emitters reach $f_T = 87$ GHz and $f_{max} = 173$ GHz, the latter being a very high value for a power HBT structure. These transistors have MSG and U values at 10 GHz of 21 dB and 26 dB, respectively.
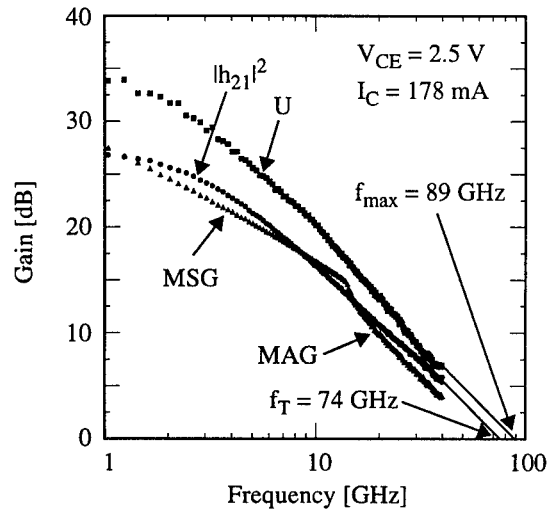
Fig. 4 Small-signal current gain $|h_{21}|^2$, maximum stable (MSG), maximum available (MAG) and Mason's unilateral (U) power gain versus frequency of an InP/InGaAs power DHBT with $5 \times 2.2 \times 16$ μm^2 emitter area at $V_{CE} = 2.5$ V and $I_C = 178$ mA.

CW RF-power measurements were performed at 10 GHz by using coaxial mechanical tuners. The tuners were adjusted for maximum output power. The five-finger DHBTs were biased for near class B common-emitter operation, with a collector-emitter voltage $V_{CE} = 7.0$ V. The base-emitter voltage was kept constant with a collector current $I_C = 1$ mA at zero RF-power at the input. Under these bias conditions, the maximum output voltage swing is approximately 12 V, which is the limit imposed by BV_{CEO}. Fig. 5a shows the output RF-power and the power gain as functions of the input RF-power. The peak output power is 600 mW, corresponding to a 7.5 W/mm or a 3.4 mW/μm^2 power density. These values are very high, considering that only wafer thinning was used to reduce thermal resistance and no thermal shunts or backside vias were employed. The output power at 1-dB gain compression is 550 mW. Maximum power gain is 8.8 dB. As a consequence of the on-wafer measurement setup with lossy connections between mechanical tuners and measurement sample, it is not

possible to obtain perfect impedance matching to the low-impedance transistor input. The effective power gain of these transistors is therefore expected to be larger than the values in Fig. 5a. In fact, for two-finger DHBTs having an higher input impedance and optimized input matching, a maximum power gain of 10.5 dB was measured for similar bias conditions. The PAE and the average collector current versus input power of the five-finger DHBT are shown in Fig. 5b. The maximum PAE is 46%.

(a)

(b)
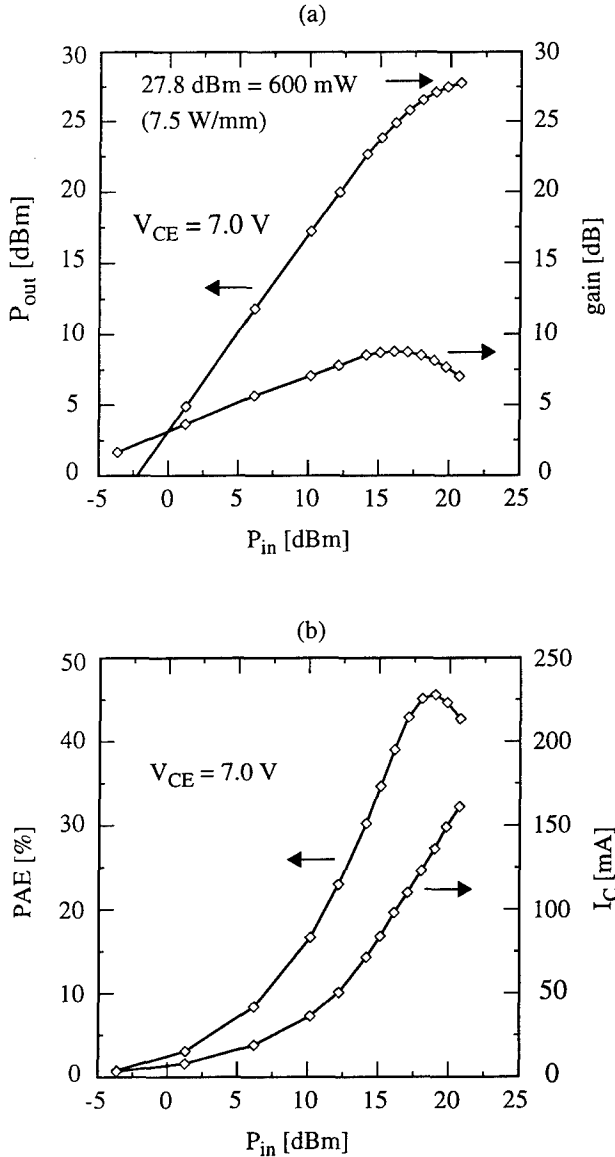
Fig. 5   InP/InGaAs power DHBT with $5 \times 2.2 \times 16 \, \mu m^2$ emitter area biased at $V_{CE} = 7.0 \, V$ and $I_C = 1 \, mA$.
(a) Output power and power gain versus input power at 10 GHz.
(b) Corresponding PAE and average collector current I_C versus input power.

The thermal resistance θ was obtained by measuring the temperature dependence of the base-emitter bias for a constant emitter current at different power levels and temperatures (5). For a power DHBT with 5 fingers, a room-temperature value for θ of 210 $K \cdot W^{-1}$ or 16.8 $K \cdot W^{-1} \cdot mm$ was obtained. The latter value is comparable to values obtained for AlGaAs/GaAs HBTs with similar total device areas, but with thinner substrates (100 μm) (5), which is a direct result of the higher thermal conductivity of InP compared to GaAs. The arrangement of the emitter fingers is shown in the chip photograph in Fig. 6. The junction temperature for the maximum RF output power operating condition is estimated to be below the ceiling temperature of 150 °C typically targeted for microwave power applications. The transistors are therefore expected to operate reliably even at the high power densities reported above.
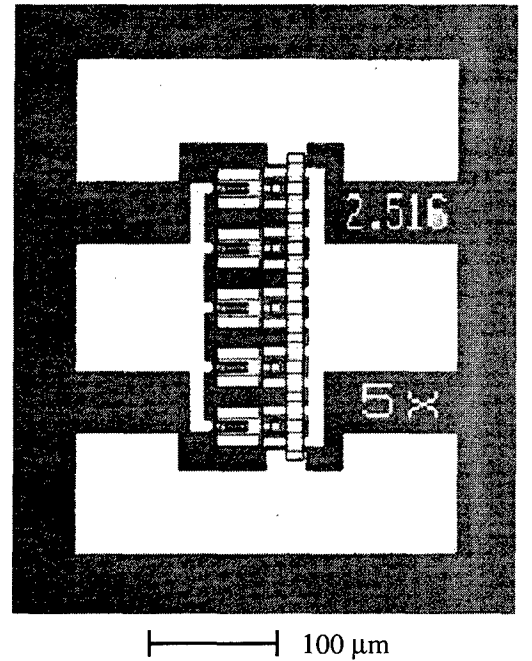
Fig. 6   Photograph of a 5-finger DHBT power cell.

IV. Conclusions

The performance of InP/InGaAs DHBTs capable of operation at high speeds and high power levels is reported. Major characteristics of these high-performance transistors combine high maximum collector current density, high breakdown voltage, low knee voltage, as well as excellent small-signal and large-signal high-frequency behaviour. The CW power density of 7.5 W/mm obtained at 10 GHz, which was achieved without the use of thermal shunts or backside via processing, is one of the highest values reported for a microwave power transistor. These characteristics make these transistors suitable for compact microwave power applications

as well as for high-speed digital circuits operating at high power levels such as drivers for laser diodes, semiconductor optical amplifiers and optical switches.

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InAlGaP Vertical Cavity Surface Emitting Lasers (VCSELs): Processing and Performance

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Introduction

$(Al_yGa_{1-y})_{1-x}In_xP$ semiconductor alloys lattice-matched to GaAs are widely used in visible optoelectronic devices. One of the most recent developments in this area is the AlGaInP-based red vertical cavity surface emitting laser (VCSEL) [1,2]. These lasers, which employ AlGaInP active regions and AlGaAs distributed Bragg reflectors (DBRs), have demonstrated continuous-wave (CW) lasing over the 630-690 nm region of the spectrum [2,3]. Applications for these lasers include plastic fiber data communications, laser printing and bar code scanning. In this paper, we present an overview of recent developments in the processing and performance of AlGaInP based VCSELs. This overview will include a review of the general heterostructure designs that have been employed, as well as the performance of lasers fabricated by both ion implantation and selective oxidation.

I. General Heterostructure design of AlGaInP VCSELs

The general design for the visible VCSEL active region is similar to that which has been employed in AlGaInP edge emitting lasers. It includes compressively strained $In_{0.56}Ga_{0.44}P$ quantum wells with $(Al_yGa_{1-y})_{0.5}In_{0.5}P$ barriers and cladding layers. The quantum well thickness is typically 70 Å with 65 Å barriers. The one wave thick cavity is approximately 2000 Å for the 670 nm region. A schematic of the active region is shown in Figure 1.
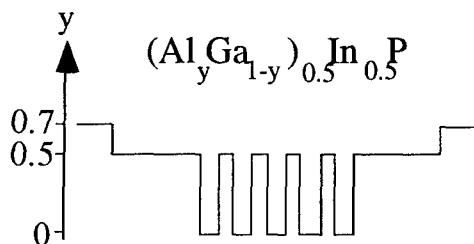
Figure 1: Heterostructure design for AlGaInP based visible VCSEL active region

The DBRs for the visible VCSELs are $Al_xGa_{1-x}As$ alloys and typically x=0.5 alloys have been used for the high index layer and x=0.92-1 alloys have been used for the low index layers . Bi-parabolic grading of the alloy composition is employed between the layers to reduce the resistance of the mirrors. For these top emitting devices, up to 36 high and low index layer pairs are used in the top DBR and 55.5 pairs are used in the bottom DBR [1, 2, 8].

II. Processing of Visible VCSELs

The most conventional VCSEL structure is a planar design utilizing ion implantation to define the current aperture of the lasers and to provide isolation from neighboring devices. Significant advances in the performance of both near-IR and visible VCSELs have been realized by employing an alternate fabrication technique, namely selective oxidation, in the processing of the VCSEL [3-8]. This technique involves the preferential oxidation of one or more relatively high aluminum containing AlGaAs layers in the DBRs near the active region of the device. In the visible VCSEL design, the low index layer of the top DBR pair closest to the cavity is typically $Al_xGa_{1-x}As$ with x=0.98 and x=0.95 is typically used for the remaining low index layers. One to five x=0.98 layers have been employed in a given design.

In the selective oxidation process, mesas are fabricated by dry etching down to the AlGaInP layers. The devices are oxidized in a wet steam furnace at 440 °C with an oxidation rate of approximately 0.8 µm/min.
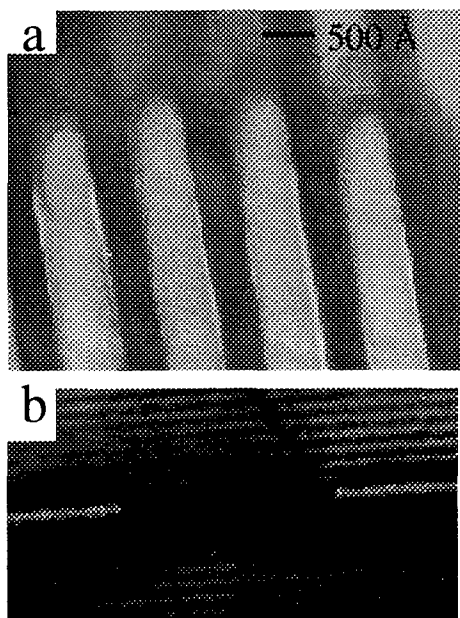
Figure :2 TEM images of a) edges of four oxide layers and b) oxide defined aperture in near-cavity region of a selectively oxidized VCSEL. The oxide aperture in (b) is approximately 3 μm.

TEM images of oxidized visible VCSELs are shown in Figure 2. In Figure 2a, we show the edges of four neighboring oxidized layers, demonstrating the sharp definition of the oxide layers. Figure 2b shows a single oxidized layer above the AlGaInP cavity, where the aperture created by the oxide layer is approximately 3 μm. Nearby regions of the top and bottom DBR are also seen in the image. The thin (500 Å) and low index (n = 1.55) aluminum-oxide layer serves to provide both electrical and optical confinement and can enable well defined device diameters as small as 1 μm.

III. Performance of Visible VCSELs

The performance of visible VCSELs has advanced markedly over the past several years. State of the art performance includes the demonstration of 2 mW single mode power at 690 nm, > 8 mW multimode at 690 nm and up to 11 % wallplug efficiency from ion implanted devices [2]. Selectively oxidized devices have been demonstrated with reduced threshold conditions (Ith < 1 mA) [8] as compared to ion implanted structures and with CW lasing down

to 630 nm [3]. In this section, we review further advances that have been made with improvements in heterostructure design and selective oxidation.

A. High Temperature Performance of Ion Implanted and Selectively Oxidized VCSELs

One of the areas in which visible VCSEL performance has lagged behind that of near-IR VCSELs is in high temperature performance. Achieving CW lasing from visible VCSELs at elevated temperatures is challenging due to enhanced carrier leakage in the AlGaInP-based active region [9] as compared to the GaAs and InGaAs quantum well active regions of 850 nm and 980 nm VCSELs, respectively .

While previously reported visible VCSEL designs incorporated $(Al_{0.5}Ga_{0.5})_{0.5}In_{0.5}P$ barrier layers with no cladding layers [2], recent designs have included higher bandgap $(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$ cladding layers, as shown schematically in Figure 1. The temperature dependent performance of both implanted and selectively oxidized structures incorporating this design have been evaluated.

In Figure 3, we show temperature dependent light output power-current-voltage (L-I-V) data for a 10 μm diameter ion implanted VCSEL employing the higher bandgap $(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$ cladding layers. The lasing wavelength is 677 nm at 25°C. The VCSEL structure has a cavity mode/ gain peak offset of approximately 7 nm to improve performance above room temperature, although the design was not specifically optimized for high temperature performance. CW lasing up to 75 °C has been achieved with a change in peak power with temperature of -0.029 mW/°C. Exact comparison with previously reported data on devices which do not employ the $(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$ cladding layers is difficult due to the fact that the optimized devices were 15 μm in diameter with emission at 690 nm. However, best performance previously achieved in these structures demonstrated a -0.075 mW/°C peak power change with temperature and CW lasing up to 60 °C [2].
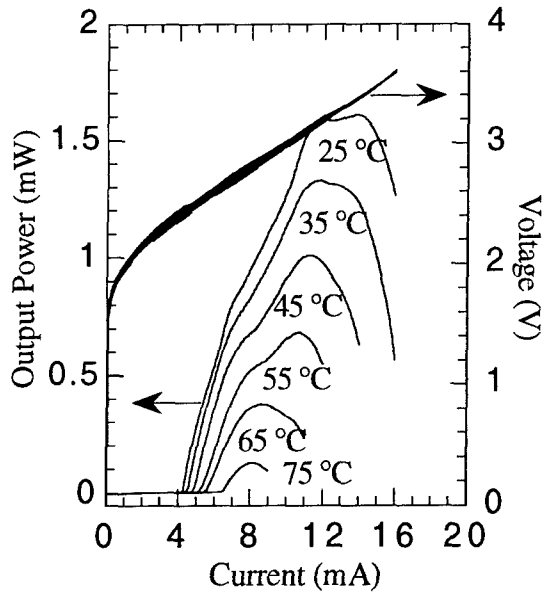
Figure 3: Temperature dependent L-I-V data for an ion implanted VCSEL with $(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$ cladding layers.
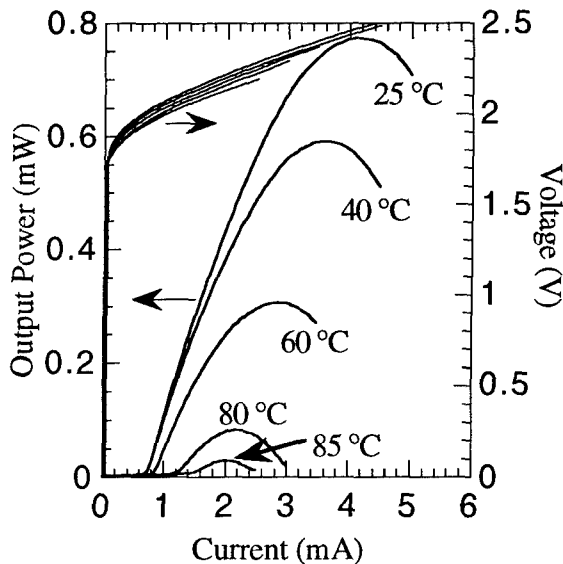
Figure 4: Temperature dependent L-I-V data for a selectively oxidized VCSEL with $(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$ cladding layers.

Selectively oxidized visible VCSELs have the potential to achieve CW lasing at even higher temperatures, due to their high efficiency and low input power requirements. As an example, in Figure 4, we show the performance of a 3 μm x 3 μm selectively oxidized VCSEL with a similar active region as the ion implanted device represented in Figure

3. The lasing wavelength is 683 nm at 25 °C. Although the maximum output power of the device is less, CW lasing up to 85 °C is achieved and low threshold voltages of 2.0 V over the 25-80 °C temperature range are seen. The drop in peak power with temperature is slightly less than for the ion implanted structure, namely -0.0125 mW/°C.

B. Low Threshold Performance of Selectively Oxidized VCSELs

The small volumes and enhanced electrical and optical confinement provided by selective oxidation has resulted in improved threshold performance and wallplug efficiencies for both visible [8] and IR VCSELs [10-12]. Recent work on red VCSELs has included design changes to improve these properties. As previously mentioned, applying $(Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P$ cladding layers was performed to reduce carrier leakage. Another area of device design that was explored was the number of oxide layers above the active region. Previous designs employed 5 oxide layers [8], while fewer pairs are expected to improve performance due to reduced scattering loss.

In Figure 5, we present L-I-V data of a design employing 2 oxide layers above the AlGaInP cavity. A low threshold voltage of 1.980 V (only 135 meV above the photon energy) has been achieved. This device also demonstrates a relatively low threshold current of 0.6 mA and a peak wallplug efficiency of 12.2%, the highest value reported for visible VCSELs.

We have also explored the performance of selectively oxidized VCSELs with varying top mirror reflectivity. The devices previously mentioned have employed 34 top mirror pairs, which results in a top mirror reflectivity of approximately 0.9981. CW lasing has been achieved with structures employing 28-36 mirror pairs, with an effective range of reflectivity of 0.9948-0.9986. In Figure 6, we show L-I-V data from a 2 μm x 3 μm selectively oxidized VCSEL with 36 top mirror pairs. The device demonstrates a low threshold current of 0.38 mA and a threshold voltage of 2.10 volts.
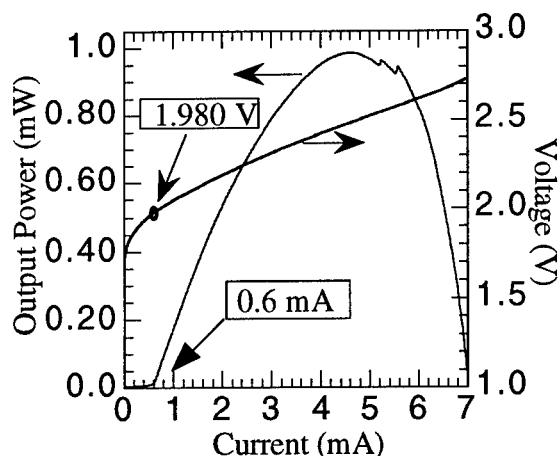
Figure 5: L-I-V data for a 3 μm x 3 μm selectively oxidized visible VCSEL with 34 top DBR pairs and emission at 672 nm.
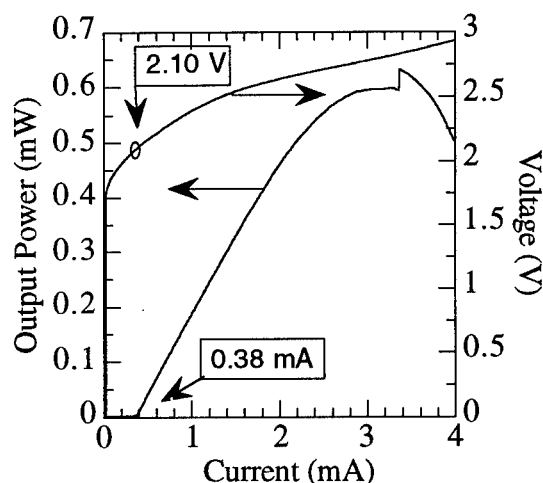
Figure 6: L-I-V data for a 2 μm x 3 μm selectively oxidized VCSEL with 36 top mirror pairs. Emission is at 673 nm.

IV. Conclusions

The performance of AlGaInP based visible VCSELs has been advanced with the application of new heterostructure designs and the technique of selective oxidation. Improved performance at elevated temperatures as well as high wallplug efficiency, low threshold devices have been demonstrated for devices operating in the 670-680 nm region. Challenges still remain in demonstrating high performance devices with emission wavelengths shorter than 650 nm.

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Temperature Performance Of 1.55μm Vertical Cavity Lasers With Integrated InP/GaInAsP Bragg Reflector

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Introduction

Long wavelength vertical cavity lasers (VCL) have gained considerable interest after the first continuous wave (CW) room temperature (RT) operating devices were fabricated[1]. As a potential light source for future optical communication systems, they offer a number of advantages such as array fabrication, on-chip-testability, cost effective fabrication, and effective fiber coupling. We fabricated 1.55μm laser diodes based on an integrated GaInAsP/InP mirror. Here we focus on the temperature sensitivity, especially of the threshold current as a function of the gain offset (cavity tuning).

I. Background

Long-wavelength laser diodes show a strong temperature dependence, especially of the threshold current[2]. This is caused by carrier leakage across the quantum wells and high non-radiative losses such as inter valence band absorption (IVBA) and Auger recombination[3]. The behaviour of $I_{thr}(T)$ is found to be considerably different from edge emitters[4,5,6,7]. The temperature behaviour of Fabry-Perot (FP) edge emitters can be characterised by the parameter T_0 while for VCL it has to be used with care. Here, the mode spacing is large and usually there is only one mode in the range of the gain linewidth. Unlike in FP edge emitters, varying the temperature leads to an offset $\lambda_p - \lambda_c$ of gain peak wavelength, λ_p, and cavity mode, λ_c. Especially at low temperatures, this mismatch dominates the temperature sensitivity. Besides of the choice of active material and the cavity design it is important to realise the optimal gain offset in order to reach low threshold current and high output power. For pulsed operation, it is commonly assumed that the gain peak should match the cavity mode (no heating). For CW, a certain offset should be considered due to the heating of the active layer and cavity. Another common design rule says that the temperature related minimum in threshold current occurs for that matching case[7,13]. This rule does not apply to the lasers investigated in this paper. We analyse the output characteristics of 1.55μm VCL, based on an InP/GaInAsP integrated bottom mirror. This design offers full-wafer-scale fabrication, in contrast to the successfully operating wafer fused devices[1,8]. Lasers with a varying gain offset are fabricated and the threshold current for different temperatures is recorded. The results are compared to numerical simulations.

II. Design and Fabrication

Two different devices were fabricated: Fig 1(a) shows the low mesa structure, embedded in polyimide. Fig 1(b) is basically the same structure, but a semi-insulating (SI) InP regrowth is employed in order to improve thermal properties and reduce leakage along the mesa surface.
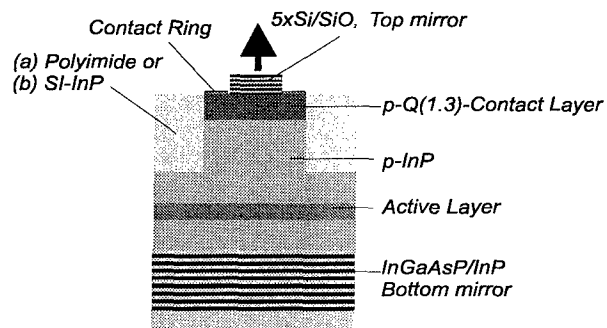
Fig. 1: VCL structures with a 50 period InGaAsP/InP integrated bottom mirror, strain-compensated multi-quantum-well active, and Si/SiO2 top mirror. (a) embedded in polyimide, (b) regrown with SI-InP

The devices are fabricated in two steps, using low-pressure metal organic vapour deposition. In the first step the bottom mirror is grown, consisting of 50 pairs of n-type (Si) GaInAsP/InP quarter-wavelength thick layers. The nominal plane-wave reflectivity is 99.9%. In a second step, the active region of nine compressively (+1% cs) strained, 7nm thick GaInAsP quantum wells (QW) and strain-compensating (-0.9% ts) 8nm thick GaInAsP barriers is grown. Details about the MQW structure and the growth procedure are described elsewhere[9]. The Zn-doped p-cladding InP and p+-GaInAsP (1.3μm)-contact layers are grown on top of the active, resulting in a cavity length of 4.5λ.

For later investigations, it is necessary to determine the PL-spectrum of the QW-structure properly. A reference piece *without* underlying mirror is grown in the same run as the lasers, since the PL of the active material on top of a mirror is always modulated by the cavity formed between the mirror and the semiconductor-air interface on top of the structure.
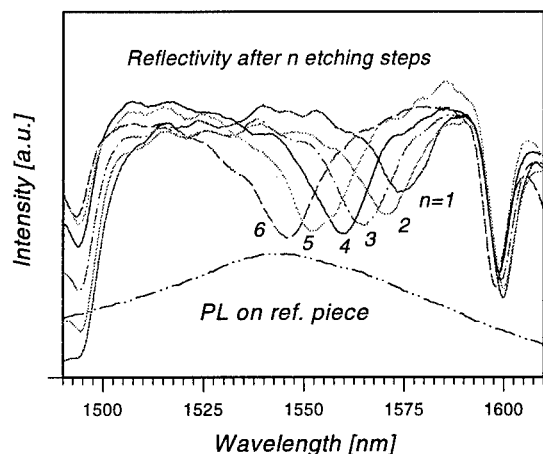
Fig. 2: Controlled thinning of contact layer and related shift of cavity resonance before deposition of the top mirror

Here, the PL peak wavelength λ_{PL} is roughly tuned to the desired PL offset. For the fine tuning the wavelength position of the cavity resonance can be further corrected by controlled RIE (reactive ion etching) thinning of the contact layer, see Fig. 2. For the laser processing, circular 1.6 µm high mesas with diameters between 5 and 22µm are etched and either embedded in polyimide or regrown with SI-InP (grown by hydride vapour phase epitaxy). The processing is concluded by the deposition of a Si/SiO$_2$ mirror with a diameter between 3 and 20µm. The actual cavity mode position at this stage is given by the emission line of the lasers.

III. Characteristics

In the following devices of a diameter of 15µm are analysed. For structure (a), pulsed RT operation is achieved at a threshold current of 30mA, corresponding to a current density of 13kA/cm^2.
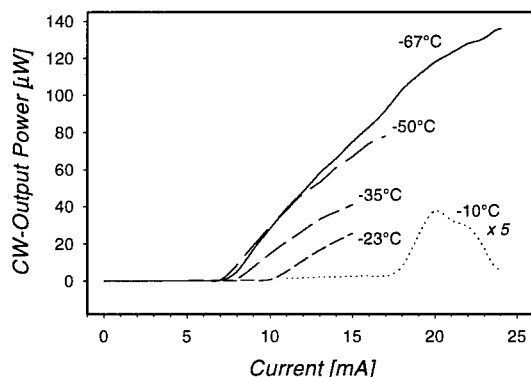
Fig. 3:   Typical CW output characteristics of a SI-InP-regrown 15µm laser for a set of temperatures

The linewidth is less than 0.1nm. The differential resistance at threshold is 18Ω, and the threshold voltage is 1.8V. The lasers operate pulsed within the ambient temperature range of -160°C to +42°C[10]. CW-operation is achieved at temperatures up to -25°C, even though the lasers are not designed for CW. The regrown structure, Fig. 1(b), operates CW up to -9°C, clearly indicating the improved heat conductivity off the active layer due to the SI-InP. Typical CW-output characteristics for several temperatures are shown in Fig. 3. Output powers of more than 100µW are achieved for low temperature.

IV. Temperature Impact

Differential quantum efficiency: For the polyimide embedded devices, a very low external quantum efficiency is found. This is most likely explained by a surface leakage channel along the mesa, caused by defect induced (RIE) non-radiative recombination. Another indication for this leakage is a small temperature rise in the active region. According to numerical simulations, the CW active region heating is expected to be three times higher than measured, indicating that a large part of the heat power is generated far away from the active region
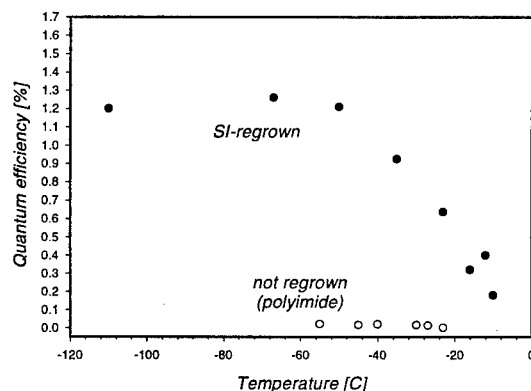
Fig. 5: Differential optical efficiency as function of temperature for VCL with and without SI-InP regrowth

Employing SI-regrowth instead of polyimide, the quantum efficiency increases by a factor of 50 (Fig. 5). Here, the regrowth eliminates the leakage current channel along the surface. Despite of this, the threshold currents are still high, most likely due to absorption in the p-doped contact layer. The differential efficiency also depends on the temperature, caused by changes in the refractive indices as well as in the absorption coefficients. Especially IVBA within the MQW or within other layers with high hole concentration could reduce the quantum efficiency at higher temperatures[2]. In the pulsed measurements, a strong reduction of $\eta_d(T)$ is observed above 0°C in agreement with the simulation, indicating the influence of IVBA in the VCL. For CW operation, the quantum efficiency drops for temperatures above -30°C, indicating a temperature rise in the active region of at least 30°C.

To determine the temperature dependent gain offset, the PL (band gap) and the laser line (cavity) are measured as a function of temperature.

37
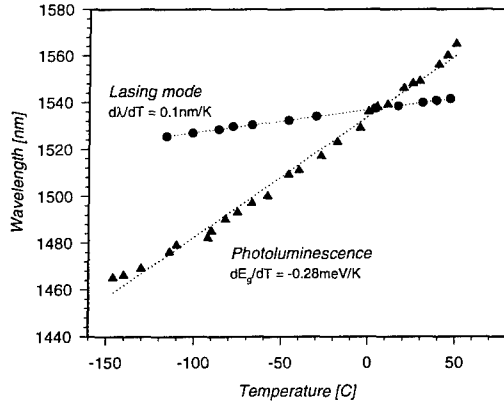
Fig. 4: Variation of cavity mode and PL, respectively, with temperature. At RT, the gain peak is 8nm above the PL

Energy band gap: Fig. 4 shows the PL peak wavelength λ_{PL} as a function of temperature. λ_{PL} shifts by 0.54nm/K, resulting in $dE_g/dT = -0.28meV/K$.

Cavity mode: With increasing temperature, the cavity mode λ_c red-shifts due to the temperature dependence of the refractive index dn/dT and layer thickness. dn/dT is assumed to be $2 \cdot 10^{-4}K^{-1}$ for the semiconductor, $1 \cdot 10^{-4}K^{-1}$ for Si and $1 \cdot 10^{-5}K^{-1}$ for SiO_2. The measurement yields $d\lambda_c/dT = 0.1nm/K$ (Fig. 4). Thus, the cavity wavelength $\lambda_c(T)$ red-shifts about six times slower than the PL peak $\lambda_{PL}(T)$ with rising temperature.

V. Active Layer and Optical Gain

The active layer has to be analysed carefully since gain calculations are very sensitive on the composition and the thickness of well and barrier. This is done by high resolution X-ray diffraction and the recorded PL-spectrum. The computation of the band structure using the values given by this procedure shows that due to strain compensation, light holes experience almost no quantum confinement as well as a considerable amount of MQW carriers can be assumed outside the QWs at high injection. On the other hand, the distance of the QW states to the InP spacer band edges is relatively large (241meV and 302meV, respectively) and no significant carrier escape rate from the MQW is expected at RT.

The following analysis is done for the polyimide embedded structure only and assumes pulsed operation. Self-heating of the laser is neglected. Using the parameters of the active layer as well as the values for the temperature shift of band gap and cavity mode, the material gain $g(\lambda,N,T)$ is calculated as a function of wavelength, temperature and carrier density. The gain model is based on Fermi's golden rule and 4x4 **kp** band structure computations for the strain-compensated MQW active region[11]. Fig. 6 shows the gain spectrum calculated for different temperatures and carrier densities. At RT, the gain peak wavelength λ_p is located 8nm above the PL peak wavelength λ_{PL}. The height g_{max} of the gain peak also shifts with temperature almost linearly by $dg_{max}/dT = -11cm^{-1}K^{-1}$ (Fig. 6(a)). This is caused by the increased spreading of the carrier's Fermi distribution with rising temperature.

(a)   *(b)*
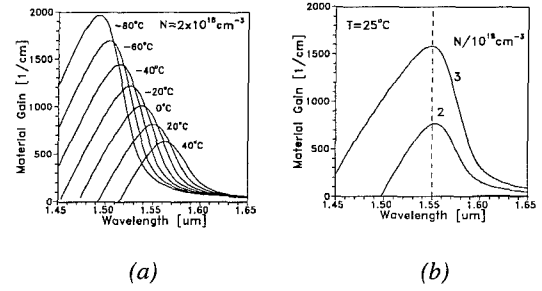
Fig. 6: (a) MQW gain spectrum at different ambient temperatures showing the thermal shift of the peak wavelength λ_p as well as of the peak height g_{max}. (b) Calculated spectrum of the MQW optical gain with the carrier density as a parameter

VII. Influence of Gain Offset on Threshold Current

The measured emission wavelength (cavity mode) changes slightly with the VCL position due to inhomogeneous layer thickness across the wafer, leading to different RT gain offsets. Taking the offset as a parameter, the pulsed threshold current is measured as a function of temperature (Fig. 7). The minimum threshold current occurs at different temperatures because of the different RT gain-offset. To further evaluate the effect of the gain-offset, numerical simulation is applied[12].
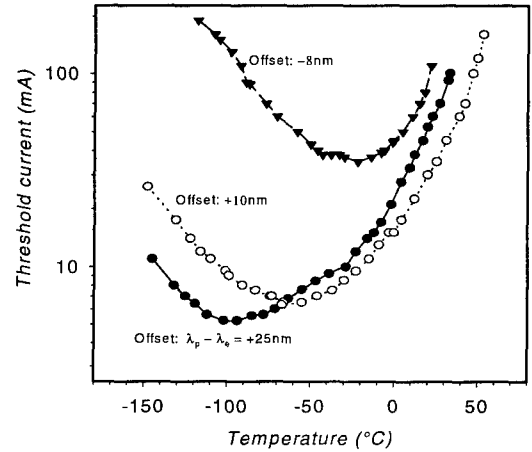
Fig. 7: Measured threshold current for three different RT-gain-offsets as a function of ambient temperature

We take the curve in Fig. 7 showing the minimum at -60°C as an example: This device exhibits a RT-gain offset of +10nm (i.e. a PL-offset of +2nm). Firstly, the transfer matrix method is employed to obtain emission wavelength λ_c, threshold gain g_{th}, and differential optical efficiency η_{opt} as function of the ambient temperature. In a second step, MQW gain calculations are performed for any given wavelength and temperature, leading to the threshold carrier density N_{th} as a function of the temperature (solid curve in Fig. 8).The calculation shows the following: perfect *match of gain and mode occurs for 0°C.* Despite of this, the *minimum in threshold current occurs at -30°C.* This can be explained as follows: When the gain offset $\lambda_p-\lambda_c$ is increased by lowering the temperature, an *increase* in gain occurs for the

38

same carrier density (Fig. 6(b)), i.e., the same gain is achieved by a *lower* carrier density. Within a certain temperature range, this effect overcomes the mismatch of gain peak and cavity mode. The threshold carrier density *decreases* despite of the fact that the tuning of the laser becomes worse at lower temperature. Only for large temperature reduction, the gain drops for $N = const$. The mismatch becomes dominant, and the threshold carrier density increases again. In other words, to maintain a given threshold gain g_{th} required for lasing, the threshold carrier density N_{th} (T) is minimum for a gain-offset towards smaller wavelength, i.e., for $\lambda_p-\lambda_c < 0$. This result is in contrast to a widely used VCL design rule saying that the gain-offset must be zero for minimum threshold current $I_{thr}(T)^{7,13}$.

We still find a deviation of measurement (minimum at -60°C) and calculation (at -30°C). This might be caused by an internal heating of the active region even in pulsed operation and/or by an additional temperature dependence of the surface leakage current. Fig. 8 shows simulated curves N_{th}(T) for different RT gain offsets $\lambda_p-\lambda_c$ that correspond to the measurements in Fig. 7. We observe a similar behaviour in the calculated curves: A change of the gain offset towards negative numbers at RT shifts the minimum of N_{th}(T) towards higher temperature but it also increases the value of this minimum. There are several reasons for the rising minimum: the gain is smaller and IVBA is larger at higher temperatures, and the DBR reflectivity becomes smaller for larger wavelength offset.
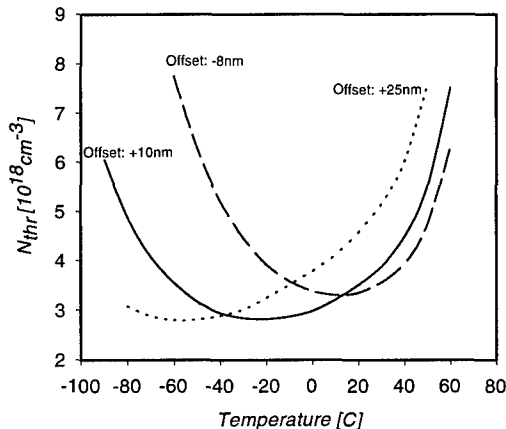
Fig. 8: Calculated threshold carrier density as function of temperature for different RT gain offset

Taking into account the results, the lowest achievable threshold current for RT is found for a match of gain and mode at RT, as expected. However, this does not mean the *minimum* of I_{thr}(T) is found at this temperature. The observed behaviour is important to design the temperature sensitivity of the VCL. For instance, minimum threshold current at RT might be reached at the expense of a stronger temperature dependence, since the slope of the curves in Fig. 9 is quite steep at this temperature. Moving the minimum to a higher temperature will increase threshold current, but reduce the temperature sensitivity of the threshold current.

VIII. Conclusion

We have fabricated 1.55μm VCL with an InP based integrated bottom mirror and a dielectric top mirror. SI-InP regrowth shows clear improvement of the characteristics. The temperature performance of the devices, in particular of the threshold current, was investigated. The experimentally observed behaviour is described well by a model based on kp band structure calculations and a transfer matrix method. The recorded I_{thr}(T) characteristics show that the minimum in temperature does not occur for perfect matching of the gain peak and the cavity mode. Therefore, the lowest threshold current for RT is not reached when the minimum is at RT. Anyway, for minimum I_{thr} at RT the gain peak has to match the cavity mode at this temperature. The model is a tool to tune the lasers for e.g. low threshold current or reduced temperature sensitivity.

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PHOTO-PUMPED OPERATION OF InGaAsP VERTICAL-CAVITY LASERS ON Si FABRICATED BY WAFER BONDING

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Introduction

Long-wavelength vertical cavity lasers have been successfully fabricated on Si substrates using wafer bonding technique. InGaAs/InGaAsP multi-quantum well active layers with 40.5-pair InGaAsP/InP stacked mirrors have been directly bonded on 3.5-pair Al_2O_3 / a-Si mirrors deposited on Si substrates. The sample has been optically pumped at room temperature and lasing operation at 1.58-μm has been achieved.

I. Background

Optical interconnections between Si LSI chips have been attracting increasing interest as a key technology to overcome an electrical interconnection problems in the LSI systems.[1] The integration of III-V optical devices on Si has been widely studied for this purpose. Especially, InGaAsP/InP vertical cavity lasers (VCLs) are very attractive light sources for vertical interconnections between stacked Si chips because Si is transparent at the lasing wavelength.

Integration of InP lasers on Si have been investigated using several approaches, including solder bonding,[2] lattice-mismatched epitaxial growth,[3] and direct wafer bonding.[4] Solder bonding with metals such as AuSn is the most straightforward method,[2] but it is not suitable for vertical interconnections between Si chips because the metals interrupt the vertical light propagation. Lattice-mismatched epitaxial growth has been widely investigated and room-temperature CW operation of the InP lasers on Si has been successfully demonstrated. However, there are some problems in this growth technique, such as high dislocation density (> 5×10^6 cm^{-2}) and high growth temperature (typically > 900 °C for thermal pre-cleaning and > 550 °C for high-quality epitaxial growth). Direct wafer bonding, in which dissimilar wafers can be bonded through hydrogen bonding between surface OH-groups [5] and/or atomic rearrangement occurring at high temperatures [6], seems to be the most promising method because the light can propagate through the bonded interface and the wafers can be bonded at low temperatures (even at room temperature) and with low dislocation density (2×10^4 cm^{-2}).[4]

Recently, we demonstrated room-temperature CW operation of InP edge-emitting lasers on Si fabricated by wafer bonding.[4] In this work, we have applied the technique to fabricate InP VCLs on Si and successfully achieved room-temperature photopumped operation.

II. Design and fabrication

Figure 1 shows the structure of the VCL. The cavity is formed by wafer bonding of an InGaAs(P)/InP epitaxial wafer to 3.5-pair Al_2O_3 / a-Si stacked mirror sputtered on a Si substrate. The InGaAs(P) / InP epitaxial wafer is grown by metalorganic vapor phase epitaxy (MOVPE) on a p-type (100) InP substrate and is composed of a 0.5-μm Zn-doped InP buffer layer, a 0.1-μm Zn-doped InGaAsP (λg = 1.3 μm) etch stop layer, a 1.1-μm Zn-doped InP cladding layer, undoped multiple quantum well (MQW) active layer, a 0.25-μm S-doped InP cladding layer, and a 40.5-pair S-doped InGaAsP (λg = 1.42 μm) / InP quarter-wavelength stacked mirror. The MQW active layer consists of 12
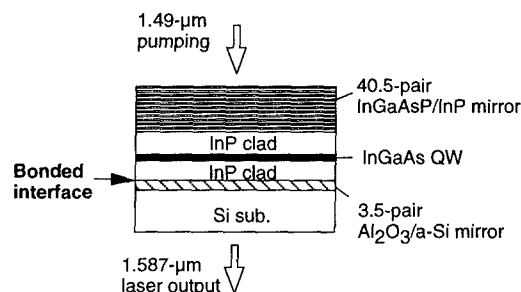
Fig. 1: Schematic structure of the long-wavelength vertical-cavity lasers fabricated on Si.

unstrained InGaAs wells (7 nm-thick) and 11 InGaAsP barriers (6 nm-thick, λgap = 1.2 μm), embedded in 38 nm-thick InGaAsP (λgap = 1.2 μm) separate confinement layers on both sides.

The fabrication process is summarized in Fig. 2. The InGaAs(P)/InP epitaxial wafer is first stuck on a glass plate with black wax for mechanical support (Fig. 2 (a)) and the InP substrate and InGaAsP etch stop layer are selectively etched away. The surface of the exposed p-InP cladding layer is then cleaned with H_2SO_4:H_2O_2:H_2O solution. The surface of the Al_2O_3 top layer in the 3.5-pair Al_2O_3 / a-Si stacked mirror is also cleaned with H_2SO_4:H_2O_2:H_2O. Immediately after rinse and spin-dry, the surfaces are placed in contact under a pressure of 4 kg/cm^2 (Fig. 2 (b)). The wafers adhered to each other after this surface contact due to hydrogen bonding between OH-groups absorbed on the cleaned surfaces. Finally, the bonded wafers are immersed in warm organic solvent to dissolve the wax completely and detach the glass plate from the wafers (Fig. 2 (c)). A SEM picture of the fabricated structure is shown in Fig. 3.

Fig. 3: A SEM picture of the fabricated structure.
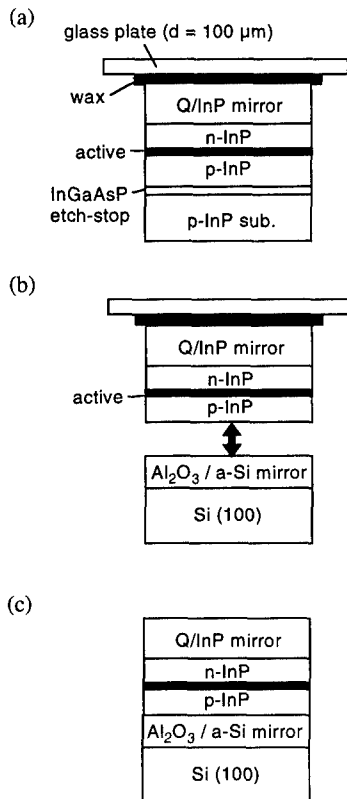
Fig. 2: Fabrication process of the VCLs.

In our previous work,[4] we heated the bonded wafers at 400 °C to improve bonding strength. In this work, however, the heat treatment caused degradation of the Al_2O_3 / a-Si mirror surface, which is probably due to thermal instability

of our sputtered a-Si. The heat treatment was, therefore, excluded from the wafer process in this work. Even without the heat treatment, the bonding was strong enough to endure the wax-dissolving process and following photopumping experiments.
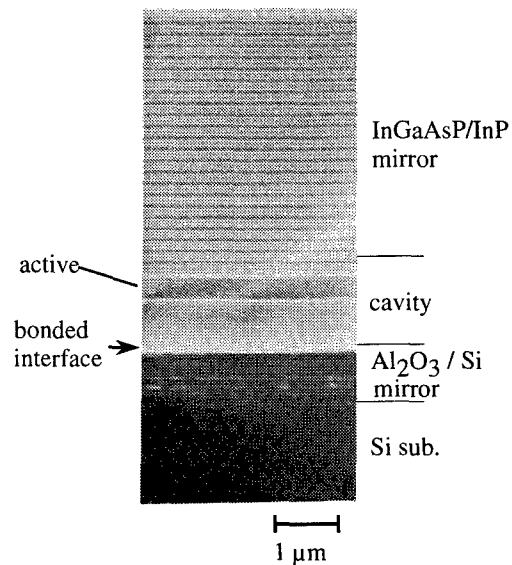
III. Characteristics

Figure 4 shows the measured reflectivity spectrum of a 40.5-pair InGaAsP/InP mirror on a InP substrate (Fig. 4 (a)) and a 3-pair Al_2O_3/a-Si mirror on a Si substrate (Fig. 4 (b)). The figure also shows the calculated spectrum with dashed curves. Material dispersion is taken into account in the calculation for the InGaAsP/InP mirror. The good agreement between the measured and calculated spectrum is indicative of the high quality of the mirrors. The reflectivity at 1.55 μm is measured to be higher than 99 % for both mirrors.

The fabricated structure was optically pumped by a 1.49-μm semiconductor laser through the 40.5-pair InGaAsP/InP mirror, as indicated in Fig. 1. The pumping laser was operated under a pulsed condition with 1-μs pulses at a repetition rate of 1 kHz. The pumping light was focused on the sample surface using a hemispherical fiber with a measured spot size of about 15 μm in diameter. Sixty percent of the pumping light was found to be reflected by the total cavity and the transmittance was almost 0 %, resulting in 40 % of the pumping light being absorbed in the cavity. Half of that is estimated to be absorbed in the InGaAsP/InP mirror, and half in the active region. The pumping efficiency is, therefore, approximately 20 %. The 1.587-μm resonant light emitted from the cavity was collected through the Si substrate and detected using a Ge photodetector with a lock-in amplifier.

Figure 5 shows light output versus input power

41

(a)

(b)
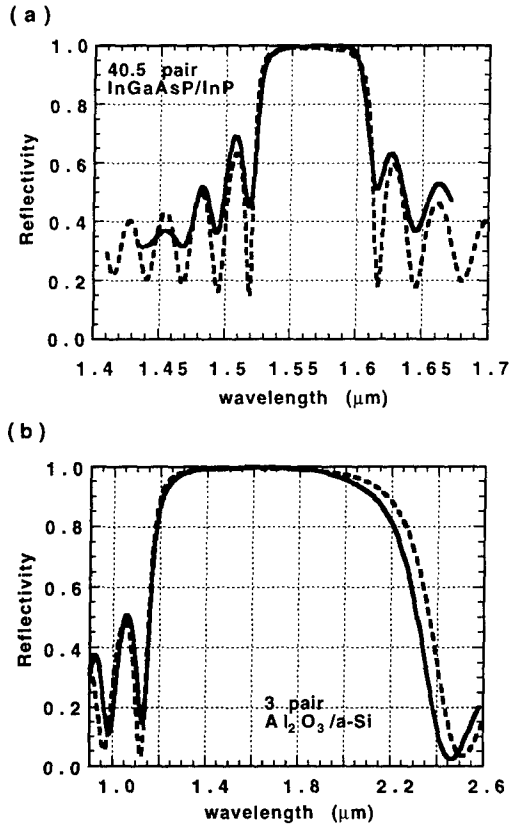
Fig. 4: Measured (solid lines) and calculated (dashed lines) reflectivity spectrum of (a) a 40.5-pair InGaAsP/InP mirror on InP and (b) a 3-pair Al_2O_3/Si mirror on Si.

Fig. 5: Output power vs. input power characteristics of the VCL under room-temperature photo-pumped operation.
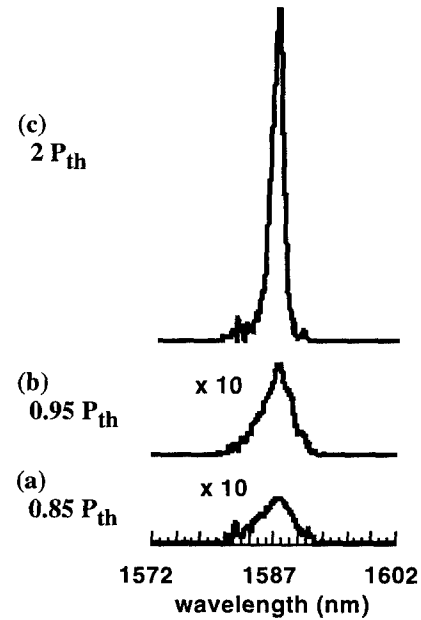
Fig. 6: The emmissin spectrum at pumping power of (a) 0.85 P_{th}, (b) 0.95 P_{th}, and (c) 2 P_th.

characteristic at room temperature. A distinct lasing threshold (Pth) is clearly observed at the input power of 14.4 mW. Polarization-resolved characteristics are also shown in the figure. Above the lasing threshold, about 90 % of the emitted light is confirmed to be linearly polarized along the (110) orientation.

The lasing wavelength is 1.587 μm and the emission spectrum at the pumping power of (a) 0.85 Pth, (b) 0.95 Pth, and (c) 2 Pth are shown in Fig. 6. Full width at half maximum (FWHM) of the spectra are (a) 4.8 nm, (b) 3.7 nm, and (c) 1.6 nm, respectively. The FWHM is reduced as the pumping power increased and reached an almost constant value of 1.6 nm above the lasing threshold. The broad spectrum above the lasing threshold can be attributed mainly to thermally induced chirping caused by instantaneous temperature rise during the pulse excitation. The multitransverse mode emission may be an additional reason for the broad spectrum..

Assuming the pumping efficiency of 20 % and diameter of 15 μm mentioned above, the threshold power density can be estimated to be 1.6 kW/cm^2, corresponding to a current density of around 2 kA/cm^2. According to a theoretical calculation,[7] this result indicates that the effective mirror

reflectivity higher than 99 % has been achieved in this VCL structure.

IV. CONCLUSIONS

In conclusion, we have fabricated 1.58-μm InGaAs(P)/ InP vertical cavity lasers on Si substrates using wafer bonding. The unstrained InGaAs/InGaAsP/InP MQW structures with 40.5 pair InGaAsP/InP mirrors have been directly bonded on 3.5-pair Al_2O_3 / Si mirrors deposited on Si substrates. The sample was optically pumped by a 1.49-μm semiconductor laser and room temperature lasing

operation has been achieved. The threshold power density has been estimated to be about 1.6 kW/cm^2, corresponding to a current density of around 2 kA/cm^2. To our knowledge, this is the first report on lasing operation of InP VCLs fabricated on Si substrates. This result shows that wafer bonding technique is a promising way to integrate InP VCLs on Si VLSIs and implement the optical interconnections in stacked VLSI systems

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LOW-THRESHOLD ALUMINIUM FREE 808 nm LASERS GROWN BY SOLID SOURCE MOLECULAR BEAM EPITAXY

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Introduction

We report on the 808 nm wavelength lasers grown by solid source molecular beam epitaxy. These tensile strained GaInP-GaInAsP single quantum well lasers exhibited a low threshold current density of 230 A/cm^2 with a cavity length of 2 mm. A 1 mm long device launched 2 W CW output power with the wallplug efficiency of nearly 50 %. The measured lasing characteristics compare favorably to those of the 808 nm lasers grown by other growth techniques.

I. Background

High power diode lasers emitting at 808 nm are widely used for Nd:YAG laser pumping. Recently, GaInAsP/GaAs lasers has attracted a notable amount of attention due their beneficial properties in comparison with conventionally used AlGaAs/GaAs lasers. Advantages of GaInAsP/GaAs system include resistance against degradation by dark-line defect formation, lower surface recombination velocity, and low mirror facet temperature.[1] Additional benefits are the absence of oxidation during growth, and the simplicity of postgrowth processing. Until now aluminium free 808 nm lasers have been grown by metal organic vapor deposition (MOCVD)[2,3] or gas source molecular beam epitaxy.[4] These growth techniques use typically highly toxic hydrides as group-V sources. Recently, all solid source molecular beam epitaxy (SSMBE) using valved cracking cells has been proved to be a viable alternative for growth of phosphorus containing materials. The state-of-the-art laser diodes have been grown by this novel toxic-gas-free growth method for a large range of emission wavelengths.[5] In this paper we report on the 808 nm laser diodes grown by SSMBE. The properties of the fabricated lasers are comparable to those obtained using other growth methods.

II. Experimental

Two independent valved cracking cells were employed to supply and regulate group-V fluxes of As$_2$ and P$_2$. These fluxes were found to be stable and reproducible as verified by growing several quaternary GaInAsP layers or laser structures with the same preset values for the valve positions. The phosphorus cell was loaded with elemental red phosphorus (7N purity) that was converted *in situ* to white phosphorus prior to growth.[6] Standard effusion cells supplied the fluxes

of gallium and indium as well as the n-type and p-type dopants, silicon and beryllium. A more detailed description of our growth system and procedures can be found elsewhere.[5,7]

For device characterization the wafers were processed into uncoated broad-area lasers using standard photolithographic methods. The cavity length ranged from 0.5 mm to 2.0 mm and the width of the stripe was 150 μm. The chips were mounted either *p*-side up with epoxy or *p*-side down with indium on submounts for testing in pulsed and CW mode, respectively.

III. Results and Discussion

The separate confinement heterostructure quantum well (SCH-QW) lasers were grown on (100) n$^+$-GaAs substrates. The structure consisted of a 2.5 μm thick *n*-type GaInP cladding, an active region, a 2.5 μm thick *p*-type GaInP cladding layer, and a 0.15 μm p$^+$-GaAs cap. The active region contained one tensile strained GaInAsP QW sandwiched between GaInAsP waveguide layers ($E_g \sim 1.8$ eV) lattice matched to GaAs. The growth parameters were optimized by preparing a series of test structures containing the similar active regions to that of the laser structure. Room temperature photoluminescence (RT-PL) was measured from these structures to evaluate the optical quality of our laser material. A typical RT-PL spectrum recorded for a 808 nm test structure is shown in Fig. 1. We grew several laser and test structures within a period of two weeks and the emission wavelength reproducibility was found to be ±3 nm using the same preset values for the valve positions of the cracking cells.

Threshold current density (J_{th}) of broad-area lasers versus cavity length is shown in Fig. 2. A low J_{th} of 230 A/cm^2 was achieved for 2 mm long devices. The inverse of total differential quantum efficiency as a function of cavity length is given in Fig. 3. The modal gain coefficient was calculated to

be 20.9 cm^{-1}, transparency current density as 165 A/cm^2, internal losses (α_i) as low as 1.96 cm^{-1} and internal quantum efficiency (η_i) to be 80 %. A characteristic temperature (T_0) of 130 K was determined from the measured light-current curves at heat sink temperatures 20 °C - 50 °C for diodes having 1 mm cavity length. The obtained values are good enough for efficient high power CW operation as demonstrated in Fig. 4. An AR/HR (10 % / 90 %) coated 1 mm long device launched about 2 W CW output power with a slope efficiency of 1 W/A and a maximum wallplug efficiency of 48 % (these measurements were limited by our measurement system and heat dissipation). The measured lasing characteristics anticipate very good performance for laser bars to be processed from this material.

The obtained results are comparable to the values typically measured for 808 nm laser diodes. We have got a threshold current density of 260 A/cm^2 (1.5 mm cavity length) using the similar laser structure grown by GSMBE.[4] Upphal et al. have reported a threshold current density of 221 A/cm^2 (2.34 mm cavity length) for MOCVD grown GaInP-GaInAsP-GaAsP tensile strained QW lasers emitting at 805 nm.[2]

Fig. 2. Threshold current density for broad area lasers versus cavity length. The solid line is a fit to the experimental data using the logarithmic gain approximation..[8]

Fig. 1. Room temperature photoluminescence spectrum from the test structure containing the similar active area to that of the grown lasers.
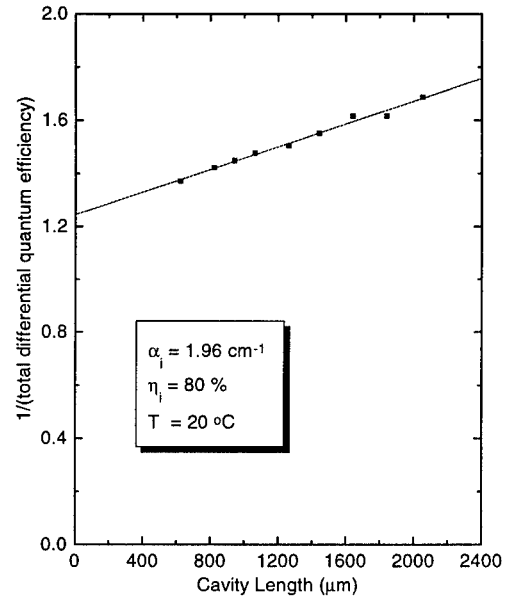
Fig. 3. Inverse of the total differential quantum efficiency as a function of cavity length for broad area lasers.

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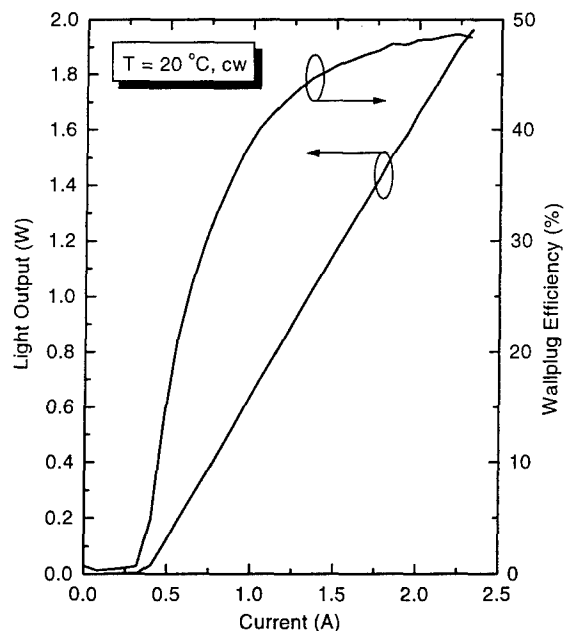
Fig. 4. CW L-I -characteristics of an AR/HR coated 808 nm tensile strained SQW laser.

IV. Conclusions

To summarize, we have grown tensile strained GaInP-GaInAsP QW lasers by SSMBE. The characteristics of the fabricated devices are comparable to those of the similar aluminium free 808 nm lasers grown by other growth methods. These results demonstrate that SSMBE is a potential alternative to MOCVD for the mass production of phosphorus based optoelectronic devices.

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Silicon doping of InP grown by MOVPE using tertiarybutylphosphine

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Abstract

Disilane has been used to grow Si-doped InP by low pressure metal organic vapour phase epitaxy (LP-MOVPE). As phosphorous precursor we used tertiarybutylphosphine (TBP) and phosphine (PH_3) for comparison. Trimethylindium (TMIn) was the In source. The dependence of carrier concentration on substrate temperature, V/III ratio and reactor pressure was investigated. The Si concentration was proportional to the ratio of molar fraction of disilane to TMIn independent on the used group V precursors. The doping efficiency using TBP was much higher than using PH_3. The Si incorporation increases slightly with increasing V/III ratio independent on the group-V source. Also the electron concentration increases with increasing reactor pressure. Apparent activation energies of 1.4 eV, 1.6 eV and 1.8 eV were observed at reactor pressures of 100, 40 and 20 hPa for growth temperatures between 823 K and 883 K. Si incorporation mechanisms, which may explain the experimental results, will be discussed.

I. Introduction

N-type InP is an important material for electronic device application. In the literature many reports on silicon doping of GaAs can be found (1-9), but only few reports for silicon incorporation in InP are available (10, 11). To our knowledge there is no report about n-type doping of InP with disilane using tertiarybutylphosphine (TBP).

The group-V hydrides arsine (AsH_3) and phosphine (PH_3) are still commonly used as precursors for the growth of III-V-compound semiconductors. One advantage the MOVPE offers in contrast to the molecular beam epitaxy (MBE) is the capability of large scale production. Here the hazardous standard gases cause a big problem for the process safety. Beside, the thermal stability of the hydrides (especially phosphine) make the consumption of source material inefficient. This causes a large amount of toxic residual gases, which have to be removed in the scrubber unit. The disposal of the toxic waste, which arises as a result is an unneglectable cost factor in industrial production. Therefore there is a strong interest to replace those precursors. In recent years the low pressure and less toxic liquids TBAs and TBP gained acceptance as substitutions for arsine and phosphine. Many reports show that beside the increased safety of the MOVPE process the alternative sources allow to reduce the growth temperature and the group-V consumption considerably. In first studies we have demonstrated the qualification of TBP for the growth of high quality undoped InP (μ_{77K} = 57000 cm^2/Vs, $(N_D-N_A)_{77K}$ = 7.7·10^{14} cm^{-3}). We also used TBP successfully for selective epitaxy and regrowth experiments (12).

In this work we discuss in detail the disilane (Si_2H_6) doping of InP using TBP. The dependence of the carrier concentration on gas phase mole ratio of disilane to TMIn, the substrate temperature, reactor pressure and V/III ratio was studied. PH_3 was used for comparison.

II. Experimental

Growth was carried out in a horizontal low pressure MOVPE system. Pd-diffused hydrogen with a total flow rate of 3.6 l/min or 6.8 l/min served as carrier gas. Trimethylindium (TMIn), TBP and PH_3 were used as source materials. N-type doping was accomplished using disilane (100 ppm in H_2). The graphite susceptor was heated by means of five quartz halogen lamps. The substrate temperature varied from 823 K to 933 K. Growth rate was about 2.0 μm/h. Substrates were semiinsulating Fe-doped (001) exactly orientated InP wafers. They were cleaned in organic solutions, deionized water, etched in H_2SO_4:H_2O_2:H_2O (3:1:1), and HF (4%). Immediately after cleaning, the substrates were transferred into the reactor.

The surface morphology was observed by phase-contrast optical microscopy and scanning electron microscopy (SEM). Hall effect measurements of uniformly doped epilayers were carried out using the van der Pauw method. In order to clarify the influence of growth conditions on silicon incorporation, epilayers with a multilayer structure were grown by varying either the gas phase mole ratio of disilane to TMIn, the substrate temperature, or the V/III ratio while keeping other parameters unchanged. Carrier concentration of those epilayers was measured by electrochemical C-V depth profiling. The etched

depth was corrected by measuring the depth using a mechanical profiler.

III. Results and discussion

The surface morphology of all InP layers using PH_3 was smooth. It is known that the growth temperature window to achieve good surface morphology using TBP at low V/III ratios is very small (13). Therefore the samples grown with TBP at temperatures higher than 883 K became rough. Thus the high V/III ratio of 40 was used for higher growth temperatures.
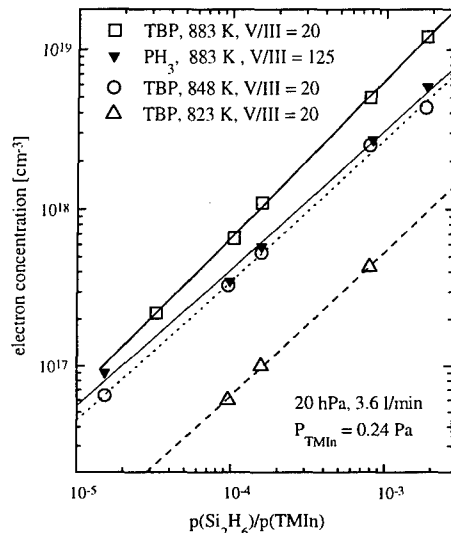
Fig. 1: Dependence of carrier concentration on the ratio of gas phase molar fraction of disilane to TMIn for T_G = 823 K, 848 K and 883 K using TBP and 883 K using PH_3.

The dependence of the donor concentration on the ratio of gas phase molar fraction of disilane to TMIn is shown in Fig. 1. The reactor pressure was 20 hPa and the total carrier gas flow 3.6 l/min. The lines are apparent linear fittings to the experimental results. The linear relationship does not change with the substrate temperature, V/III ratio, reactor pressure or group V sources. This character is a common feature of silicon doping, and is also observed in GaAs and InGaAs [6, 14].

The efficiency of silicon doping can be described by using the distribution coefficient, which is defined as the ratio of gas phase and solid phase atomic concentrations of silicon normalized to TMIn atomic concentrations in the gas and solid phases, respectively. Using TBP with V/III = 20, the distribution coefficient increases with increasing growth temperature from 0.03 at 823 K to 0.32 at 883 K. The coefficient using PH_3 at 883 K with V/III = 125 is 0.17. With the growth parameters used in fig. 1 the silicon doping efficiency is about two times higher using TBP instead of phosphine at the same substrate temperature.

Fig. 2 demonstrates the dependence of the 300 K Hall mobility on the carrier concentration. The solid lines are

theoretical mobilities for different compensation ratios $\theta = N_A/N_D$ from Walukiewicz et. al. (15). The experimental data for TBP and PH_3 show no significant difference in the compensation ratio. Apart from one phosphine sample the compensation ratio for all others is equal or less than 0.4. The total values are slightly lower than those reported by A. R. Clawson et. al. (10) who used PH_3 and SiH_4. They found ratios between 0.4 and 0.6. The good agreement for the compensation ratios using TBP and PH_3 indicates that the higher (N_D - N_A) concentrations using TBP are really caused by a higher Si incorporation.
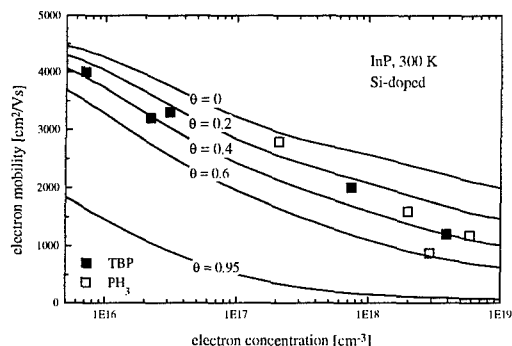
Fig. 2: Dependence of 300 K Hall mobility on the electron concentration. The solid lines are theoretical mobilities for different acceptor/donor compensation ratios from Walukiewicz et. al. (10)
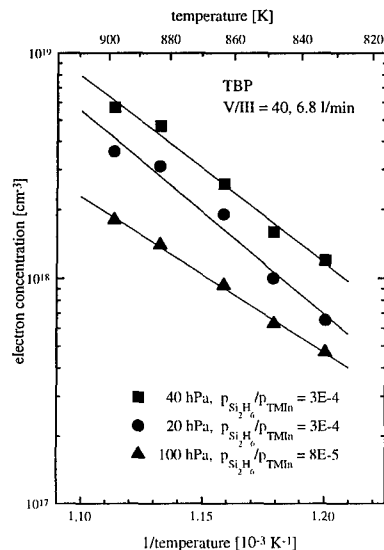
Fig. 3: Dependence of electron concentration on substrate temperature for reactor pressures of 20 hPa, 40 hPa and 100 hPa.

In fig. 3 the dependence of electron concentration on substrate temperature is plotted for reactor pressures of 20 hPa, 40 hPa and 100 hPa. The V/III ratio was kept constant at 40. The total carrier gas flow was 6.8 l/min. The ratio of molar fraction of disilane to TMIn was $3 \cdot 10^{-4}$ at the reactor pressures of

20 hPa and 40 hPa and $8 \cdot 10^{-5}$ at 100 hPa. The electron concentration increases with increasing growth temperature and reactor pressure. At a reactor pressure of 100 hPa, the distribution coefficient increases from 0.3 to 1.1 if the substrate temperature increases from 833 K to 898 K. At a reactor pressure of 20 hPa it changes from 0.1 to 0.3. If the reactor pressure increases from 20 hPa to 100 hPa, the doping efficiency increases by a factor of 1.9 at 898 K and by a factor of 3 at 833 K. The difference increases in the low temperature region. Apparent activation energies estimated from the slopes in fig. 3 are 1.8 eV, 1.6 eV and 1.4 eV for reactor pressures of 20 hPa, 40 hPa and 100 hPa, respectively. We have found comparable apparent activation energies for the disilane doping of InGaAs using TMIn, TMGa or TEGa and TBAs (14) and also several authors (3, 7, 16) reported values in this range for the Si-doping of GaAs with standard precursors. Rose et. al.(11) reported that in atmospheric pressure MOVPE grown Si:InP using disilane and phosphine the electron concentration is nearly independent of substrate temperature between 873 K and 973 K. The strong dependence of carrier concentration on substrate temperature and reactor pressure in our experiments indicates that at low reactor pressure in the used temperature region the disilane is not completely decomposed. That is why the cracking efficiency of disilane can be increased by increasing growth temperature or reactor pressure. If this assumption is true the dependence of electron concentration on substrate temperature should become weaker for high growth temperatures and should saturate finally.
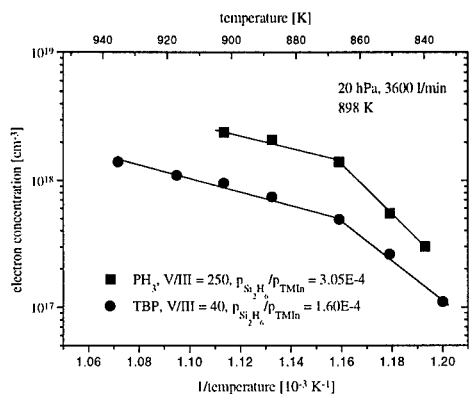
Fig. 4: Dependence of the electron concentration on substrate temperature for TBP and PH$_3$, respectively.

As shown in fig. 4, this is really the case. The dependence of the electron concentration on substrate temperature for TBP and PH$_3$ is plotted. Using TBP and PH$_3$ the ratios of Si$_2$H$_6$/TMIn were $3.05 \cdot 10^{-4}$ and $1.60 \cdot 10^{-4}$, respectively. The V/III ratios were 40 (TBP) and 250 (PH$_3$). In addition to fig. 3 the temperature variation included values up to 933 K. Independent of the used group-V source the donor concentration nearly saturate above 883 K. Also, J. M. Redwing et. al.(1) have found that for n-type doping of GaAs with disilane the donor concentration is substrate temperature dependent up to 923 K and saturates above this temperature. The doping efficiency is nearly equal using TBP and PH$_3$ with the growth parameters shown in fig. 4. The explanation for this behaviour is the high V/III ratio of 250

using PH$_3$. As shown in Fig. 5 the doping efficiency depends not only on growth temperature and reactor pressure but also on V/III ratio. The ratio of Si$_2$H$_6$/TMIn was kept constant at $1.58 \cdot 10^{-4}$. The reactor pressure was 20 hPa. The bottom axis shows the V/III ratio for the use of PH$_3$ and the corresponding top axis the values for TBP. At a substrate temperature of 883 K the doping efficiency increases slightly with increasing V/III ratio for TBP. The same dependence results if PH$_3$ is used at 863 K and 913 K, respectively. For a substrate temperature of 913 K it is not possible to achieve epilayers with smooth surfaces using TBP with normally used V/III ratios. Therefore we cut out this experiment. In the whole range of V/III variations, the doping efficiency using TBP at 883 K is higher than that using PH$_3$ in defiance of the high substrate temperature of 913 K. The comparison for normally used V/III ratios of 15 (TBP) and 150 (PH$_3$) results in distribution coefficients of 0.61, 0.33 and 0.10 for TBP at 883 K, and PH3 at 913 K and 863 K, respectively.
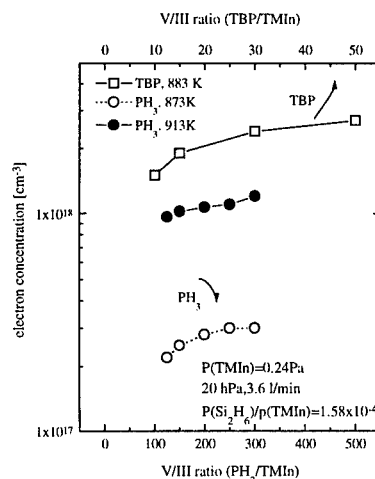
Fig. 5: Dependence of electron concentration on V/III ratio using PH$_3$ at 883 K and 913 K (bottom X-axis), and using TBP at 883 K (top X-axis).

The main results of our experiments will be discussed now. The dissociation of disilane proceeds in two steps (A) and (B) (17, 18) as described below:

$$Si_2H_6 \rightarrow SiH_2 + SiH_4 \qquad (A)$$
$$SiH_4 \rightarrow SiH_2 + H_2 \qquad (B)$$
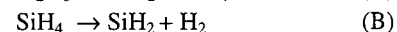
Reaction (A) starts at 753 K (1). But in the temperature range below 973 K the decomposition efficiency of SiH$_4$ (B) is very small (1,9). One possible doping mechanism is the gas phase formation of SiH$_2$ and its subsequent diffusion to the growing surface followed by incorporation. From the temperature dependence of donor concentration at 20 hPa reactor pressure which is shown in fig. 4 we can determine two different temperature regions for the disilane doping using TBP and phosphine, respectively. Above 883 K the donor concentration is nearly independent of the substrate temperature. In this region the disilane is almost completely decomposed to SiH$_2$ and SiH$_4$ and the doping is mass transport limited. The slight

increase with increasing growth temperature can be explained by the low dissociation rate of SiH_4. Below 883 K the strong temperature dependence shows that Si doping is controlled by kinetic processes. One is the decomposition of disilane itself, but the reaction (A) should be complete at about 853 K. Therefore we assume another inhomogeneous reaction. In analogy to the disilane doping of GaAs and InGaAs (1, 3, 14, 21), we propose the formation of monosilylphosphine (SiH_3PH_2) near the growing surface during decomposition of disilane in presence of TBP and PH_3 followed by adsorption and the final incorporation into the epilayer. The assumed reaction is:

$$PH_3 + SiH_2 \leftrightarrow SiH_3PH_2. \qquad (C)$$

Fritz (19) reported about the formation of SiH_3PH_2 by the pyrolysis of a mixture of SiH_4 and PH_3. Blazejowski and Lampe (20) observed, that the reaction rate to form SiH_3PH_2 is equal to the SiH_2 supply. As well as the SiH_3AsH_2 the SiH_3PH_2 should be thermally unstable, too. A quantity of monosilylarsine could be detected up to 873 K (1). Reaction (C) depends on the group V supply, which explains the dependence of donor concentration on V/III ratio.

Because of the kinetic processes we observed a higher influence of the reactor pressure on the doping efficiency at lower substrate temperatures than at higher ones. For the reactor pressure of 100 hPa and $T_G = 898$ K we observed a distribution coefficient higher than one. This can be explained as follows: At our growth temperatures SiH_2 should be produced only by reaction (A). Therefore we took only one Si-atom per molecule for the calculation of the distribution coefficient into account. We assume, that the high reactor pressure enhanced the decomposition rate of SiH_4 and therefore more than one Si-atom per disilane molecule can be incorporated. In addition the high pressure reduces the gas velocity and so enhances the reaction time. This will produce more SiH_3PH_2 and the Si incorporation consequently increases with increasing reactor pressure.

IV. Conclusion

In this work we have investigated the disilane doping of InP using TBP as phosphorous source. Phosphine was used for comparison. We have shown that the donor concentration has a desired linear dependence on the ratio of molar fraction of disilane to TMIn independent of the used group V precursors. Also the doping efficiency depends on substrate temperature and V/III ratio. Below about 883 K the doping was dominated by kinetic reactions. We proposed that the Si doping in this temperature region occurs by means of gas phase formation of SiH_2 and its subsequent diffusion to the growing surface followed by incorporation and in addition by the formation of SiH_3PH_2 near the growing surface followed by adsorption and the finally incorporation. Above the growth temperature of 883 K the Si doping is mainly mass transport limited. The Si-doping efficiency using TBP at typical growth parameters was much higher compared to the use of PH_3, but the total value was strongly dependent on the growth parameters like substrate temperature, reactor pressure and V/III ratio. Electron concentrations up to $1.2 \cdot 10^{19}$ cm^{-3} could be achieved.

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SUPPRESSION OF INTERDIFFUSION OF Fe AND Zn IN InP:Fe/InP:Zn STRUCTURES

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Introduction

Fe in Semi-insulating (SI) InP:Fe has a low thermal stability when it is grown adjacent to p-InP:Zn. This report investigates the possibility to use S-codoping of the SI material to suppress the interdiffusion of Fe and Zn. At a sulphur codoping concentration of $5x10^{17}$ cm^{-3} no interdiffusion occured and the material had a resistivity of 10^7 Ωcm, as indicated by SIMS- and I-V analysis of n/SI/n and n/SI/p structures. These results show that S codoping of SI-InP can be used to suppress the interdiffusion of Fe and Zn while still maintaining the SI properties of the material.

I. Background

Fe doped InP is an important high resistivity semi-insulating (SI) material used for electronic and optoelectronic applications. By using SI-InP as substrates or epitaxial layers one can achieve current confinement, integration and minimisation of parasitic capacitance. It is a well known fact that Fe in InP has a low thermal stability when SI-InP is grown adjacent to p-type material [1,2]. The interdiffusion of Fe and p-type dopants can deteriorate the sharpness of the dopant profile at the interface and thereby the quality of the device. To ensure a high performing, long living device this interdiffusion must be suppressed. An n-type blocking layer between SI-InP and p-type InP has been attempted successfully [3], but is not suitable for all kinds of applications. Codoping of the SI-InP with Ti or S has also been used. In contrast to the case of Ti [4] codoping with S [3] has not yet been shown to give a SI material.
In this report the possibility to supress the interdiffusion by S-codoping is further investigated by SIMS- and I-V analysis of n-InP:S/SI-InP:Fe:S/n-InP:S and n-InP:S/SI-InP:Fe:S/p-InP:Zn structures.

II. Experimental

A HVPE system [5] was used to prepare six n/SI/n and six n/SI/p structures with various amounts of S but constant amount of Fe in the SI layer. The twelve structures were grown at 958K and 1 atm by depositing a 2 μm thick iron and sulphur codoped InP layer on sulphur or zinc doped InP substrates (n = $3x10^{18}$ cm^{-3}, p = $5x10^{18}$ cm^{-3}) followed by a 1 μm sulphur doped InP top layer (n = $4x10^{18}$ cm^{-3}). InCl, PH$_3$,

H$_2$S and FeCl$_2$ were used for the deposition in an ambient of nitrogen. Eight of the grown samples were annealed at 973K for 30 minutes in an PH$_3$ ambience. All the samples are enumerated in Table 1 with their respective codoping concentrations. The Fe , Zn and S concentration profiles were studied by SIMS using a Cameca IMS 4f with Cs$^+$ (Zn, Fe and S) and O$_2^+$ (Fe) as ion sources. To measure the I-V characteristics, ohmic contacts were made on circularly etched mesas of diameter 1150 μm formed by conventional lithography and wet etching. The wet etchant consisted of hydrogen peroxide, hydrogen bromide and water in the ratio of 1:1:10. The ohmic contacts used were AuGe/Ni/Ti/Pt/Au for n-InP.

Table 1. Fe and S concentrations used in the codoped semi-insulating layer.

Sample	Structure	Annealed	Fe (cm^{-3})	S (cm^{-3})
1	n/SI/n	no	$2*10^{18}$	$<10^{15}$
2	"	yes	"	$7*10^{16}$
3	"	no	"	$2*10^{17}$
4	"	no	"	$5*10^{17}$
5	"	yes	"	$9*10^{17}$
6	"	no	"	$3*10^{18}$
7	n/SI/p	yes	"	$<10^{15}$
8	"	yes	"	$7*10^{16}$
9	"	yes	"	$2*10^{17}$
10	"	yes	"	$5*10^{17}$
11	"	yes	"	$9*10^{17}$
12	"	yes	"	$3*10^{18}$
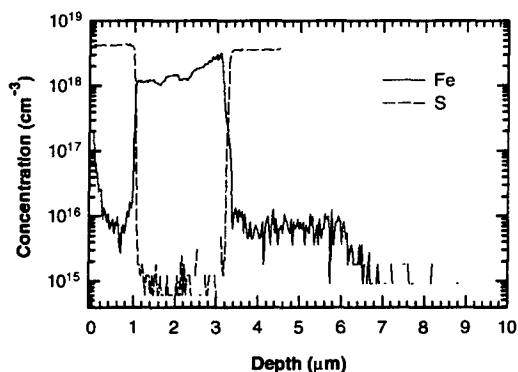
Figure 1. SIMS-profile showing the Fe and S codoping concentrations in sample 1. The S doping in this case was unintentional

Figure 2. SIMS-profile showing the Fe and S codoping concentrations in sample 4. The S doping in this case was $5*10^{17}$ cm^{-3}.

III. Results and discussion

A. SIMS (n/SI/p)

To study the diffusion SIMS profiles were analysed for every sample. In Fig. 1 and 2 the SIMS results are shown for the n-type substrate samples 1 and 4. The Fe and S diffusion in samples 1-6 before and after annealing is almost negligible. There seems to be a small diffusion front of Fe reaching about 3μm into the substrate. But this low concentration diffusion ($\sim10^{16}$ cm^{-3}) is independent of both S codoping and heat treatment indicating a small but constant amount of movable Fe interstitials in the SI layer.

In the samples with low S codoping concentration one can see an accumulation of iron towards the substrate interface. This phenomenon has been explained to be caused by FeP percipitates [6-7]. When the S concentration is increased the accumulation dissappears which can be interpreted as an

increase in Fe solubility even beyond the interface. The favourable effect of S on the Fe solubility has also been observed when Fe has been ionimplanted into S doped InP substrates [8].

B. SIMS (n/SI/p)

The Fe and Zn SIMS profiles for the p-type substrate samples 7 and 10, shown in Fig. 3 and 4, were measured simultanously using a Cs$^+$ source. In sample 7, where no intentional codoping was used, the interdiffusion is considerable. Almost all Fe has diffused into the substrate and a lot of Zn has diffused into the SI layer. Increasing the S codoping results in less diffusion and at a S concentration of 5×10^{17} cm^{-3} (sample 10) the interdiffusion is stopped. Comparing SIMS results of samples with low S codoping before and after annealing shows that the diffusion continues during the annealing step. This is also the case in the highly
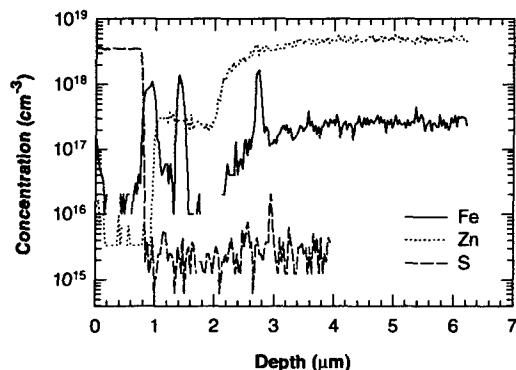
Figure 3. SIMS-profile showing the Fe, Zn and S codoping concentrations in sample 7 before the annealing step. The S doping in this case was unintentional .
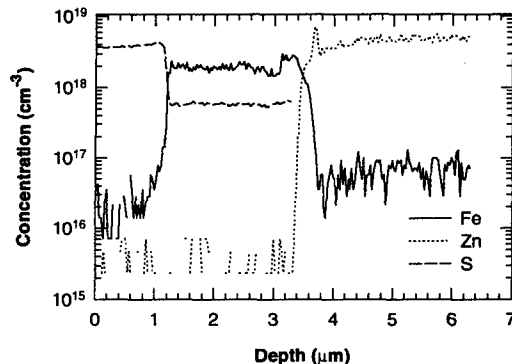
Figure 4. SIMS-profile showing the Fe, Zn and S codoping concentrations in sample 10 before the annealing step. The S doping in this case was $5*10^{17}$ cm^{-3}

52
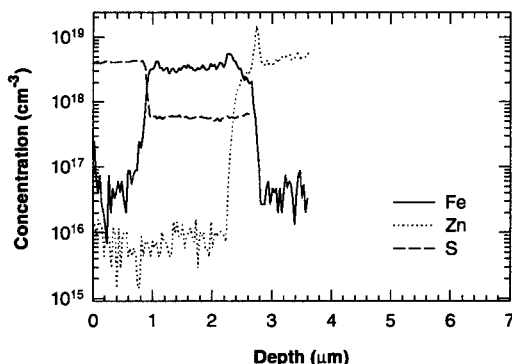
Figure 5. SIMS-profile of sample 10 after annealing.

Figure 6. SIMS-profile of sample 8 showing a typical Fe-Zn interdiffusion behaviour.

codoped samples but to a much lesser extent as can be seen in Fig. 5. The disparity in layer thickness of sample 10 between Fig. 4 and Fig. 5 is due to thickness uniformity.

Both Fe and Zn diffuse in InP according to the interstitial-substitutional diffusion model [9]. This means that only the interstitials are mobile and the "kickout" mechanism can be used to explain the interdiffusion [3,4,10]. This mechanism, in wich Zn diffuses into the SI layer and "kicks" Fe out of its substitutional site, can be described as:

$$Zn_i + Fe^-_{In} = Zn^-_{In} + Fe_i \qquad (1)$$

Since this reaction is reversible (Fe that becomes interstitial can diffuse into Zn rich areas and "kick" out substitutional Zn) a steep concentration gradient of Fe and Zn interstitials is maintained leading to a fast diffusion. The SIMS profiles for the samples with low S codoping is consistent with this mechanism. In sample 8, depicted in Fig. 6, the Fe profile

"follows" the Zn level as expected when an equilibrium like (1) prevails. Whenever a Zn atom replaces an Fe atom at a substitutional site there is a hole transfer from Zn to Fe. The explanation for the ability of S to supress the diffusion is that S can compensate these holes before the "kickout" takes place.

C. I-V

The results from the I-V measurements is depicted in Fig 7 and shows that the resistivity decreases with increasing S concentration. This is because codoping with S leads to a lowering of the active iron concentration by compensation. In sample 5 and 6 the compensation has gone so far that no active iron is left in the material. The differential resistivity in sample 4 (with S codoping concentration corresponding to sample 10) is about 10^7 Ωcm, i.e. it is still semi-insulating. This means that the solubility of iron (at substitutional sites) in sample 4 must be at least as high as the sulphur concentration of 5×10^{17} cm^{-3}. This is a very high value since earlier reports of iron solubility has been below 10^{17} cm^{-3}.

IV. Conclusion

Our results show that codoping of SI-InP with Fe and S is a possible way to effectively supress the interdiffusion of Fe and Zn between SI-InP and Zn doped eptaxial layers. This can be done without loosing the SI qualities of the material if the S codoping concentration is carefully chosen.

V. Acknowledgments
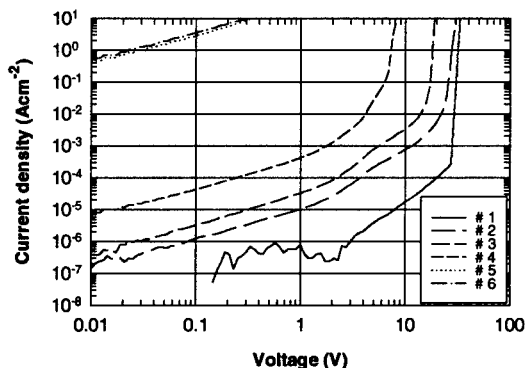
Figure 7. I-V measurements of the six n/SI/n samples.

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Fe DISTRIBUTION AROUND HYDRIDE VPE InP:Fe REGROWN LASER STRIPES

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In the Hydride VPE mesa stripe structures are regrown in a lateral growth mode exceeding the normal planar growth rate by more than an order of magnitude depending on the stripe orientation. During the embedding of mesas with InP:Fe a dilution of the Fe dopant due to the raised growth velocity in the vicinity of the original stripe might occur. An insufficient Fe level may effect the loss of the required semi-insulating character. Thus, we analyzed regrown mesa structures with < 011 > and < 01-1 > orientation by SIMS. A moderate dilution of the Fe dopant down to ~30 % was found for lateral growth zones with an increase in growth rate up to a factor of 35. Therefore, our data indicate that the attractive advantages of the rapid lateral regrowth can be used without changing the conventional doping conditions.

I. Introduction

The Hydride VPE is an outstanding tool for selective InP:Fe regrowth over structured surfaces in device production. Semi-insulating InP is a prerequisite for optoelectronic device integration as well as for high-speed single components like lasers and receivers to avoid hybrid techniques based on the use of polyimide. Especially for high-speed lasers, InP:Fe is indispensable for low parasitics and thermal conductivity reasons.

When regrowing ridge-stripe laser structures, a rapid sidewall coverage and a rapid planarizing lateral broadening of the original mesa stripe is generally observed.[1] The velocity of this high lateral growth speed depends on the crystal orientation and exceeds the planar growth rate in our experiments by factors up to about 35. If the Fe concentration, being typically 2×10^{18} cm^{-3} for planar growth, is diluted by higher growth rates, the semi-insulating character of the deposited InP:Fe may disappear and consequently deteriorate the device characteristics. Therefore, we analysed the Fe concentrations of differently oriented regrown mesa stripes by SIMS.

II. Experimental

To achieve transferable results, two mesa stripe samples were prepared in the same way as our laser samples. The striped mesas were defined parallel to either the < 011 > or the < 01-1 > direction on exactly oriented (100) n-InP:S substrates by dry etching using 7 μm wide Si$_3$N$_4$ / Ti etch masks. The mesas are 4.3 μm in height with a slope angle of ~15° and the ridges are spaced equidistantly 500 μm apart. After removing the Ti layer, both samples were given a standard H$_2$SO$_4$ treatment and immediately afterwards loaded to the VPE reactor together with a planar n-InP:S substrate sample (orientation (100), 2° off). The selective VPE regrowth was performed at 655°C for 5 min in N$_2$

ambient at atmospheric pressure. For more experimental details see Göbel and Janning.[2] The SIMS analysis of the Fe dopant was carried out with a Cameca IMS4F equipment using Cs$^+$ as primary ions at 10 kV and a beam width of about 8 μm. The Si$_3$N$_4$ was left on the mesa sample during the SIMS experiments. The sputter area was always 125 μm x 125 μm and the sputtered layer thickness per cycle about 50 nm. To detect the iron of the epitaxial material, FeP$^-$ was chosen as the secondary ion and calibrated with an implant standard whereas the S intensity is merely qualitative. In this way Fe concentration data of the whole SIMS crater volume were obtained, but only smaller parts were used for different evaluations, e.g. a volume just in a laterally regrown mesa shoulder. SIMS analyses were performed of the regrown mesas, of the areas in between them and of the unstructured substrate sample.

III. Results and discussion

The VPE regrowth resulted after 5 minutes in a lateral broadening of the original mesas of 30 and 60 μm on each side for the < 011 > and < 01-1 > orientations, respectively. The corresponding lateral growth rates, simply defined as the velocity of the mesa plateau edges, amount to 360 and 720 μm h^{-1}. Despite this significant broadening of the stripes, the planarity of the regrown mesas is better than 200 nm (!) over the whole smooth plateau. This structure represents an excellent basis for subsequent device processing. Between these laterally regrown mesas, zones of planar growth reveal a rough surface which is the typical 3-dim hillock formation for VPE deposition on exactly oriented substrates. SIMS data of a depth profile from a 42 μm x 42 μm area in this planar growth zone are illustrated in Fig.1. The simultaneous increase of the qualitative S signal and decrease of the quantitative Fe concentration indicate an epitaxial layer thickness of about 1.5 μm and a planar growth rate of ~ 20 μm h^{-1} which is, however, not very well defined due the rough surface. The Fe level of
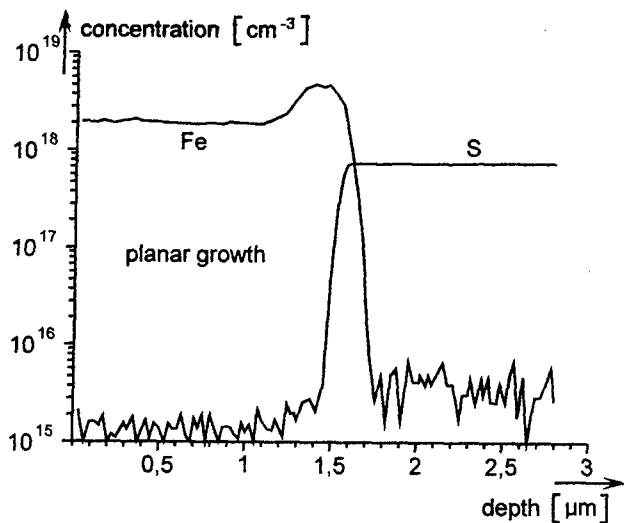
Fig. 1. SIMS depth profile of a planar growth zone ($r_{plan} \approx$ 20 μm h^{-1}; Fe conc. quantitative, S conc. qualitative).

$2x10^{18}$ cm^{-3} is quite constant except for a typical interface enrichment. The same Fe concentration and growth rate was determined for planar growth on the unstructured substrate sample revealing a mirrorlike surface morphology as a result of the misorientation. Fig. 2 shows the depth
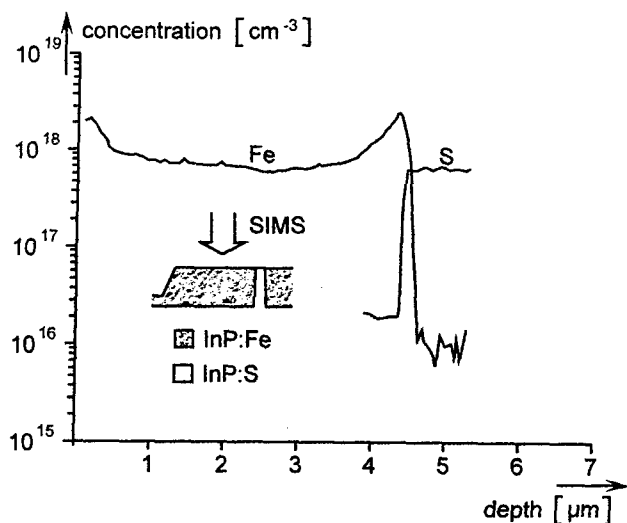
Fig.2. SIMS depth profile through a lateral growth zone (r_{lat} = 720 μm h^{-1}).

profile through the laterally regrown part of the < 01-1 > mesa sample using also a 42 μm x 42 μm area for the evaluation which does not overlap with either the original mesa or the planar growth zone. The epitaxial layer thickness corresponds to the 4.3 μm height of the original mesa pointing to the excellent planarity. The Fe signal in this laterally grown material is as constant as in the planar sample (Fig. 1). Interface enrichments are also present. From this SIMS analysis S and Fe intensity distributions of a cross section through the whole structure are illustrated in
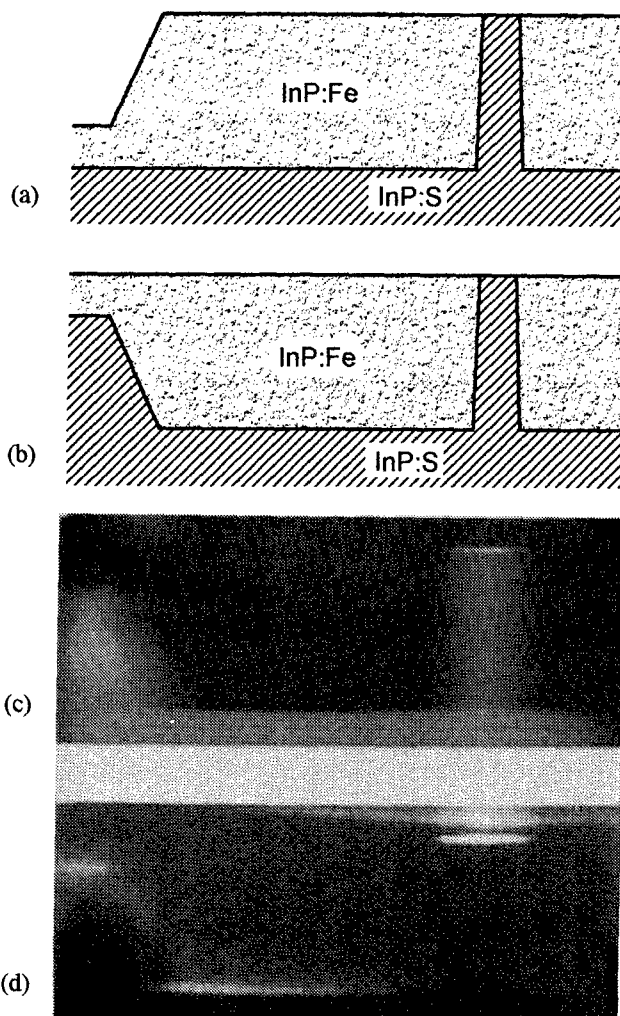
Fig. 3. Schematic of a regrown mesa structure (a) and its presentation for the levelling SIMS analysis (b); S and Fe intensity distribution, (c) and (d) respectively. Contrast enhanced by image processing. Lateral dimension 125 μm.

Figs. 3(c) and 3(d) and explanatory schematics to this in 3(a) and 3(b). From the shape of the originally etched mesa in the S distribution picture one can estimate the lateral resolution which is about a few microns. The Fe is homogeneously distributed in the whole lateral growth zone, that means the dopant level is constant not only in the vertical direction, as already known from Fig. 2, but also constant in the direction of the high lateral growth. Interface enrichments are recognizable in the lateral and planar growth regimes, as well. Since the Si$_3$N$_4$ interferes under our experimental conditions mass spectroscopically with the FeP, the strong signal on top of the mesa (Fig. 3(d)) can be attributed to the sputtering of the mask material.

In Fig. 4 the Fe levels of all SIMS analyses are plotted versus the corresponding growth rates. The Fe is diluted by the increasing growth. The measured levels vary from 0.6 to $2x10^{18}$ cm^{-3} for regions with growth rates between 720 and 20 μm h^{-1}. However, even the lowest Fe level can still bring about the semi-insulating character of the deposited
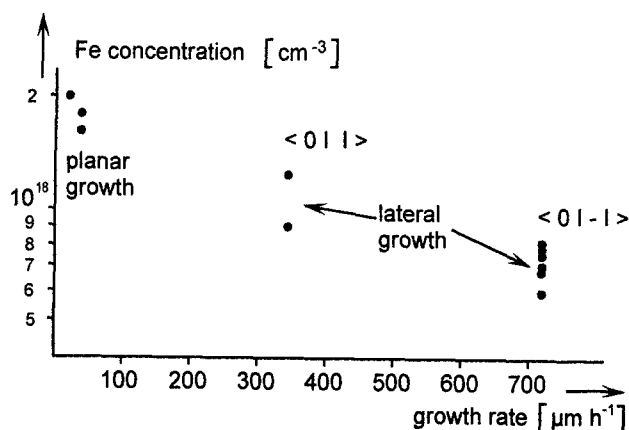
Fig. 4. Total Fe concentrations as analyzed by SIMS versus growth rates of different growth mechanisms. The "planar growth" data refer to growth on unstructured substrates and on planar growth on mesa stripe structures, as well. For the "lateral growth" the stripe orientations are given.

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InP with resistivities in the order of 10^8 Ω cm. This was verified by I-V measurements just for planar growth. This result can, strictly speaking, only be transferred to the laterally deposited material if the activation of the Fe therein is not substantially lower. The SIMS analysis cannot answer this question since it detects the total Fe and does not distinguish between the substitutionally incorporated and the interstitial dopant. The latter was found to be bound in orthorhombic FeP precipitates which are supposed to be electrically and optically passive.[3] Another restriction is the limited lateral resolution of our SIMS measurements. This is why we obtained no detailed Fe data from the closest vicinity (~<1 μm) of the original mesa which is most sensitive to leakage currents. But even if this problem can be overcome by a sophisticated SIMS technique, one is still confronted with the question of the Fe activation. Nevertheless, our SIMS experiments clearly reveal a merely moderate dilution of the Fe dopant by the very high lateral growth rate.

IV. Conclusion

In this paper, we have measured the Fe dopant levels by SIMS in the vicinity of mesa stripes laterally regrown by hydride VPE InP:Fe with extreme growth rates up to 720 μm h^{-1}. In all samples the Fe was found to be homogeneously distributed except for typical interface enrichments. The Fe doping level of 2×10^{18} cm^{-3}, typically used for normal planar growth at deposition rates of 20 μm h^{-1}, is decreased by the rapid lateral regrowth to ~1×10^{18} and 6×10^{17} cm^{-3} for mesa stripe orientations of < 011 > and < 01-1 >, respectively. This moderate dilution still maintains Fe concentrations which are supposed to bring about the required semi-insulating character of the embedding material.

Ultrahigh-Speed InGaP/AlGaAs/InGaAs HBTs Using Mg as the Base Dopant

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Abstract

We have fabricated ultrahigh-speed InGaP/AlGaAs/InGaAs graded-base hetero-bipolar transistors (HBTs), which employ Mg as the base-region p-type dopant.   In addition, the dead region under the base metal contact layer has been etched away.   Even with a HBT base layer as thick as 60nm, we obtained excellent frequency characteristics of the short-circuit current-gain frequency ft and the maximum frequency of oscillation fmax as high as approximately 140 GHz and 230 GHz, respectively.

We obtained maximum toggle frequency of 22.5GHz and direct oscillation frequency of 80GHz for the static frequency divider and   the base common transistor oscillator, respectively, by using the 4-inch full process of InGaP/AlGaAs/InGaAs graded-base HBT .

I . Introduction

In a previous paper, we reported that an AlGaAs/GaAs HBT and an InAlAs/InGaAs HBT with excellent frequency characteristics can be fabricated using Mg as the p-type dopant in the base region[1].   We have conducted further research to greatly enhance the switching speed of the InGaP/AlGaAs/GaAs HBT again using Mg as the dopant. In this paper, we report the successful fabrication of the prototypes for such HBTs.   There are several techniques that can be adopted to increase the speed.   We employed a method in which we increased the concentration of Mg in the base region [1.0×10^{20}/cm^3] and applied a constitutional gradation of In [X=0 $\rightarrow$ 0.1].   At the same time, we set the offset for the alignment of the base and emitter to   0.2 μ m   using an i-line stepper.   Consequently, we achieved an alignment accuracy as high as that in self-alignment. In addition, the GaAs layer under the base metal contact layer was etched away to minimize the parasitic capacitance across the base and collector. In this process, obtaining only an etched base layer is the key point; we achieved this by

Table 1	Layer Structure	
Emitter Cap 120nm	n-In$_x$Ga$_{1-x}$As (X: 0 $\rightarrow$ 0.75)	4×10^{19}/cm^3
Etch Stopper 10nm	n-In$_{.5}$Ga$_{.5}$P	1×10^{19}/cm^3
Emitter 75nm	n-Al$_{.225}$Ga$_{.775}$As	5×10^{17}/cm^3
Base 60nm	p-In$_x$Ga$_{1-x}$As (X :0.1 $\rightarrow$ 0)	1.0×10^{20}/cm^3
Collector 150nm	n-GaAs	5×10^{16}/cm^3
Subcollector 700nm	n-GaAs	1×10^{19}/cm^3

using an InGaP etch-stop layer

II. Material, Growth, Fabrication, and Experiments

Table 1 shows the layer structure of the HBT. A multichambered solid-state MBE apparatus is used to grow the respective layers. Si and Mg were used n- and p-type dopants, respectively. In a previous paper, we reported that the Mg was a very good p- type dopant, similar to Be. Moreover, the diffusion coefficient of Mg is smaller than that of Be. To increase switching speed, electron was accelerated by the composition inclination of the InGaAs base. The heavily doped p-type InGaAs base was grown at a temperature of 500°C with the growth rate of $0.2 \sim 0.3$
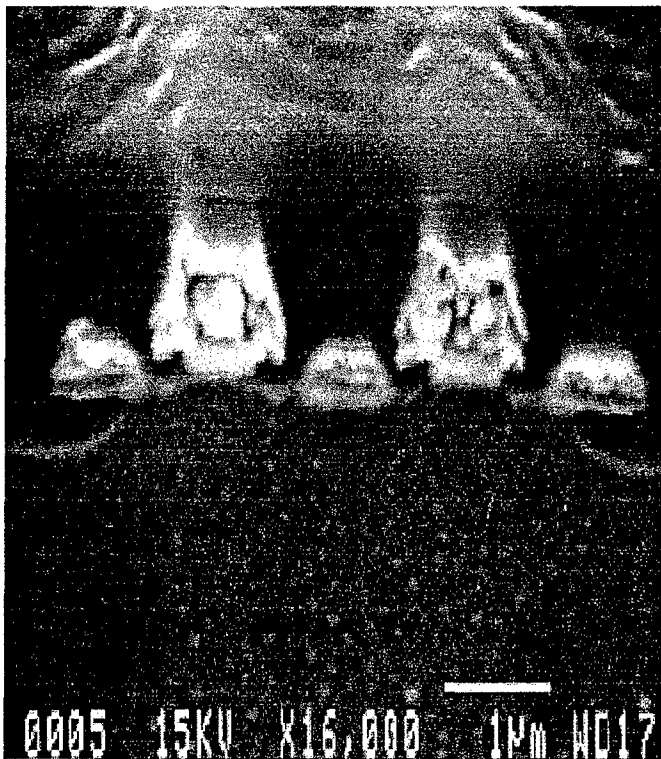
Figure 1 SEM micrograph of cross sectional view of our dual emitter type our HBT)

μ m/h. The HBT's main epi-layers were grown in the As-growth chamber. The n-type InGaP layer was grown in the P-growth chamber. In this chamber, phosphorus vapor was supplied by pyrolysis of high purity InP. The InGaP etch-stop layer placed at the depth within the emitter layer reduced the number of factors contributing to the instability in the wet-etch process.

To minimize the parasitic capacitance across the base and collector, the collector GaAs layer under the base metal contact layer was etched away.

Figure 1 shows a cross sectional view of the our dual emitter type HBT. From this figure, it was determined hat GaAs in the base part on both sides was removed by the etching. The parasitic capacity of the base could be considerably reduced by this etching away process.

We set the clearance of the base and emitter at 0.2 μ m with an i-line stepper. From the SEM image in figure 1, it is clear that we achieved an alignment accuracy as high as that in the self-alignment process. We could exclude the non- reliability, fluctuations and instability caused by the self-alignment process.

For other IC elements, the thin film resistors were fabricated using Ta_2N and the thin film MIM capacitors were fabricated using Ta_2O_5.

Over the whole 4 inches S. I. Of the GaAs substrate, we could obtained a very high yield of the HBTs and the HBT-ICs with the above mentioned process.

III. Characteristics of HBT and IC

Figure 2 shows the high-frequency characteristics of the HBT. The S-parameter was measured with the current density of $2.5 \times 10^5 A/cm^2$ and Vcc=1.8V. An HP 85109C vector network analyzer and Cascade microtech WPH series coplanar waveguide probing heads were used to measure these RF characteristics. For the HBT with a single emitter of $1.5 \times 10 \ \mu \ m^2$ and our proposed structure, excellent frequency characteristics of ft and fmax as high as 140 GHz and 230 GHz, respectively, were obtained.

IV. Applications

Figure 3 shows the circuit diagram of the 80GHz negative resistance oscillator, which incorporated a 1.5×10 μ m single emitter HBT. The HBT was biased to the collector-emitter voltage Vcc=2V and the collector current Ic=12mA in a common collector configuration.

Figure 4 shows an output spectrum which is measured using an HP 71209 spectrum analyzer. The typical output level is -9dBm where the reading from the trace excludes the 5dBm conversion loss, the details about these data are in our paper[2].

Figure 3   80GHz HBT Oscillator Circuit
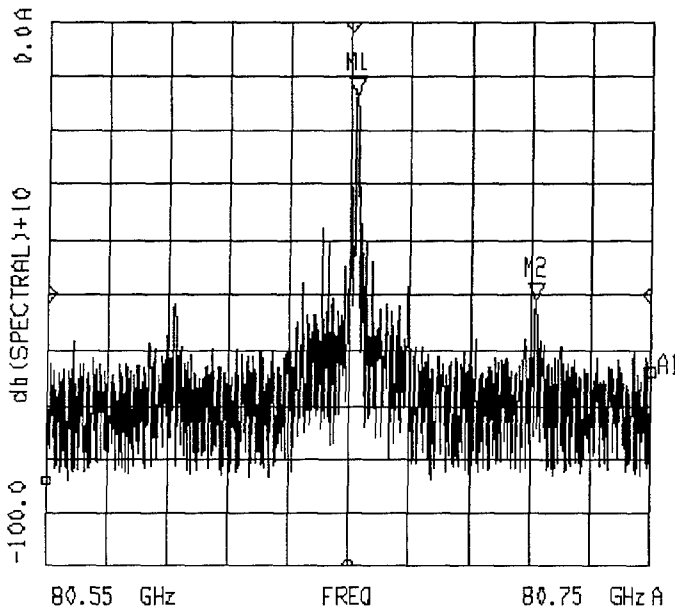
Figure 4   Output spectrum of the 80GHz oscillator
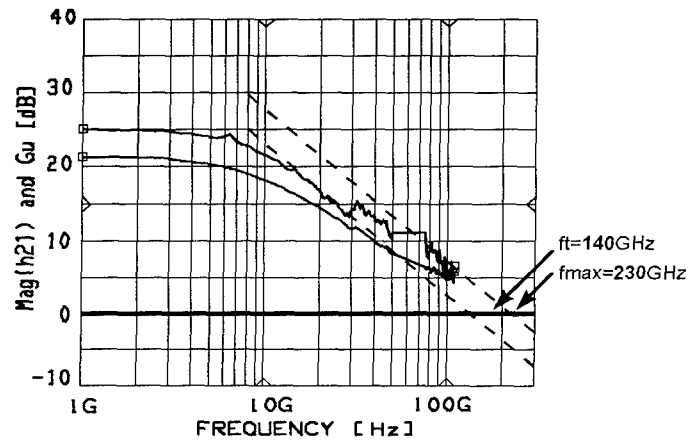
Figure 2   High-frequency characteristics of our HBT .with a single emitter of $1.5 \times 10 \ \mu \ m^2$
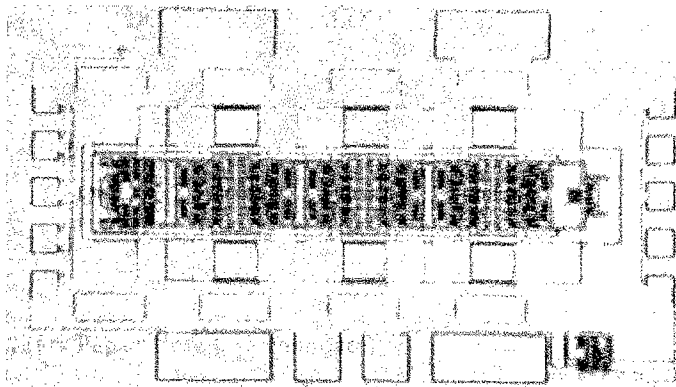
Figure 6 shows an ECL 1/2 static frequency divider

Figure 5 10 stage ECL-gate ring oscillator

Figure 5 shows a 10-stage ECL-gate ring oscillator, which consists of 190 HBTs. For digital circuit applications, the delay time of one ECL gate can be estimated with this ECL ring oscillator. We obtained 13ps for one ECL gate.

Figure 6 shows an ECL 1/2 static frequency divider, which consists of 130 HBTs. For composing logic circuits, the circuit speed can be estimated by the static frequency divider. We obtained maximum toggle frequency of 22.5GHz for the static frequency divider. When converting this value to the NRZ signal, the high-speed digital signal of 45GBps can be treated by using our InGaP/AlGaAs/InGaAs graded-base HBTs.

V. Conclusion

We have fabricated ultrahigh-speed InGaP/AlGaAs/InGaAs graded-base hetero-bipolar transistors (HBTs), which employ Mg as the base-region p-type dopant. The dead region under the base metal contact layer has been etched away. We obtained excellent frequency characteristics of the short-circuit current-gain frequency ft and the maximum frequency of oscillation fmax as high as approximately 140 GHz and 230 GHz, respectively.

For circuit applications, we obtained a maximum toggle

frequency of 22.5GHz and direct oscillation frequency of 80GHz for the static frequency divider and the base common transistor oscillator, respectively, by using the 4-inch full process of InGaP/AlGaAs/InGaAs graded-base HBTs

VI. Acknowledgment

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Overgrowth of InGaAsP Materials on Rectangular-Patterned Gratings Using GSMBE

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I. Abstract

Periodic perturbations of the refractive index is a foundation for realizing InP-based single mode photonic devices for all-optical communication networks. In order to achieve a particular refractive index modulation, such as that required by distributed feedback lasers and Bragg grating resonators, the periodic structure must reside within the device, necessitating epitaxial overgrowth. Results of an investigation of a low temperature oxide removal technique combined with gas source molecular beam epitaxial overgrowth of x-ray lithographically patterned rectangular gratings will be presented.

II. Introduction

Inherent in epitaxial growth is the need to remove the native oxide from the starting growth surface to enable the nucleation of a crystalline semiconductor overlayer. Typically, the oxide is removed by thermal desorption. However, since this technique is influenced by the wafer type, the age of the wafer, and the method used to mount the sample, the oxide desorbs from each sample at slightly different time and temperature combinations. Additionally, at elevated temperatures patterned surfaces are easily modified via mass transport effects. For the operation of distributed feedback lasers, some degradation of the overgrown grating is not detrimental. However, a variety of planar waveguide-coupled Bragg-resonant filters require high fidelity gratings following overgrowth [1,2].

A common method of suppressing the profile degradation of sawtooth-patterned InP gratings, using both solid source and gas source molecular beam epitaxy, is the desorption of the native oxide under an arsenic and phosphorus overpressure, independent of the group V composition within the patterned material. However, up to 30% profile degradation of sawtooth-patterned InP surfaces still

occurs during oxide desorption with an impinging As/P flux [3,4].

The use of a low temperature atomic hydrogen-assisted oxide removal technique combined with the gas source molecular beam epitaxial (GSMBE) overgrowth of rectangular-patterned gratings is under investigation. Gratings, patterned in both InP and $In_{1-x}Ga_xAs_yP_{1-y}$ epitaxial layers (lattice-matched to InP), with various overgrown epitaxial layer materials are analyzed. The surface morphology and the optical quality of the epitaxial layers are discussed, in addition to the significance of the low temperature oxide removal technique. Finally, preservation of the overgrown rectangular-patterned grating profile is confirmed via triple axis x-ray diffractometry (TAD).

III. Experimental Procedure

Rectangular-patterned gratings, having a 240nm period, are fabricated in both InP substrates and InGaAsP epitaxial layers via x-ray lithography. 50nm of SiO_2 is deposited on the wafer, followed by 250nm of polymethyl-methacrylate (PMMA). The coated wafer is then cleaved, and individual chips are placed in electrostatic contact with the x-ray mask. Following the x-ray exposure, the PMMA is developed in a methylisobutylketone:2-propanol

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(1:2) mixture. The grating pattern is then transferred into the SiO$_2$ via reactive ion etching (RIE) in a CHF$_3$ plasma. After removal of the remaining PMMA by oxygen plasma, the grating pattern is etched into the InP or InGaAsP by RIE in a CH$_4$:H$_2$ (1:4) plasma, achieving vertical sidewalls to depths of 80-110nm. Finally, the SiO$_2$ mask is removed with buffered hydrofluoric acid.

Prior to loading the sample into the GSMBE growth chamber, the rectangular-patterned gratings are degreased and wet chemically etched. The etchant removes some of the RIE-incurred damage while simultaneously preserving the grating profile. As indicated by Auger electron spectroscopy, scanning electron microscopy (SEM) and TAD, the grating profiles are free of residual processing contaminants and unaltered by the wet chemical cleaning process; the resulting surface is similar to that of an epi-ready wafer.

An atomic hydrogen source residing within the Riber 32P GSMBE reactor is employed to remove the native oxide from the patterned surfaces at temperatures significantly below those required for thermal oxide desorption (450°C) [5]. The atomic hydrogen-assisted oxide removal is performed at 200°C, reducing the time in which the patterned surface is exposed to elevated temperatures in the absence of material deposition.

Following the low temperature atomic hydrogen-assisted oxide removal, the patterned substrate is raised to the growth temperature under a group V flux that corresponds to the group V composition in the patterned material. Within two to three minutes of reaching the desired growth temperature (480°C), overlayer deposition is initiated at a growth rate of approximately 1μm/hr.

Various post-growth characterization techniques are used to analyze both the quality of the epilayer as well as the fidelity of the overgrown grating. These techniques include Nomarski interference microscopy, SEM, TAD, and low temperature (10K) photoluminescence (PL). The SEM was performed with a Zeiss DSM 982 Gemini electron microscope. The triple axis x-ray diffractometry was performed on a Bede D^3 diffractometer [6].

IV. Results and Discussion

Integral to the ability to deposit epitaxial layers on patterned surfaces is the ability to repeatably remove the native oxide without causing damage to, or degradation of, the patterned surface. The use of the low temperature atomic hydrogen-assisted oxide

removal technique leaves the patterned surface relatively unaffected. Figure 1(a) is a SEM micrograph that visually verifies the grating quality. The profile of this grating is essentially identical to that of a wet chemically etched grating. Figure 1(b) depicts TAD analysis that clearly shows the periodic fringes that correspond to a rectangular profile grating. The absence of the ±2nd order beams is indicative of a grating profile with equal lines and spaces and well defined edges. The separation of the periodic fringes confirms a grating period of 240nm [7].

(a)

(b)
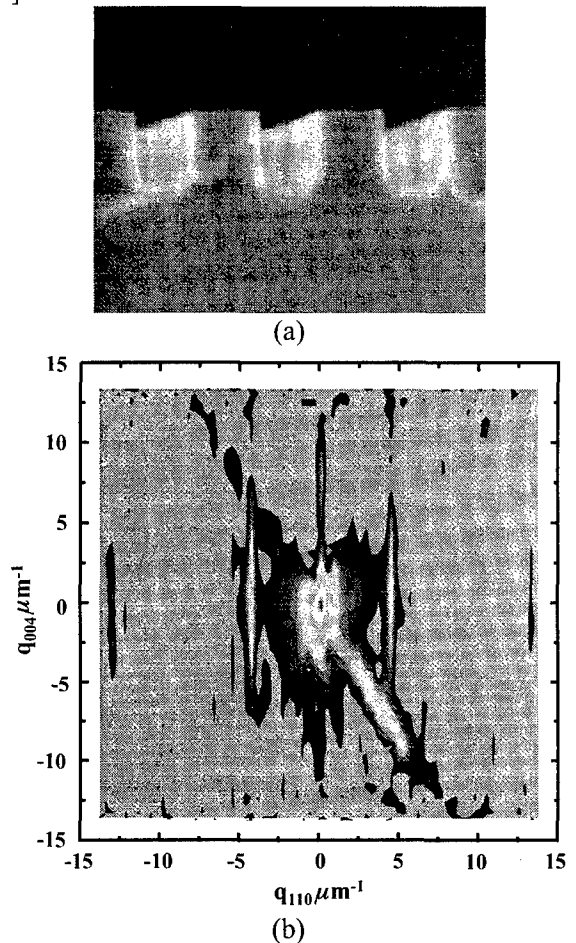
Figure 1. (a) SEM micrograph of a low temperature atomic hydrogen-cleaned rectangular-patterned InP grating. (b) TAD analysis of the grating in Fig. 1(a).

In order to more accurately characterize the material grown on the patterned surfaces, a portion of an InP epi-ready wafer was simultaneously mounted alongside the patterned sample to provide an experimental control. Typical surface morphology, analyzed via Nomarski microscopy, indicated that the patterned surface overgrowth morphology was as smooth as, or slightly rougher

than, that of the unpatterned InP control sample, although both surfaces remained specular. Additionally, planarization of 1μm of InP and 200nm of $In_{1-x}Ga_xAs_yP_{1-y}$ (x~0.07, y~0.23) deposited on rectangular-patterned gratings of InGaAsP (x~0.23, y~0.43) and InP, respectively, was verified via SEM and transmission electron microscopy.

The optical quality of the overlayers was determined via low temperature PL. Of particular importance is the PL intensity and its indication of nonradiative recombination. The signal strength of the epitaxial layer grown on the patterned surface is less intense than that of the control sample due to the increase in interfacial area between the patterned material and the epi-layer. Additionally, the use of RIE for formation of the rectangular gratings damages the surface. Although some of the damaged material is removed by the wet chemical etchant, it is probable that damaged material remains on the surface of the gratings. Figure 2(a) shows the PL spectrum of an unpatterned InP control wafer with a 200nm InGaAsP (x~0.07, y~0.23) epi-layer. Figure 2(b) shows the PL spectrum of a rectangular-patterned InP grating overgrowth, in which the InP signal is undetectable. The InGaAsP epi-layer signal is 10 times weaker when a grating is present. The quaternary composition of the epitaxial layer on the InP grating is unaffected by the presence of the patterned surface. Additionally, the full-width-at-half-maximum (FWHM) of the epitaxial layer on both the patterned and unpatterned samples are essentially identical.

The existence and preservation of the rectangular-patterned gratings following the GSMBE overgrowth was verified via SEM and TAD. Various patterned surface overgrowth experiments have been performed (structures described in Table 1). In all experiments, the presence of the overgrown grating was verified via TAD.

The use of the low temperature atomic hydrogen-assisted oxide removal technique is of particular importance to the fidelity of the overgrown grating. This surface cleaning method alleviates the dependence on thermal oxide desorption and is crucial to preserving the profile of the grating. More specifically, the oxide is completely removed from a low temperature atomic hydrogen-cleaned sample when the sample reaches the growth temperature. Thus, the epitaxial layer can be nucleated immediately, thereby reducing the

amount of time the patterned surface is at elevated temperatures in the absence of material deposition.

(a)

(b)
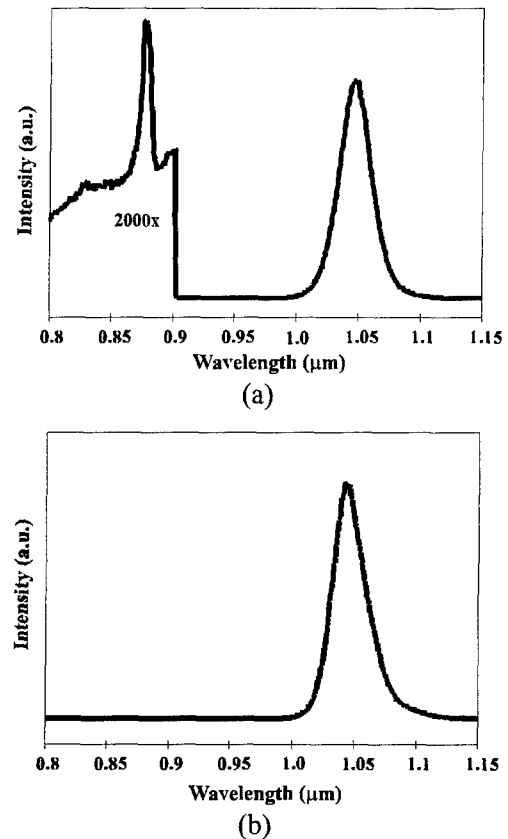
Figure 2. (a) 10K PL of InGaAsP (x~0.07, y~0.23) on an unpatterned InP substrate. (b) 10K PL of InGaAsP (x~0.07, y~0.23) on a rectangular-patterned InP grating. The PL signal is 10 times less intense than the signal in Fig. 2(a). In both cases the FWHM of the InGaAsP signal is approximately 33meV.

Table 1. Documentation of Overgrowth Structures.

Patterned Material	Epi-Layer Material
InP	InGaAsP (x~0.07, y~0.23)
InGaAsP (x~0.23, y~0.43)	InP
InP	$In_{1-x}Ga_xAs$ (x~0.47)

To verify the effectiveness of the low temperature atomic hydrogen-assisted oxide removal technique, an InGaAs epitaxial layer was deposited on both an hydrogen-cleaned and a thermally-cleaned InP grating. The thermally-cleaned grating was exposed to the growth temperature (480°C) without deposition for approximately three minutes longer than the hydrogen-cleaned grating in order to verify the absence of the native oxide via reflection high energy electron diffraction. Both epitaxial layers consisted of 200nm of InGaAs nominally lattice-matched to InP, as verified by x-ray

diffraction of the control sample. However, the average composition of the InGaAs overlayer is different from that of the control sample. Specifically, the concentration of In is greater in the patterned surface overlayer than that of the control overlayer. This phenomenon has also been observed by other groups [8].

(a)

(b)
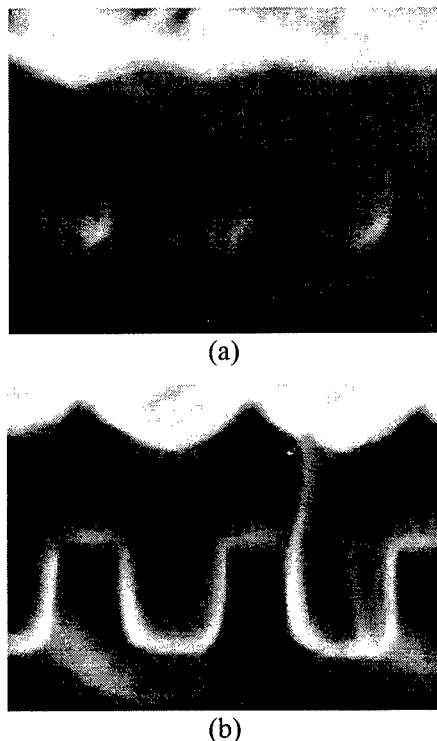
Figure 3. (a) SEM micrograph of InGaAs on thermally-cleaned rectangular-patterned InP gratings. (b) SEM micrograph of InGaAs on low temperature atomic hydrogen-cleaned rectangular-patterned InP gratings.

Although the grating is present in both samples, a SEM comparison shows observable degradation of the thermally-cleaned grating, as shown in Figure 3(a). The grating degradation is indicative of the onset of mass transport: slightly thinned grating teeth, slightly filled-in grating trenches, and a slight rounding of both the grating teeth and trenches. The hydrogen-cleaned grating experienced very minimal, if any, grating degradation (Figure 3(b)) and appears very similar to the hydrogen-cleaned grating in Figure 1(a). An additional feature seen in the SEM micrographs is the non-planarity of the InGaAs epitaxial layers. Although this effect has been observed by others, it is not yet understood and is still under investigation [8,9]. The results of this comparison emphasize the vulnerability of patterned surfaces to elevated temperatures. In a matter of minutes the patterned surface experiences mass

transport effects which degrade the patterned profile, thus illuminating the need for a low temperature cleaning process.

V. Summary

The use of a low temperature atomic hydrogen-assisted oxide removal technique has been shown to minimize the degradation of rectangular-patterned surfaces in GSMBE overgrowth. The hydrogen-cleaning technique eliminates the need for an As/P flux mixture during the oxide desorption process of InP patterned surface overgrowth. Additionally, the epitaxial layer can be nucleated the moment the patterned surface reaches the proper growth temperature. TAD and SEM confirm the fidelity of the overgrown gratings.

VI. Acknowledgments

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MBE REGROWTH OF INP ON PATTERNED SURFACES AND ITS APPLICATION POTENTIAL FOR OPTOELECTRONIC DEVICES.

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Introduction

High-quality InP material was grown with solid source molecular beam epitaxy (SSMBE) using a GaP source. Dry- as well as wet-etched corrugated quaternary surfaces (DFB-gratings) were successfully regrown with InP, fully planarized final surfaces were obtained in each case. Finally, InP regrowth on mesa structures demonstrates favourable conditions for butt-coupling integration schemes.

I. Motivation

Advanced optoelectronic devices require multiple epitaxial steps and, consequently, high-quality regrown material. For InP-based integrated devices solid source molecular beam epitaxy (SSMBE) has not found an intensive use, which was mainly due to the impossibility of growing InP material. However, recent results show that high quality InP as well as InGaAsP can be obtained using a GaP source (1) or a valved cracker cell (2). A further drawback for MBE were apparent limitations concerning regrowth options. Despite promising results with (pseudo-) selective growth (3), specially the profiles of InAlAs/InGaAs layers regrown on mesa structures (4) were rather discouraging. It is the aim of this paper to demonstrate that by facilitating the growth of InP material, the situation changes drastically. Due to a higher surface diffusion length of the growth species, it is possible not only to planarize DFB-gratings, but to obtain smooth growth boundaries on dry-etched mesa structures as well, a crucial step for e.g. butt-coupling of optical waveguides.

II. Experimental

In our experiments, InP layers were grown in a conventional MBE system, equipped solely with an ion pump. A GaP source was used, which provides a cost-effective way to generate an extremely pure P_2 molecular beam. Reduction of the residual Ga beam was achieved by the implementation of a multiple diaphragm approach (5).

InP layers were deposited at temperatures between 400°C and 500°C. As already reported (1), InP layers show high optical quality, equivalent to state-of-the-art MOVPE-grown structures, and, due to lower growth temperatures, Be-doping levels as high as $1*10^{19}$ cm^{-3} are possible. However, arsenic contamination leading to strain relaxation was observed. After a thorough examination of the system, it is believed that this was due to parasitic As evaporation, as a result of GaAs deposited in the vicinity of the GaP source. Apart from thermal cleaning of the GaP source area, As-concentration in InP layers can be drastically
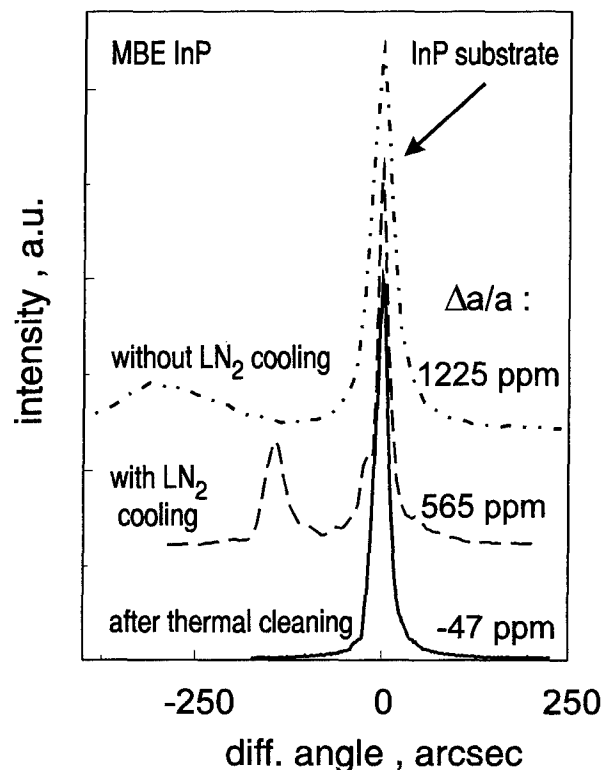
Fig. 1. Impact of continuous liquid N_2 cooling on the As-contamination in InP layers (MBE) as demonstrated on DCXRD-spectra of respective layers.

reduced by contaminant trapping through the continuous operation of the liquid N_2 cooling system (Fig. 1).

III. Regrowth of DFB gratings with InP

As a crucial step for the fabrication of DFB- (DBR-) lasers, InP regrowth was studied, to our knowledge for the first time, on corrugated quaternary surfaces. DFB-gratings were dry- as well as wet-etched in $In_{0.52}Al_{0.16}Ga_{0.32}As$
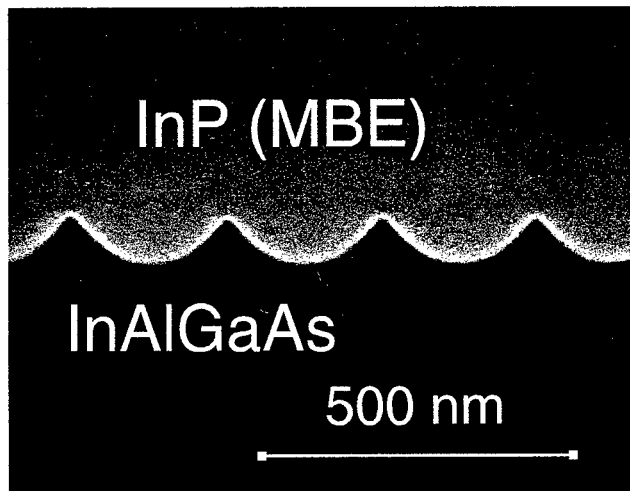
(a)
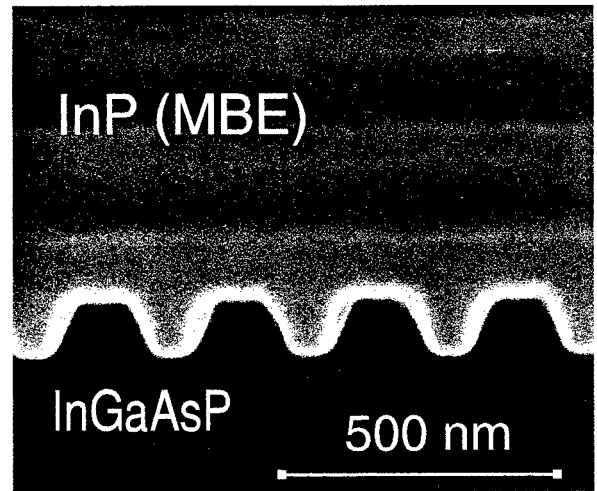
(b)

Fig. 2. SEM-views (cleaved facets) of a wet-etched $In_{0.52}Al_{0.16}Ga_{0.32}As$ (a) and a dry-etched (RIE) InGaAsP (λ_g = 1.3 μm) (b) DFB-grating, overgrown with InP (MBE). Gray shadows in (b) correspond to stain-etched, embedded, Si-doped layers.

and InGaAsP (λ_g = 1.3 μm) material. Fully planarized surfaces were obtained in each case (Fig. 2). By using Si-doped layers embedded in undoped material and a special stain-etch solution we were able to demonstrate that planarisation occurs within the first 100 nm of regrown InP material. We believe that this is the result of a higher surface diffusion length of the group-III component Indium, as compared to Ga or even Al, which leads to a high vertical-to-lateral growth rate ratio.
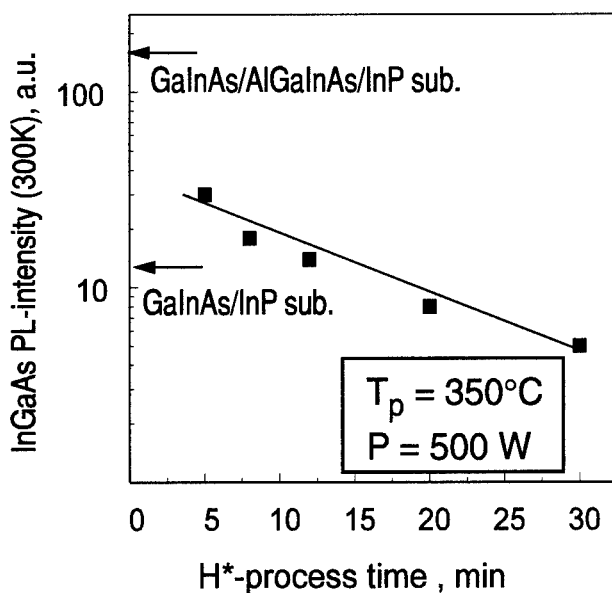
Fig. 3. Influence of the H* pre-treatment on the PL-intensity yield of a regrown InGaAs layer (T_{sub} = 535°C). Arrows show the measured PL-intensity of continuously grown layer structures.

In particular for the Al-containing layers, removal of the native oxide layer was performed by in-situ hydrogen radical (H*) processing. For DFB-laser applications the pre-treatment parameters were varied in order to achieve a high PL-intensity yield. As shown for a regrown InGaAs layer in Fig. 3, a long H*-treatment, which is necessary for a complete removal of the existing contamination (6), apparently creates surface defects; the respective PL-intensity yield is low. In the case of a short process (4 min.), a satisfactory PL-intensity is achieved, however, still a factor of 5 lower than for a continuously grown structure. Nevertheless, parallel regrowth tests on Broad-Area-Laser structures showed that this surface preparation method leads to threshold values practically equivalent to continuously grown structures.

No degradation of the DFB-gratings during the heating/stabilisation phase of the MBE process was observed. These promising results will be evaluated on DFB-lasers currently under process.

IV. Regrowth of structured surfaces with SSMBE material

Regrowth of InP opens various possibilities for accomplishing butt-coupled integration schemes with MBE, such as laser/passive waveguide coupling or monolithically integrated laser/modulator. This could be demonstrated by the regrowth of InP on patterned (mesa) structures. Prior to these experiments, InP mesas of up to 2 μm were etched with RIE. Thus, the MBE regrowth mechanism at vertical sidewalls could be investigated in detail. InP regrowth was performed at temperatures between 425°C and 475°C. The growth rate varied between 0.5 and 1.14 μm/h, V/III ratios between 6 and 12 were applied. As shown in Fig. 4 in both

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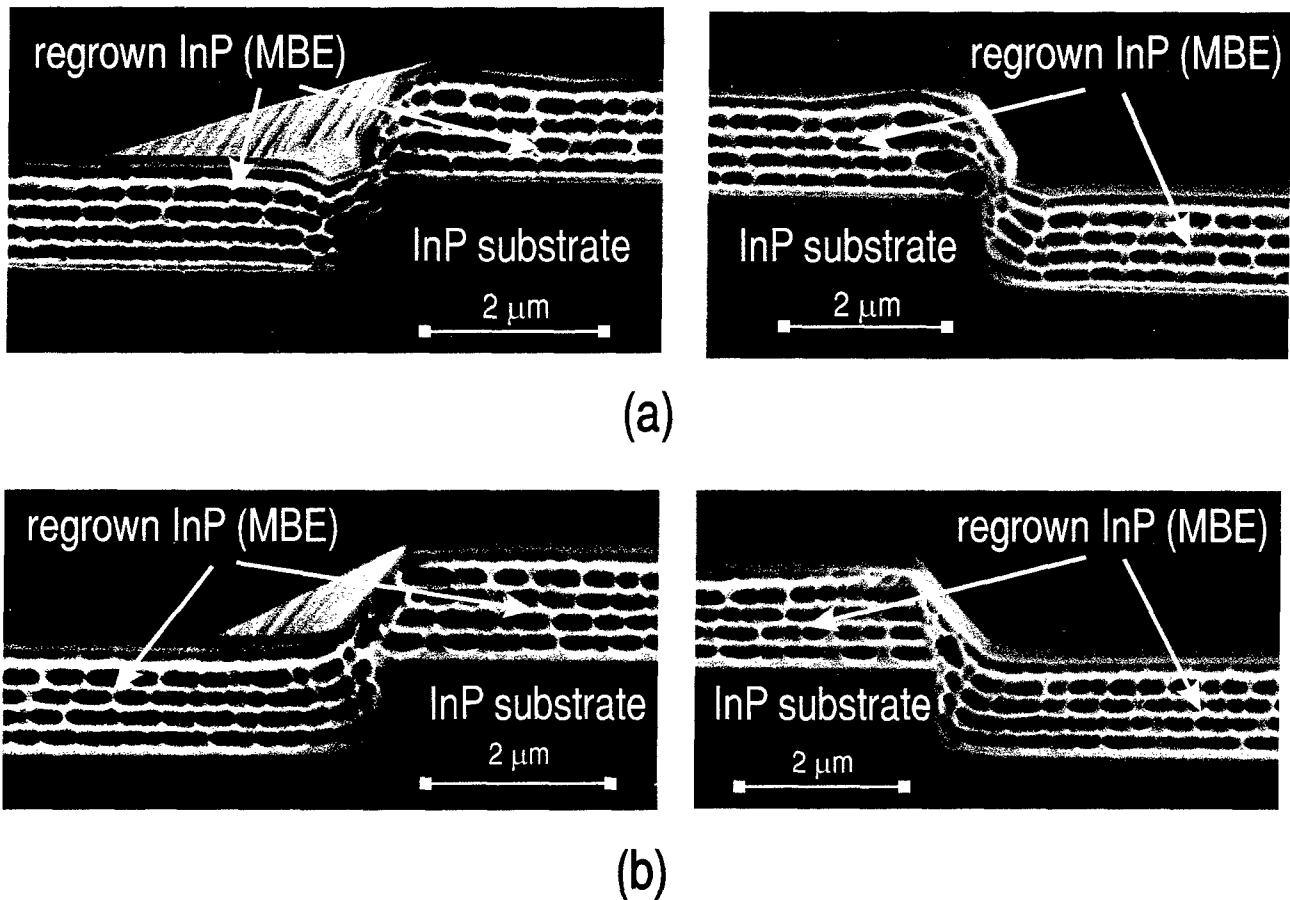
Fig. 4. Cross section (SEM view) of a patterned (mesa) InP substrate, (0-11) (a) and (0-1-1) (b) cleavage plane, over-grown with InP (MBE). The corrosion of the regrown material is due to inhomogeneous stain-etching of the embedded, Si-doped layers.

crystal directions ([0-1-1] and [0-11]) smooth growth boundaries were obtained. Due to the low ratio between lateral and vertical growth rate eventual thickness distortions remain in a limited lateral zone of less than 2 μm from the mesa sidewalls, despite the shadowing effects arising from the MBE evaporation geometry. The growth parameter variation showed insignificant changes of the regrown structure profile, which demonstrates a high process stabi-

lity.

In comparison, reported experiments (4), as well as own results with InAlAs/InGaAs regrowth on similar structures, showed trench-like structures near the vertical sidewalls. These are due to the lower surface diffusivity of the growth components Ga and Al. Nevertheless, through an appropriate choice of epitaxy parameters lateral growth on the mesa sidewalls can be achieved, as demonstrated by the SEM
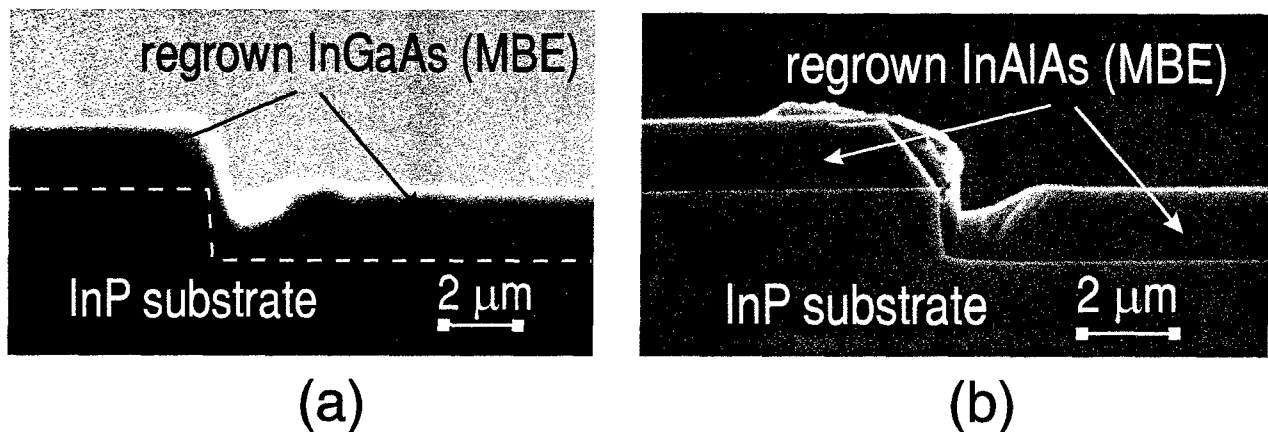
Fig. 5. Cross section (SEM view) of a patterned (mesa) InP substrate, (0-1-1) cleavage plane, overgrown with InGaAs (a) and InAlAs (b) (MBE). Despite the formation of a trench, smooth growth at the mesa sidewalls is apparent.

profiles in Fig. 5.

Thus, in the case of InP, the diffusion behaviour of the mobile group III species appears sufficient for a planar final surface and provides favourable conditions for butt-coupling integration schemes.

V. Conclusions

In conclusion, regrowth experiments were performed, based on high-quality InP material, grown by SSMBE using a GaP source. Full planarization of quaternary DFB-gratings was achieved. High diffusivity of In leads to planar layers after the first 100 nm of regrown material. In the case of structured surfaces (up to 2 μm mesas) with vertical sidewalls, smooth growth boundaries were obtained, eventual thickness distortions remained in a limited lateral zone of less than 2 μm. Growth parameter variation demonstrated a high process stability. These results open various possibilities for accomplishing InP-based monolithic integrated optoelectronic devices with SSMBE.

VI. Acknowledgements

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Electrical Characterization of High Resistivity InP and Optically Fast (sub-picosecond) InGaAsP Grown by He-Plasma-Assisted Epitaxy

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Introduction

Defects, intrinsic and extrinsic, are routinely used to tailor the electrical and optical properties of semiconductors. For example, an epitaxial technique using low growth temperatures has been used to produce As clusters in GaAs resulting in highly resistive, optically fast material with applications to picosecond switching [1] and radiation hardening [2]. For InP-based materials, a plasma assisted epitaxial technique has been developed at McMaster University which results in high resistivity ($>10^5$ Ω-cm) InP and optically fast (sub-picosecond) InGaAsP with a band-gap wavelength of 1.5 μm [3]. The initial electrical characterization of the plasma-generated traps responsible for the observed behaviour is presented in this submittal.

I. Background

InP and InGaAsP (band-gap wavelength 1.5 μm) have been grown by a He plasma assisted technique which consists of conventional gas source molecular beam epitaxy (GSMBE) with the surface of the crystal simultaneously exposed during growth to a flux of energetic He generated by electron cyclotron resonance (ECR). Compared to "normal" GSMBE material, the plasma grown material displays equivalent surface morphology under optical microscopy (x300) and similar double crystal x-ray diffraction linewidth. In addition, the plasma grown material has a reduced (more than a factor of 300) photoluminescent yield, and displays increased resistivity and speed of optical response. These general properties have been achieved for a range of growth temperatures of 430-470 C (typical of GSMBE), group V flows of 4-5 sccm, and He input to the ECR (operating at $\sim$ 100 W absorbed power) of about 10 sccm. Also, the speed of optical response and electrical resistivity have been found to depend on Be doping.

The effect of Be doping on optical response is illustrated in fig. 1 which presents the results of a

standard pump-probe measurement of the recovery of absorption in InGaAsP grown with He plasma for various values of Be doping.
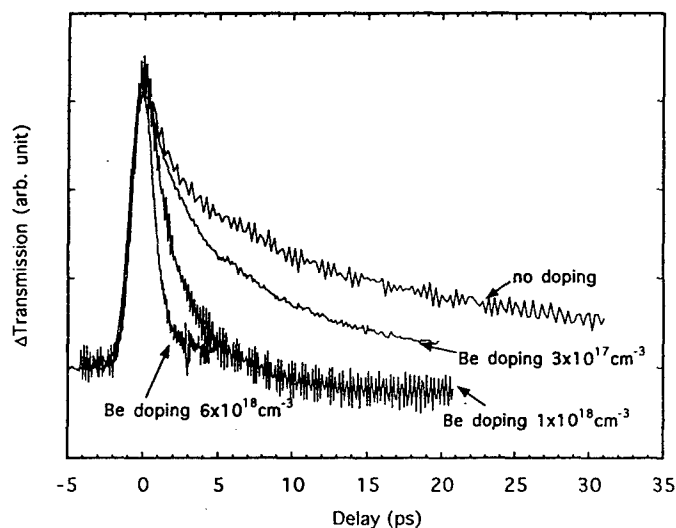
Fig. 1 Standard pump-probe measurements of change in transmission through 2 μm thick InGaAsP grown by He- plasma-assisted epitaxy for different Be doping concentrations.

The response time decreases with increasing doping level, and is sub-picosecond (experimental

resolution) for a doping level of 6×10^{18} cm^{-3}. To gain insight into the nature of the plasma generated defect responsible for this optical response, undoped and doped (Be $\approx 1 \times 10^{18}$ cm^{-3}) InP and InGaAsP grown with the He plasma have been characterized electrically by a) Hall measurement, b) temperature dependent resistivity, and c) current injection in n-i-n structures where the "i" region consists of the plasma grown material.

II. Electrical Characterization Results

a) Hall measurements (van der Pauw method at room temperature on 2 μm thick layers grown on semi-insulating substrates) indicate that He-plasma-grown InP and InGaAsP, undoped as well as doped with Be $\approx 1 \times 10^{18}$ cm^{-3}, is n-type. The mobility of the InP(He) is typically 500 - 1000 cm^2/Vs, while for the InGaAsP(He) it is 1000 - 2000 cm^2/Vs. The Hall method yields resistivities for the InP of 10^3-10^5 Ω-cm, and 40 - 500 Ω-cm for the InGaAsP ("normal" undoped material is typically <1 Ω-cm and n-type with a carrier concentration of $\sim 10^{15}$ cm^{-3}). Higher resistivities are obtained with the doped material. These results suggest that the He plasma introduces deep traps which lower the carrier concentration resulting in resistive material, as well as deep donors which compensate the Be doping. However, the Hall technique is somewhat unreliable for the higher resistivities since variable charge effects at the surface and substrate interface can overwhelm the low bulk carrier concentration in thin epilayers.

b) To more reliably determine the resistivity and an activation energy associated with the plasma generated traps, n-i-n structures were grown on n-type substrates where the "i" region consisted of the plasma grown material and the "n" layers were normal material doped with Si at 1×10^{18} cm^{-3}. After patterning with alloyed contact dots with radii 60, 100, 200, 300 μm, the samples were etched to produce mesa resistors. For InP "i" layers of 0.3 μm thickness, room temperature resistivities of greater than 10^5 Ω-cm are consistently achieved corresponding to a carrier concentration of <10^{11} cm^{-3} assuming a nominal mobility of 750 cm^2/V s. Doping with Be (1×10^{18} cm^{-3}) increases the

resistivity by up to a factor of 10. For InGaAsP "i" layers, 0.3 μm thick, resistivities of 4×10^4 and 50 Ω-cm, with and without Be doping respectively, are obtained.
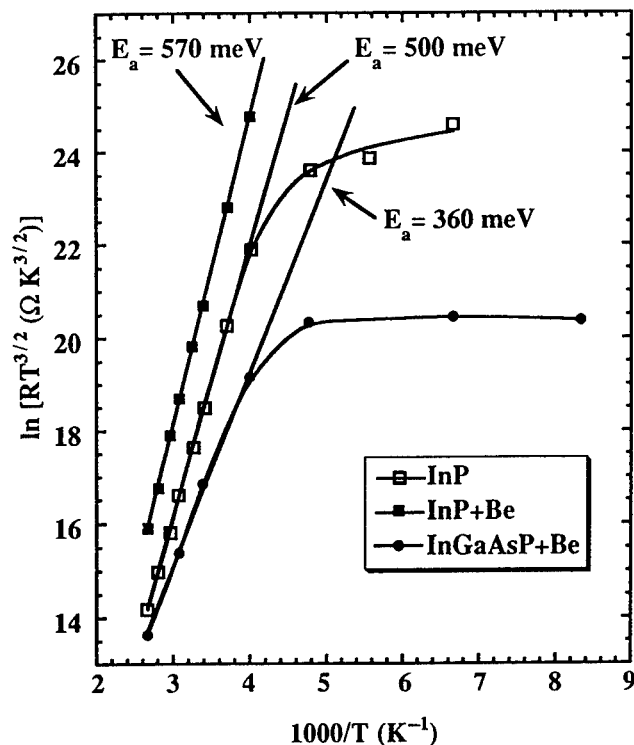
Fig. 2 *Thermal activation energy, E_a, plots for InP(He) and InGaAsP(He) devices.*

Figure 2 presents the results of temperature (T) dependent resistance (R) measurements for "i" layers of InP (200 μm device radius) with and without Be doping and InGaAsP (100 μm radius) with Be doping (the undoped InGaAsP material is too conductive to yield reliable results for the thin layer devices used in this study). The Arrhenius plot consists of the product $R \times T^{3/2}$, to account for the temperature dependence of the density of states, versus 1/T. For temperatures between 360 K and 250 K, thermal activation energies for InP of 500 meV without Be and 570 meV with Be are obtained, while for doped InGaAsP an energy of 360 meV is obtained. For lower temperatures the "plateau" indicates that another conduction process controls, perhaps due to tunnelling between defects

generated by the plasma.

The activation energies indicate that the Fermi level is near but above the centre of the bandgap; the effect of the Be doping is to move the Fermi level closer to mid-gap, which is consistent with the increase in resistivity with doping.

c) An estimate of the density, N_t, and the energy, E_t (relative to the conduction band), of the traps responsible for the Fermi level positioning discussed above can be obtained from the I-V characteristic for space-charge-limited current injection in which significantly more carriers are injected than are present in thermal equilibrium. The I-V characteristic for a 60 μm radius undoped InP resistor (as in part b) above) at 300 K is presented in fig. 3. Also shown are calculated curves based on the theory of current injection in solids [4] for traps of density N_t at
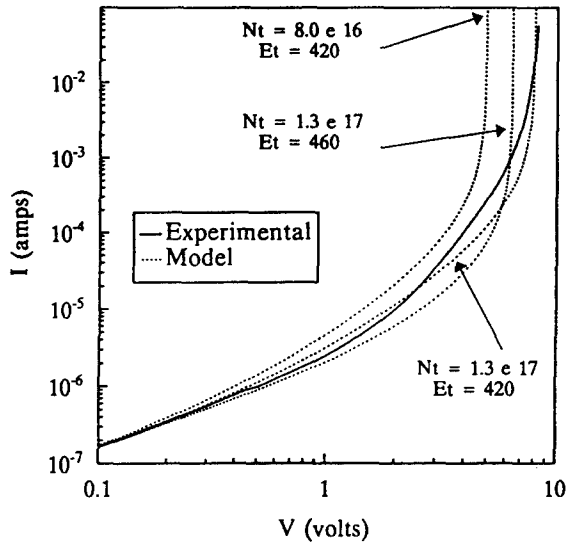
Fig. 3 Experimental results for current injection in InP(He) and model for traps of density N_t cm^{-3} at energy E_t meV.

energy E_t as indicated in the figure. Based on this model, the He plasma introduces ~1.3x10^{17} cm^{-3} traps at an energy of 420 meV below the conduction band.

Alternatively, the traps may be modelled as uniformly distributed in energy as shown in fig. 4 for trap densities N_{et} of 3x10^{17}, 6x10^{17}, and 1.2x10^{18} cm^{-3}eV^{-1}. Thus, in this model, which displays a better fit compared to the single energy model, the
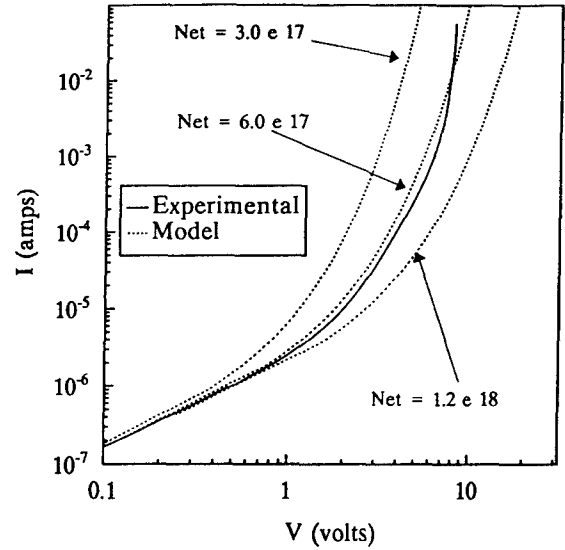
Fig. 4 Experimental results for current injection in InP(He), modelled with a continuous trap distribution; trap density N_{et}cm^{-3}eV^{-1}.

He plasma introduces ~6x10^{17} cm^{-3}eV^{-1} traps.

For the more resistive Be doped InP plasma material, the model with traps at a single energy yields a slightly increased trap density of 1.7x10^{17} cm^{-3} at 440 meV below the conduction band, as shown in fig. 5 for a 60 μm radius dot. Thus, the model indicates that the increased resistivity is attributable to both a higher trap density and deeper energy level(s). Note also that the single energy trap model fits the data for the Be doped material better than that for the undoped material.

Because the InGaAsP material has higher carrier concentration than the InP, reliable results for the trap characteristics by current injection in InGaAsP have not been obtained for devices fabricated to date.

The theory of space-charge-limited current injection contains several approximations; for example, diffusion currents are neglected and the carrier mobility is assumed constant, independent of the applied field. In this study, with 0.3 μm thick "i" layers, carriers from the n-type contacts may diffuse into the "i" layer and fill traps resulting in an effectively thinner "i" layer. Not accounting for
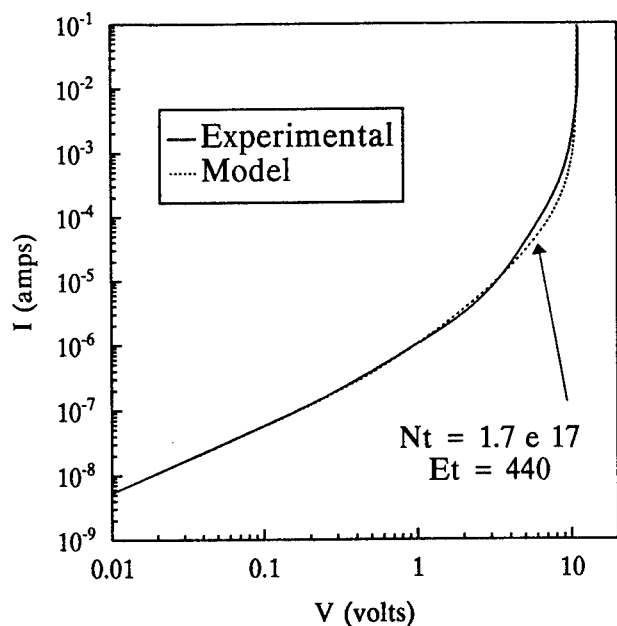
Fig. 5 Experimental results for current injection in Be doped InP(He), and single energy level model.

this effect would result in lower-than-actual trap densities. The impact of such effects on · the characterization of the plasma-grown material will be the subject of further work.

III. Summary Discussion

InP and InGaAsP grown with He plasma assisted GSMBE display increased resistivity and fast optical response. This resistive property is attributed to deep trapping states, associated with defects generated by the plasma, that deplete the undoped material. The observation that Be doped material grown with plasma is even more resistive (and weakly n-type) suggests that there is also a deep donor character associated with the defects which compensates the Be; however, this simplistic model is incomplete since Be doping of 1×10^{18} cm^{-3} only generates an additional $\sim 0.4 \times 10^{17}$ cm^{-3} deep states according to the results of the current injection modelling. More work is required to understand the role of Be doping, particularly in view of its impact on the optical response of InGaAsP (fig. 1). Interestingly, the highest doped (6×10^{18} cm^{-3}) material with the fastest response (subpicosecond) is p-type; the He plasma defects have not

compensated all the Be, yet the trend to increasing recovery rate continues with increased doping level.

Additional insight into the nature of the defects is provided by positron annihilation studies, not presented here, which suggest that the defects are vacancy clusters. Then, the electrical properties could be understood in terms of a surface depletion model, where the internal surface is distributed throughout the material in the same sense as the As cluster model of low growth temperature GaAs. Also, the vacancy cluster model could account for the greatly reduced photoluminescent yield of the He plasma material, since any "breathing" or distortion of the cluster accompanying the charge state change due to electron-hole recombination at the cluster would naturally couple to the phonon field and result in non-radiative recombination. Clearly, considerable work remains to develop a complete model of the behaviour of the potentially useful InP-based materials grown by He-plasma-assisted epitaxy.

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Highly resistive FET buffer layers on InP grown by LP-MOVPE MP8

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Introduction : Electrical characteristics of field effect transistors (FETs) grown on Fe-doped InP substrates are extremely dependent on the presence of a buffer with suitable resistivity below the active channel. The growth of a semi-insulating (SI) buffer layer on the InP substrate is required to compensate the n-type impurities (silicon) accumulation on the epi-ready substrate surface, responsible for parallel conduction at the substrate/buffer interface. Known techniques to prevent parasitic conduction in MOVPE growth [1,2] could not be reproduced successfully in our reactor or were not compatible with the use of patterned substrates for OEIC processing [3,4].

In this report, we describe new growth methods of semi-insulating buffers, using low pressure metalorganic vapor phase epitaxy. In both cases, specific growth procedures described below have allowed complete compensation of the electrical activity of n-type impurities at the interface.

All layers were grown in a home-made vertical LP-MOVPE reactor designed for three 2-inch wafers. Trimethylaluminium (TMAl), trimethylgallium (TMGa), trimethylindium (TMIn), arsine (AsH_3), phosphine (PH_3), ferrocene (CpFe) and disilane (Si_2H_6) are the available source materials. Pd-diffused hydrogen was employed as carrier gas. Reactor pressure was 50 torr.

InP [Fe] growth : the first buffer is a classical Fe-doped SI InP layer. All test samples consist of a 100nm thick InP [Fe] buffer grown on SI InP substrates. Only the substrate cleaning procedure and/or the pre-growth in-situ annealing are modified. TENCOR Sonogage non-destructive resistance measurement is used for sheet resistivities lower than 20kΩ and Hall effect measurement for higher values. Low sheet resistivities (~2kΩ/sq) of some of the samples are due to a conductive sheet at the interface, since n-I-n InP diodes grown in the same reactor show SI InP bulk resistivity as high as 2.10^7Ω.cm. As a consequence, the high resistivity of such a buffer layer is not sufficient to insure a good insulation below the FET channel. Electrical activity at the interface must be compensated.

To reduce silicon n-type impurity concentration at the interface, the InP wafer is first cleaned in a H2SO4 : H2O2 : H2O (5:1:1) etching solution, followed by a rinse in highly resistive deionized water and blown dry with nitrogen. The sample is quickly introduced into the reactor. When chemical etching is used, sheet resistivities are between 20kΩ and 500kΩ. SIMS analysis showed a reduction of Si concentration below 10^{18}cm^{-3} (table I). We find the 5:1:1 solution better than other acid solutions to keep the surface free of defect and to remove the silicon impurities simultaneously.

Comparison between C-V electrochemical and [Si] SIMS profiles of the described samples shows a 10%

to 30% range donors activation. As silicon can't be completely removed, if [Si] level is sufficiently low, it can be compensated by iron incorporation at a concentration equal or below the solubility limit (~2-3.10^{17}at/cm^3) of Fe in InP. We investigated compensation of this [Si] impurity by an Fe δ-doping just before the SI InP buffer growth. Figure 1 shows Fe concentration measured by SIMS in the following structure : SI InP substrate, Fe δ-doped interface, 100nm Fe-doped buffer and 250nm undoped InP layer.
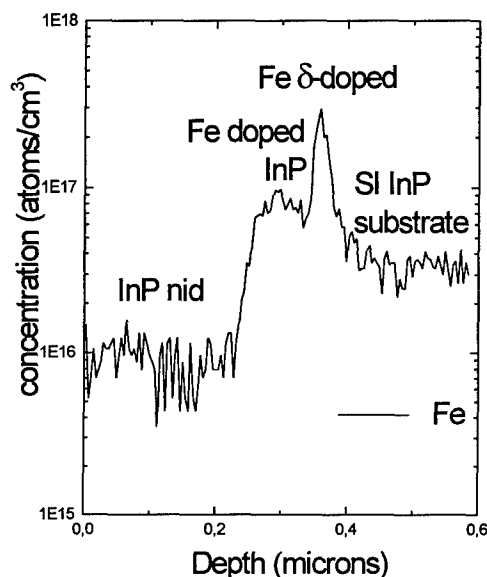
fig 1 : SIMS depth profile of Fe concentration in InP layers grown by MOVPE. Note Fe peak at the δ-doped interface.

This is achieved by the following procedure. First, a rapid thermal annealing of 60s at 650°C under PH3 is realised to desorb epi-ready oxide. Then, substrate temperature is lowered to 550°C - to limit Fe diffusion - and PH3 flux is reduced from 300 to 100sccm - to increase Fe incorporation. We first switch the CpFe flow to the growth chamber for 30s . At this time, while the CpFe flow is maintained at the same value, the TMIn flow is switched to start the SI InP growth and simultaneously the growth temperature is increased rapidly to 650°C.

When 5:1:1 etching and Fe δ-doping are omitted, sheet resistivity is always below 10kΩ/sq [5]. If Fe δ-doping is used without chemical etching, sheet resistivity depends on silicon concentration at the interface which can vary from one wafer to another. When both steps are used, SIMS depth profile shows Fe incorporation above $10^{17} cm^{-3}$ at the interface and sheet resistivity is always above 1MΩ/sq which is excellent. This buffer works very well for FET structures.

	no cleaning, no [Fe]δ-doping	5:1:1 etching	[Fe] δ-doping	5:1:1 etching and [Fe] δ-doping
[Si] at/cm^3	>10^{18}	<10^{18}	>10^{18}	<10^{18}
[Fe] at/cm^3	7.10^{16}	7.10^{16}	3.10^{17}	3.10^{17}
Rsq (Ω/sq)	R< 10kΩ/sq	20kΩ/sq <R< 500kΩ/sq	50kΩ/sq <R< 1MΩ/sq	1MΩ/sq <R

Table I : sheet resistivity, Si and Fe concentrations at the buffer/substrate interface for different surface preparation procedures.

AlInAs [C] growth : the second buffer is an undoped AlInAs layer. S. Ochi et al. have reported the high resistivity of $Al_{0.48}In_{0.52}As$ layers grown by MOVPE at low temperature [6]. They showed that carbon incorporation, depending on the growth temperature, compensates the native deep donors of the AlInAs layer. To our knowledge, we report for the first time the use of such a grown material as a buffer in MOVPE FET applications. Test samples consist of a 700nm undoped AlInAs layer grown on the SI Fe-doped InP substrate at different growth temperatures and for various V/III ratios. We confirm that carbon incorporation increases drastically as growth temperature decreases (fig. 2) and we observe that it decreases as well when V/III ratio increases (fig. 2).

Sheet resistivities lower than 20kΩ/sq were determined by TENCOR Sonogage non-destructive sheet resistance measurements and, for higher values, by current measurements on photolithographic TLM structures.
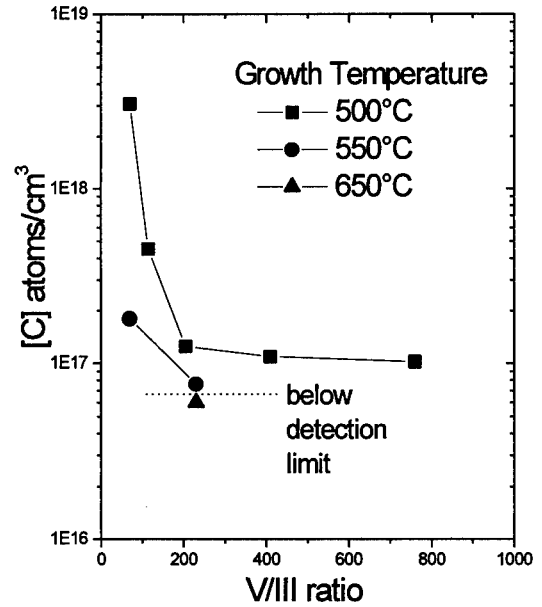
fig 2 : carbon concentration in undoped AlInAs layers grown by LP-MOVPE versus V/III ratio for different growth temperatures.

Figure 3 shows the sheet resistivities measured for the same samples versus V/III ratio at 500, 550 and 650°C.
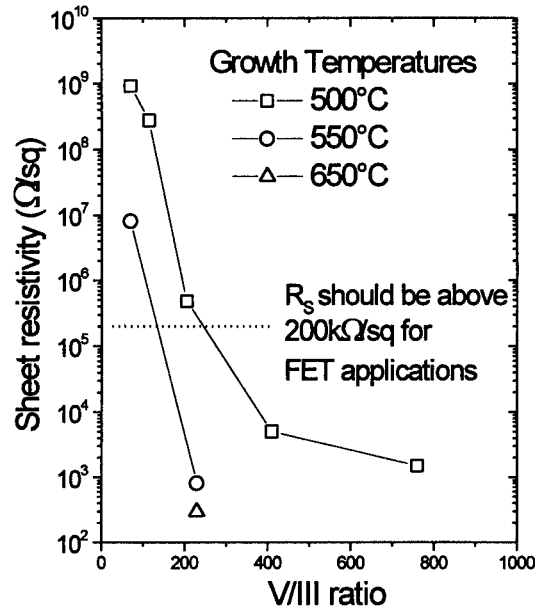
fig 3 : sheet resistivities of the undoped AlInAs layers versus V/III ratio for different growth temperatures.

One can observe that sheet resistivity varies drastically for a small carbon concentration variation around $1.3x10^{17} cm^{-3}$. At 500°C and low V/III ratio, the carbon incorporation in AlInAs is very high. Sheet resistivity as high as 920MΩ/sq was measured, which

means perfect semi-insulating continuity with the substrate. But in terms of surface morphology and crystal quality, samples grown at 500°C were not as good as those grown at 550°C or 650°C. At 550°C, using a V/III ratio of 70, high quality AlInAs is obtained as can be seen on the X-ray rocking curve on figure 4. Morphology is good and sheet resistivity is 8MΩ/sq, which is quite adequate for FET applications.
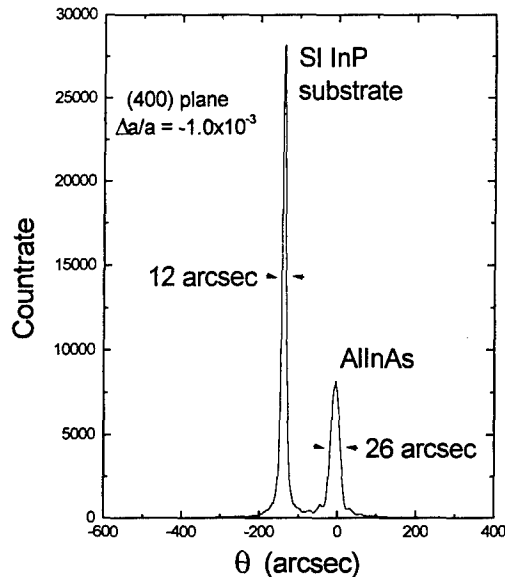
fig 4 : double crystal X-ray rocking curves of a 700nm thick u-AlInAs layer grown at 550°C and (V/III ratio)=70 on a SI InP wafer by LP-MOVPE.

Consequently, very thin buffers are sufficient (40nm) for FET structures. AlInAs spacer layer grown at 650°C between buffer and channel can be inserted to prevent channel depletion and some kink effects still under study.

This SI AlInAs deposition process is very promising : it is not necessary to prepare the wafer, carbon doesn't diffuse like iron into InP and sheet resistivities can be much higher than with Fe-doped interface and InP layers.

Device structures : the buffer growth process has been used in an interesting application of MOVPE for the fabrication of pin-FET OEICs in a single growth step (fig 5). InP substrates with etched wells have been used for the growth of FET structures followed by 2.5μm pin layers, without disturbing effects at the recess edges. The FET channel consists of an n-doped InP channel followed by an undoped GaInAs channel [7,8]. With the SI AlInAs buffer, this structure with donor charge transfer to the narrow bandgap material provides perfect channel pinch-off, a good control of pinch-off voltage and small gate leakage currents (fig 6) as required for the input stage of a pinFET receiver.
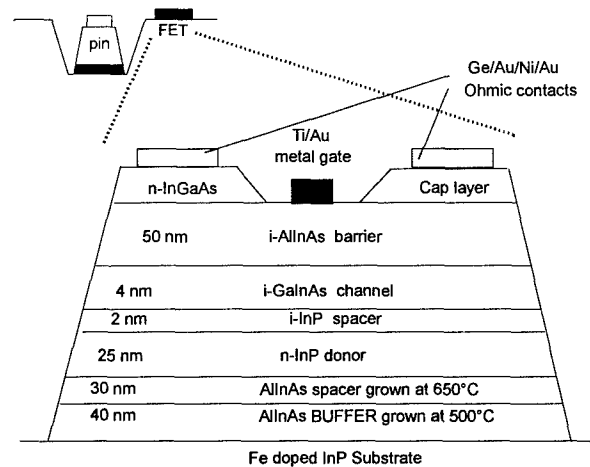
fig 5 : pinFET OEIC and FET structures.
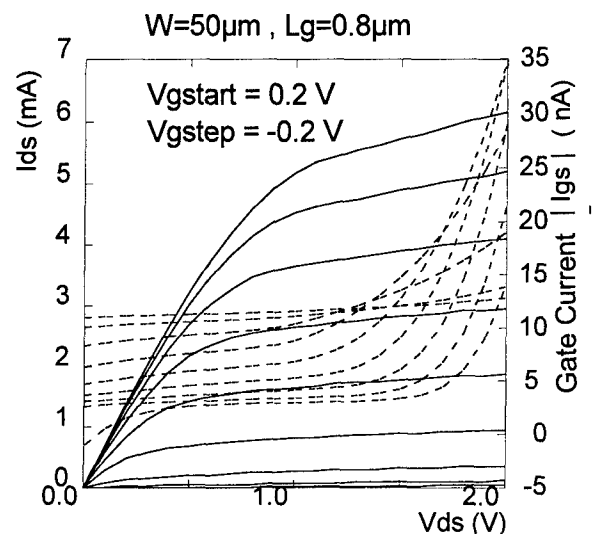
fig 6 : drain and gate current electrical characteristics.

Transistor DC and AC characteristics are unaffected by the pin growth and Zn diffusion steps, and working integrated photoreceiver arrays for 2.5Gb/s have been obtained.

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AlInAs/InGaAs Long-Period-Superlattice Resonant-Tunneling Transistor (LPSRTT) Prepared by MOCVD

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In this paper, we will demonstrate a new long-period-superlattice resonant-tunneling transistor (LPSRTT). A 20-period AlInAs/InGaAs superlattice is employed as a confinement layer and through which the RT action is developed. The interesting transistor and NDR performance are obtained for this device. The studied LPSRTT was grown by metal organic chemical vapor deposition (MOCVD) on a (100) oriented n^+- InP substrate. The device structure is illustrated in Fig. 1. The energy band diagrams of the studied device at thermal equilibrium is depicted in Fig. 2 (a). Figures 3 (a) and (b) show the common-emitter current-voltage (I-V) characteristics of the studied LPSRTT at room temperature and 77 K, respectively. It is found that a very small collector-emitter offset voltage only about of 90 mV is obtained both at room temperature and 77 K. This small offset voltage is due to the absence of potential spike at emitter-base (E-B) and base-collector (B-C) junction.

The interesting N-shape NDR phenomena are observed in the I-V curves at 77 K. The transport mechanism at 77 K may be described as follow. At low value of I_B (e.g., $I_B <$ 0.1mA), the V_{BE} is smaller than the p-n junction built-in voltage V_{bi}. Thus the applied V_{BE} is essentially across the E-B p-n junction until the flat band condition is achieved. Within this regime, the studied device acts as a conventional bipolar transistor. Beyond the flat-band condition, most of the additional increase in V_{BE} will fall across the superlattice. At some V_{BE} voltage (0.2mA $\leq I_B \leq$ 1.0mA), the Fermi-level E_F near emitter side aligns with the E_1 band in the superlattice as shown in Fig. 1(b). This will increase the transmissivity and current through the superlattice by RT action. When the collector-emitter voltage V_{CE} is increased, for the fixed I_B, the band structure near emitter side may be elevated quickly. This will cause the misalignment between E_F and E_1. Thus a quenching of RT through superlattice and the sudden decrease of conduction current will be found. This certainly exhibits an N-shaped NDR phenomenon in the I-V curves. Because the E_2 levels is near to the top surface of superlattice region, when the E_F is elevated up to align with E1, most of electrons will emit over the superlattice rather than tunnel through the E_2 band. Therefore, only a single RT and NDR phenomenon are observed in the studied device. On the other hand, at 300 K, the sufficiently high thermal energy cause most of electrons travel directly over the superlattice region. So, the RT action and NDR phenomenon are not found.

In summary, we have demonstrated a new GaInAs/AlInAs LPSRTT with 20-period i-AlGaAs/n^+-GaInAs superlattice. The good transistor performances are obtained both 300 K and 77 K. Furthermore, a significant N-shaped NDR phenomenon resulting from RT through the superlattice is obtained in the studied LPSRTT device at 77 K.
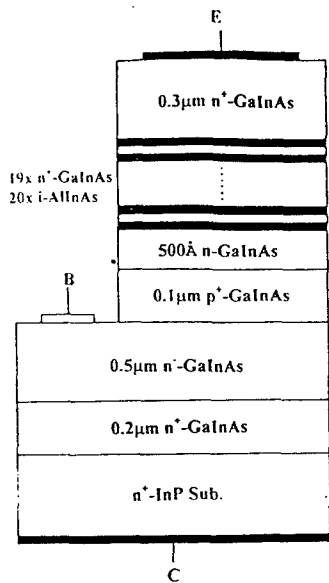
[FIG.1]The schematic cross section of the LPSRTT device

(a) V_{CE}=0.2 V/div

(b) V_{CE}=0.5 V/div

[Fig.3] Common-emitter current-voltage characteristics of LPSRTT measured at (a) 300 K and (b) 77 K. respectively.

[Fig.2] Schematic energy band diagrams of the proposed LPSRTT (a) at thermal equilibrium (b) at the onset of resonant tunneling.

78

InP NANOCRYSTALS VIA AEROSOL ROUTE

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Introduction

Indium phosphide nanocrystals, with diameters of around 10 nm, have been produced via an aerosol route. The production method allows a narrow size distribution of the nanocrystals. The method is based on the formation of monodisperse indium droplets and the subsequent reaction with phosphine at elevated temperature. The kinetics of the reaction of In to produce InP depends on the temperature and the phosphine flow. The size of the final InP nanocrystal is self-limited by the size of the introduced size-selected In droplet. This size can be tuned carefully. Since the new material grows in a self-organized fashion within the aerosol phase we call this process aerotaxy. Our approach opens the possibility for efficient production of size-selected semiconductor nanocrystals and it will allow new types of self-assembly and control of quantum dots.

I. Background

Nanometer-scale semiconductor crystals are of considerable interest due to their electronic quantum-size effects. However, the fabrication of such structures remains difficult regarding both the size and the size uniformity. A large deviation in particle diameters will average out any quantum-size effects. Indium phosphide is a commonly used material for optoelectronic applications. Nanocrystals of InP thus have a large potential for applications such as quantum dot lasers. Several attempts have been made to produce this type of nanocrystals by (i) organometallic vapor deposition into porous glass [1], (ii) solution phase synthesis [2,3], and (iii) utilizing the Stranski-Krastanow epitaxial growth mode [4]. All these attempts are characterized by the fact that the nanocrystals are bound in one or the other way to surrounding material. Most of those methods result in nanocrystals with wide size distributions. In this letter we present the fabrication of size-selected, contamination-free InP nanocrystals in the size range below 20 nm via a simple, reliable, and efficient aerosol route, called aerotaxy [5].

II. Experimental

In the present study, the same aerosol generator set-up has been used as in previous work on the fabrication of GaAs nanocrystals [6]. The fabrication route utilizes the formation of an aerosol of ultrafine indium particles. The aerosol is formed by evaporating the metal in a tube furnace and subsequent cooling down of the vapor. The aerosol particles are charged, and size selection takes place in a differential mobility analyzer (DMA). This instrument is a conventional tool in aerosol technology for both the fabrication of size-selected test aerosols and the measurement of aerosol sizes. It size-selects by balancing the mobility of charged particles in an electric field with the force of the gas used to flush unwanted particles, called sheath gas. The size distribution reached is mainly depending on the gas flows and can be made very narrow, e.g. ±5%. The monodisperse indium aerosol is then mixed with a phosphorus containing gas, here phosphine (PH_3), and sent into a second furnace for reaction. After the reaction furnace the particles can be deposited on a substrate by means of an electric field. The reaction process can be monitored with a second DMA. A schematic picture of the process is shown in Fig. 1.

Palladium-purified hydrogen was used to carry the metal aerosol, the flow of which was kept constant at 1.68 l/min. The experiments were performed with an aerosol generated at temperatures between 1100 and 1130°C. Charging of the aerosol took place in a diffusion charging device with a Kr-85 source emitting β-particles. Both DMAs were home-built devices of the Vienna type [7] and were run with 10 l/min nitrogen sheath gas (purity better than 99.995%) to flush away unwanted particles. An electrometer was used to determine particle number concentrations. A flow of phosphine (electronic grade purity), set to either 0, 2, 4, 8, 16, 32 or 64 ml/min, was introduced into the aerosol flow before entering the reaction furnace. The range of phosphine flows (for non-zero flows) resulted in a ratio of the number of phosphine molecules to the total number of indium atoms in the particles on the order of 10^6 to 10^7. The reaction furnace was operated at settings from room temperature to 650°C, a temperature range in which one may expect reaction of PH_3 with In to form InP. At each temperature setting a scan was recorded of the size distribution of the aerosol particles leaving the reaction furnace. The maximum of the size distribution curve was used as a measure for the mean particle diameter. Into the reaction furnace were let three
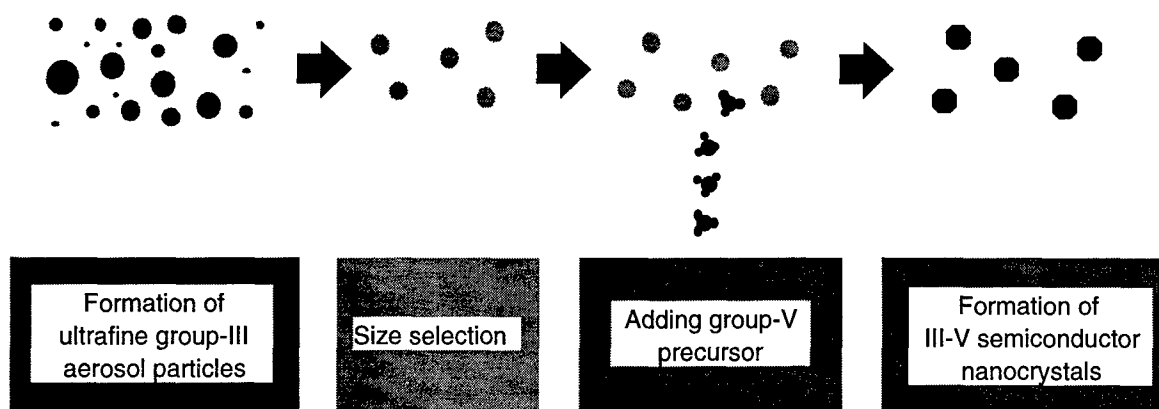
Fig. 1: Schematic diagram of the aerosol generation, sizing and reaction process.

different primary particle sizes of the indium aerosol, set to either 13, 15 or 17 nm.

The ratio of the flows in the DMAs gives a theoretical spread in the size distribution of 16%. However, the use of hydrogen as aerosol carrier and nitrogen as sheath gas implies some deviation from the normal DMA operation, thus making the calculation of the particle diameter a difficult issue. The error, however, is a systematic offset and can be solved, e. g. by calibration with transmission electron microscopy (TEM). Any given particle diameter in this letter is taken from the calculation using the ideal transfer function of the DMA. An earlier TEM study showed that those diameters may be up to 50% too large [5].

Samples have been prepared for high-resolution transmission electron microscopy at certain conditions of the reactions by depositing particles on a standard grid for electron microscopy after the reaction furnace. By investigation of those samples, high-resolution images of single particles could be obtained. Furthermore, for a few samples it was possible to acquire energy-dispersive x-ray spectroscopy data, as well as electron diffraction patterns of the particles.

III. Results and Discussion

The present work focuses on the change in the aerosol particle characteristics with temperature in the reaction furnace and with phosphine flow. The reaction results in a change in size distribution, depending on both the temperature and the phosphine flow. The characteristic shape of the size distribution, however, does not change with temperature. Thus, the maximum of this curve can well be taken as a measure of the mean particle diameter. The changes to be observed with increasing temperature are connected with changes in the particle diameter. Fig. 2 gives an example for a certain inlet diameter of the indium particles and different phosphine flows.

Several observations can be made from these plots. First, a difference in the plots concerning whether phosphine is present or not, second, a pattern in the diameter development with non-zero phosphine flows, and third, some difference for different phosphine flows. The difference in the behavior of the particles is striking concerning whether phosphine is present or not. Without phosphine the particle diameter decreases, at first slowly until about 500°C and then at an increased rate. This can be attributed to the evaporation process the pure indium particles undergo. A simple model of the evaporation process [8] shows a good agreement with the measured decrease in particle diameter when the temperature increases. As soon as phosphine is added to the aerosol flow this evaporation process is suppressed and the reaction steps of indium droplets with phosphine can be followed.
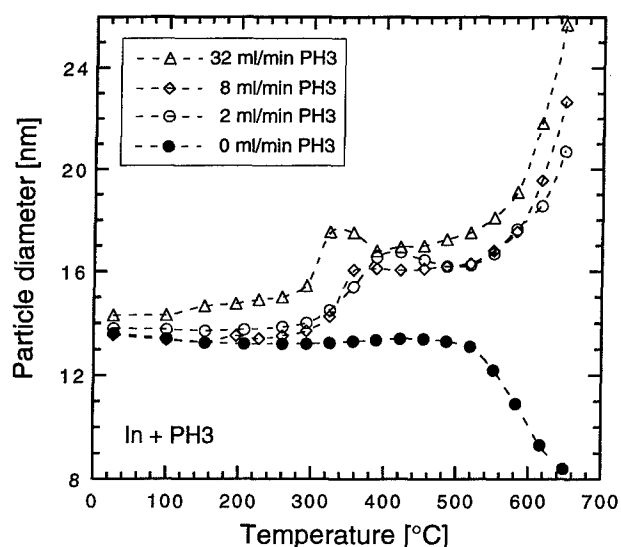
Fig. 2: Plots of the mean particle diameter of the reaction of indium particles with phosphine for different temperatures.

The overall picture of the reaction is similar for all phosphine flows investigated in this study. Step one, between room temperature and about 280°C, is characterized by an almost constant particle diameter. Above this temperature (step two), the diameter increases quite drastically and reaches a steady state value (step three), between 380 and 500°C. Increasing the temperature further (step four), leads to a steady increase in diameter. This behavior is similar to the one of gallium droplets reacting with arsine to form GaAs [6].

The different steps can be attributed to the following processes. Step one is characterized by a suppressed evaporation of the indium particles due to the adsorption of phosphine molecules on the surface. Step two reflects the reaction between the indium droplets and the phosphine gas to form InP particles. The constant diameter in step three indicates that all indium in the particle has reacted and no further change to it seems to take place. The densities for Indium and InP at room temperature are 7.30 g/cm^3 [9] and 4.81 g/cm^3 [10], respectively. This difference in density can be transformed into a volume ratio between a particle consisting solely out of In and one where the In has reacted completely into InP. Assuming spherical particles, this volume ratio gives a diameter ratio of 1.25, the InP particle being the larger one. In our experiments diameter ratios between the room-temperature value and the value at step three in the diameter curve lay between 1.18 and 1.24, close to the calculated value.
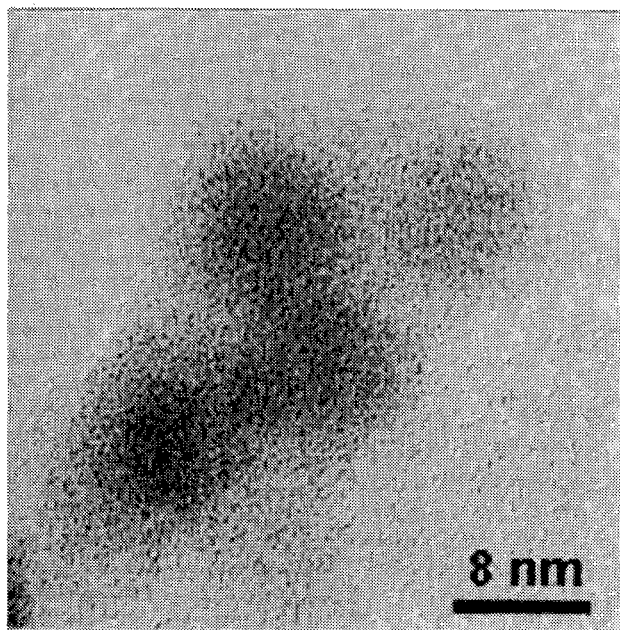
Fig. 3: Transmission electron micrograph of aerosol particles of indium after passing the reaction furnace together with 32 ml/min phosphine at a temperature of 153°C.

An increasing temperature leads to catalytic cracking of the phosphine molecule since indium, as well as InP, is pre-

sent in the furnace [11], which in turn is followed by an oversaturation of the gas with phosphorus. Some of this phosphorus will condense on the already existing InP particles when the aerosol leaves the hot zone. Thus, the particle diameter increases in step four.

This description of the reaction derived from tracing the particle diameter with reaction temperature and precursor flow is supported by the investigations made with electron microscopy. Almost all particles passing the furnace at temperatures below 300°C exhibit an amorphous structure and the composition is characterized as being mainly indium with some phosphorus. As indium metal has a low melting point (156°C), observations of such small particles in the electron microscope, due to the strong interaction of the electron beam with the particle, will melt or at least affect this type of particles. Fig. 3 shows an example of a TEM picture of such a sample.

The next step, the reaction itself, is difficult to follow by electron microscopy. Samples taken exhibit agglomerates of crystalline as well as of amorphous particles. Obviously, during the reaction process, some of the particles may react to form InP while other particles may pass the reaction zone without being reacted. This description is supported by a plot of the full width at half maximum of the size distribution versus temperature. This parameter exhibits a doubling of its value at the temperatures where the reaction takes place.
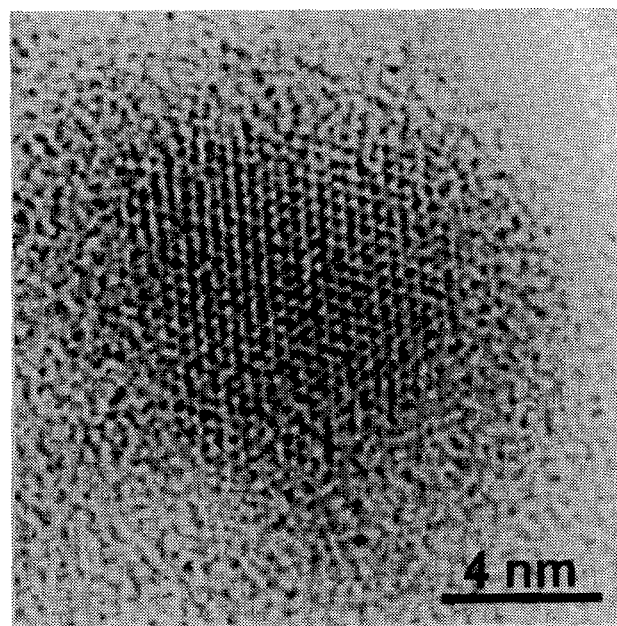
Fig. 4: Transmission electron micrograph of InP particles created by reacting indium aerosol with 8 ml/min phosphine at a temperature of 519°C.

After this reaction step a steady state situation is visible in the diameter development, with an almost constant value. Here, the electron microscopy reveals that the reaction be-

tween indium and phosphine is completed and thus the diameter is expected to be constant. However, recrystallization processes take place. For instance, 17 nm indium particles reacted with 8 ml/min phosphine are mainly amorphous at a reaction temperature of 422°C and are mainly monocrystalline at 519°C. Fig. 4 shows an example of such a particle reacted at 519°C.

It is possible to get electron diffraction from these particles as shown in Fig. 5. The diffraction pattern constitutes clear evidence that the particles created are InP. Furthermore, x-ray spectroscopy on such particles reveals their composition to be close to 50% In and 50% P.
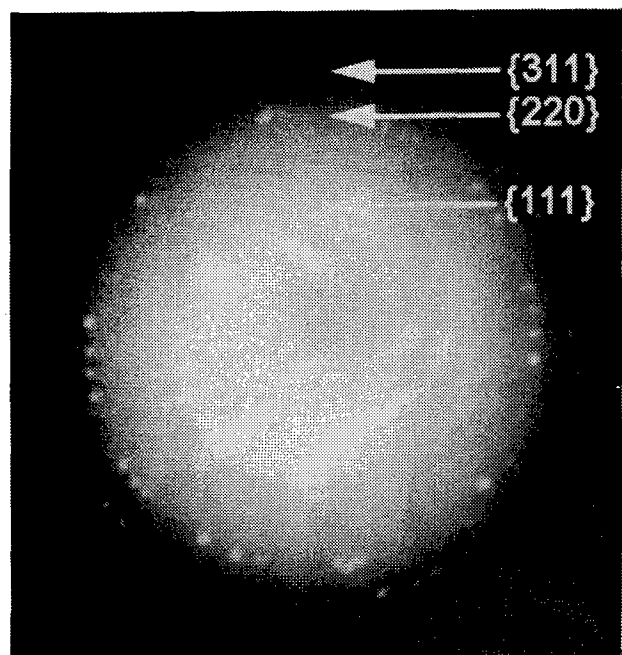
Fig. 5: Electron diffraction pattern of InP particles created by reacting indium aerosol with 8 ml/min phosphine at a temperature of 519°C.

No decisive electron microscopy observations were possible for particles created at even higher temperatures. The heavy decomposition of phosphine and the subsequent deposition of phosphorus on the sample grid makes a reasonable microscopy as well as interpretation of electron and x-ray diffraction patterns impossible.

IV. Conclusions

Using a new approach, aerotaxy, InP nanocrystals have been produced. This approach allows the fabrication of size-selected and contamination-free material. Investigations have been carried out concerning the evolution of particle diameter of the primary indium particles with reaction temperature and phosphine flow. This analysis leads to

a consistent picture and good understanding of the mechanisms involved. Investigations of produced nanocrystals by electron microscopy supports this picture.

Our approach opens the possibility to produce a sufficient number of size-selected semiconductor nanocrystals and it will allow new types of self-assembly and control of quantum dots.

Acknowledgments

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QUANTIZATION EFFECTS OF InGaAs/InP-QUANTUM WIRES GROWN ON PATTERNED SUBSTRATES

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Abstract

We fabricated $In_xGa_{1-x}As$ quantum wires on V-grooved InP substrates using low pressure metal organic chemical vapor deposition. The InGaAs layers were grown directly onto the patterned substrate forming single crescent shaped quantum wires in the groove tips. We applied transmission electron microscopy to reveal the structural properties of the samples and performed polarization and excitation dependent photoluminescence, and spatially resolved cathodoluminescence to examine the optical properties. Based on a comparison between optical measurements and an *eight-band $\vec{k} \cdot \vec{p}$* band-structure calculation we identified that nominally lattice matched grown wires are strained due to increased indium content of up to $x \approx 0.7$. The electron states are confined in the wire center and spatially separated from the hole states confined at the edges. The optical experiments unambiguously demonstrate the one-dimensional character of the quantum wires. Variations in the InGaAs layer thickness have strong impact on the optical properties.

I. Introduction

Large progress has been made in the growth of *in-situ* formed low dimensional quantum structures like quantum wires (QWRs) [1,2] and quantum dots [3]. However, work has been concentrated on GaAs based materials which are not suitable for long wavelength light sources emitting in the 1.3 to 1.55 µm range. Recently, we reported on InGaAs quantum wire structures *in-situ* grown by metal organic chemical vapor deposition (MOCVD) on V-grooved InP substrates either with InP barriers [4] or InAlAs barriers [5]. We found that on the V-grooved substrates depending on the position a strong variation in layer thickness and composition of the $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ occurred. An important unsolved problem with these structures is to minimize the planarisation of the V-groove tip during InP buffer layer growth in order to reduce the quantum wire width.

Here we report on large improvements of InGaAs quantum wire technology. The wires are now grown directly on the patterned InP substrates without buffer layer. We achieve the formation of defect-free crescent shaped QWR structures which unambiguously show a one-dimensional character.

II. Experimental

A. Substrate preparation and MOCVD growth

The nominally exactly oriented (001) InP:S substrates are patterned with fields (10 x 20 mm^2) of V-grooves aligned exactly to [1$\bar{1}$0] direction using conventional photolithography and wet chemical etching techniques [6]. The pitch is 5.0 µm and the groove opening is about 3.0 µm.

Before loading the patterned wafers into the MOCVD reactor the substrates are cleaned in an optimized procedure with HF (40%) and propanol. The MOCVD growth is performed in a horizontal quartz reactor on a rotating susceptor at a total pressure of 20 mbar. The total flow rate is 5.52 l/min. Trimethylgallium, trimethylindium, pure arsine and pure phosphine serve as precursors. Epitaxy starts with an annealing process at 710°C for 5 minutes in a phosphorous atmosphere. Subsequently the InGaAs layer is grown at 660°C onto the V-grooved InP:S substrate. We performed growth experiments with varying deposition time for the InGaAs layer. The structures were capped with an InP layer of nominally 35 nm in thickness.

B. Characterization

The structural characterization of the samples is performed by transmission electron microscopy (TEM). The optical properties are characterized by photo- and cathodoluminescence (PL, CL) spectroscopy. The PL measurements

are performed at 8 K with a Ge-diode for detection. For the excitation dependent PL we use an Ar$^+$-ionlaser with maximum excitation density of 500 W/cm^2. Due to the higher volume filling factor the InGaAs quantum wells on the ridges between the grooves dominate the spectra. To remove them we apply selective wet chemical etching. Then we compare as-grown and etched samples. For the low temperature (5 K) spatially resolved CL measurements we use an InGaAs reticon with 512 spectral channels for detection. We characterize the QWR samples in plan view and cross sectional configuration.

III. Results and Discussion

In Fig. 1 a cross sectional TEM image of an InGaAs quantum wire with InP barriers is shown. The InGaAs layer was grown nominally lattice matched. The total wire width is 180 nm. The thickness of the wire is 8.2 nm in the center and decreases down to 3 nm on the sides. No dislocations and defects are visible in the TEM image. A comparison of quantum wire structures grown with a low temperature InP buffer layer (as outlined in [4]) and quantum wires grown with no buffer layer surprisingly show that the integrated PL intensity is nearly the same. Up to now the use of a buffer layer has been found to be mandatory in MOCVD to create an acceptable interface for deposition of the active layer. Obviously the interfaces are of identical quality in our both approaches for the QWR growth.
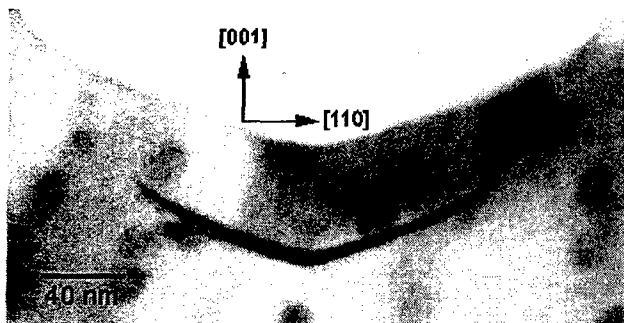
Fig. 1: Cross sectional TEM image of InGaAs/InP quantum wire grown into V-grooves on InP:S substrate. The wire thickness is 8.2 nm in the center and decreases with width down to 3 nm.

In the TEM we find that the InP substrate reveals {114}A facets in the V-groove tip before deposition of the InGaAs layer starts. In experiments we verified that these crystal planes are formed during the cleaning procedure with HF and that a planarization due to substrate annealing at 710°C is not observable. We know that sensitive variations of the cleaning process parameters have an impact on the width of the newly developed planes. Particularly the HF etching time should be reduced to avoid a widening of the groove tip.

In the PL experiments luminescence from QWRs and from quantum wells (QWLs) on the ridges between the grooves and on the groove side walls occur (Fig. 2). We unambiguously
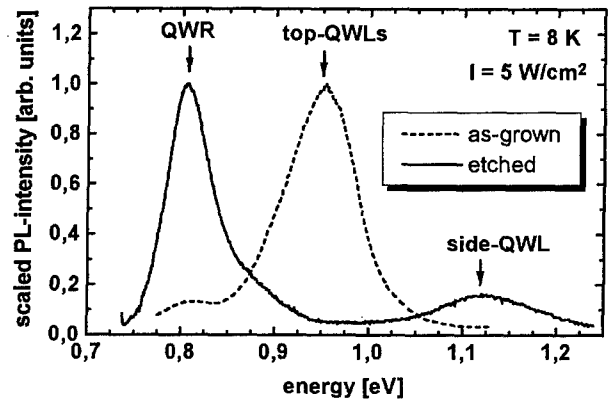
Fig. 2: Scaled low temperature PL spectra of InGaAs/InP-quantum wire structure. We observe luminescence from quantum wires, ridge quantum wells and sidewall quantum wells. Absolute luminescence from quantum wires is nearly constant in as-grown and etched sample

assign the peaks using spatially resolved CL measurements [7]. The luminescence in the spectra is dominated by the ridge quantum wells. At the emission maximum of 1.125 eV a broad luminescence is observable which we assign to the QWLs on the {111}A side walls. These side-QWLs are thinner than 1 nm and therefore not visible in TEM images. The broadening is a sign for thickness modulations resulting from the strain due to a large lattice mismatch on the {111}A planes. This effect is comparable to the case of pseudomorphic InGaAs QWRs grown in AlGaAs/GaAs V-grooves [8]. The emission from the QWLs on the ridges occurs with maximum intensity at 0.954 eV. We observe luminescence from the InGaAs layers on (001) plane and on the groove edges which are {113}A facets. Both InGaAs QWLs are lattice matched and have different thickness. The emission maximum of the QWR luminescence occurs at 0.807 eV (FWHM = 58 meV) using 5 W/cm^2 photo-excitation. The absolute intensity is nearly the same in the etched and as-grown samples showing that transport via side-QWLs is negligible. This is also confirmed by CL measurements. Line-shape analysis shows that the QWR emission has three constituents which are assigned to transitions from different conduction band states into excited hole states. The lowest energy QWR emission occurs at 0.76 meV but is a factor 100 less intense than the recombination from $n_{CB} \geq 3$ conduction band states and is only observable for excitation higher than 5 W/cm^2. Transitions with excited electrons ($n_{CB} \geq 5$) occur with maximum emission at 0.85 meV.

Using an eight-band k•p band-structure calculation (as outlined in [9]) we find that the indium content in the In$_x$Ga$_{1-x}$As QWR is x = 0.70 ± 0.02 [7]. Thus the QWR is compressively strained ($\Delta a/a$ = -1.2%). Due to the strain-induced band deformation and the existence of a strong piezoelectric field we find that the electron and hole ground-states are spatially separated in the QWR and show very small
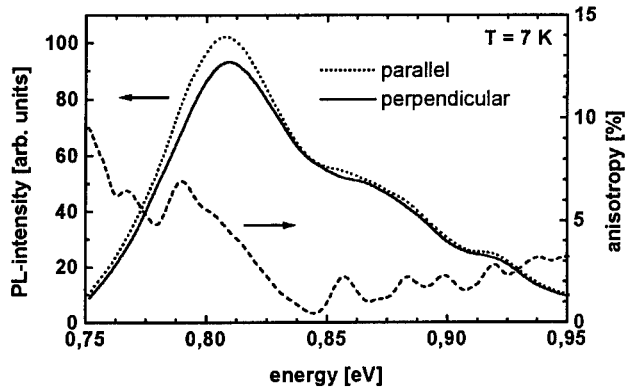
Fig. 3: Low temperature polarization dependent PL of InGaAs/InP QWRs. The linearly polarized PL measured parallel to the wires (dotted line) and perpendicular to wires and to the growth direction (solid line) shows an anisotropy of ≤ 10% (dashed line).

overlap. The electron ground state is confined in the groove center and the hole ground state is repelled from the QWR center. Therefore ground-state luminescence is not dominant here. Our theory predicts all observed PL features with high accuracy.

Moreover we measured in a polarization dependent PL experiment (Fig. 3) an anisotropy of light linearly polarized parallel and perpendicular to the QWRs [7]. This is a further indication for the one-dimensional character of this nanostructure. The degree of anisotropy is ≤ 10%, indicating a strong valence band mixing.

To examine the influence of a reduced InGaAs layer thickness we performed experiments with decreased InGaAs deposition time under otherwise identical growth conditions. We assume a reduced center thickness of the QWRs if a
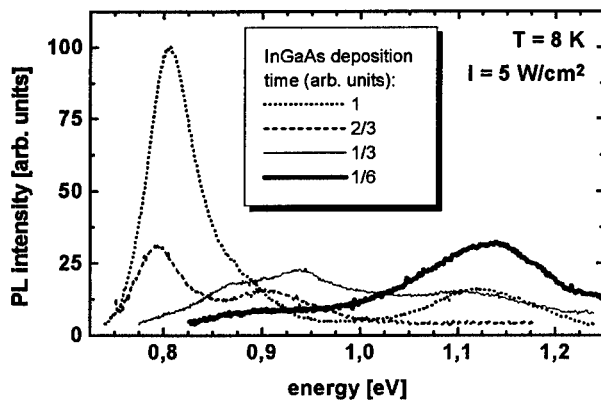
shorter InGaAs deposition time is used during QWR formation. Since the growth in V-grooves cannot be compared to epitaxy on planar substrates the resulting thickness must not necessarily be linear in deposition time. From this reason we note the growth time for the InGaAs layer in arbitrary time units scaled to the time used for the QWRs shown in Fig. 1. Comparing the PL results for four QWR structures with varying InGaAs deposition time we find a strong impact (Fig. 4). Using multiple Gaussian line-shape fits for the spectra we find for the QWR with growth time 2/3 three PL emission maxima at 0.792 eV, at 0.834 eV and at 0.901 eV. For a layer using 1/3 growth time we observe maximum PL emission at 0.818 eV, 0.880eV and 0.935 eV. If we apply the shortest deposition time in this experiment (factor 1/6) we observe PL from the most low-energetic constituent at 0.880 eV. The higher energy parts of this spectrum cannot be resolved due to the strong superposition of side-QWL luminescence. The PL results for the four QWR samples are visualized in (Fig. 5).
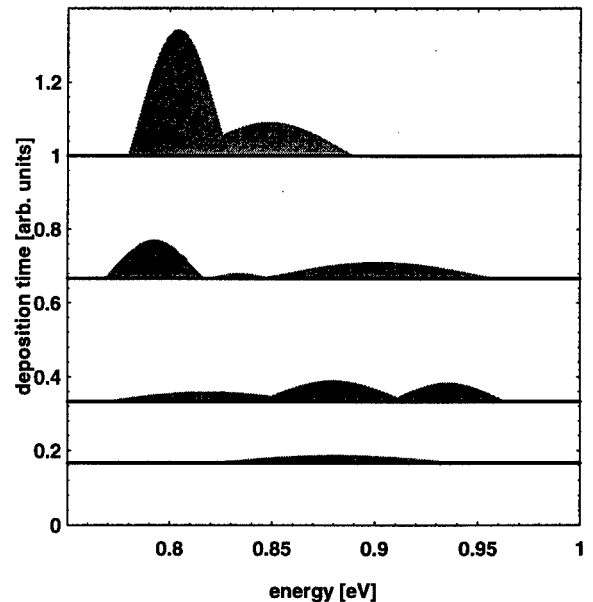
Fig. 5: Decomposition of the QWR PL (5 W/cm² photo-excitation) into Gaussian components determined by line-shape fits, for different InGaAs deposition times. The height of the peak icons indicate their relative intensities, and their base line widths are the FWHM of the respective Gaussians. Each Gaussian stems from an ensemble of different radiative transitions, and each ensemble is attributed to a respective set of conduction band states involved into the transitions. In our experiment single lines are not resolved.

Fig. 4: Low temperature PL of InGaAs/InP QWRs grown under identical conditions with varying InGaAs layer deposition time. The ridge-QWLs were selectively removed. Growth time of one time unit results in the layer shown in Fig. 1.

IV. Summary

We fabricated crescent shaped $In_xGa_{1-x}As$ QWRs by selective growth on InP V-grooves with varying InGaAs layer thickness. The wire width is 180 nm. Depending on the

InGaAs deposition time the center thickness is 8.2 nm or lower. Comparing optical measurements and an eight-band k•p band-structure calculation we found that the QWRs are compressively strained since the indium content is up to x ≈ 0.70. The strain field and the resulting piezoelectric charging impact the band structure so that in the thickest QWR sample the electron states are confined in the wire center and the hole states are repelled from this region. Reduction of the InGaAs thickness results in higher QWR recombination energy and a drop in PL intensity.

V. Acknowledgments

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OBSERVATION OF SPINODAL PHASE SEPARATION AND QUANTUM DOT FORMATION IN InGaAs/GaAs LAYERS GROWN AT DOWN-RAMPED GROWTH TEMPERATURES

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Introduction

We observed spinodal phase separation in $In_xGa_{1-x}As$ layers grown on GaAs substrates at decreasing growth temperatures. The phase separation results in quantum-wire like structures for high In content ($x \approx 0.2$) and low rates of temperature decrease (0.1 °C/s). With faster rates of temperature decrease (0.3 °C/s) and a decreased In content ($x \approx 0.03$) formation of island-like structures is observed. The islands show photoluminescence emission of high intensity and comparatively narrow linewidth ($\approx$ 30 meV) [1]. Calorimetric absorption spectroscopy (CAS) was carried out at T = 500 mK, where particularly high sensitivity is realised, in order to confirm confinement of carriers in these structures.

I. Experimental

All samples were grown in a low pressure (76 torr) horizontal quartz reactor using TMGa, TMIn, and AsH_3 as source materials and hydrogen as carrier gas with a total flow rate of 9 litre/min. Growth was carried out on exactly oriented (001) GaAs and on substrates with 2° off orientation towards (011). InGaAs was deposited at temperatures that were lowered from the initial temperature (500°C or 550°C) by 50°C or 100°C, with temperature decrease rates of 0.1°C/s or 0.3°C/s. In reference samples, where both InGaAs and GaAs were grown at a fixed temperature, no significant phase separation can be observed. The composition of $In_xGa_{1-x}As$ was nominally x=0.03 or x=0.2. From XPS measurements the In-content of the dots is estimated to be x≈0.4 (for a nominal In content of x=0.03). For AFM studies the growth was interrupted after 10-20 nm and the samples were cooled down under arsine pressure. The surface of these samples was subsequently etched in order to turn the compositional differences in the epilayer into a detectable relief.

Fig.1(a): AFM image of InGaAs layers grown with a temperature decrease rate of 0.1°C/s (growth temperature: 500-450°C) on a (001) GaAs substrate with 2° off orientation. The height range (from black to white) is 8 nm.

II. Results and Discussion

Fig. 1 shows AFM images of a structure in which $In_{0.2}Ga_{0.8}As$ was grown with a rate of growth temperature decrease of 0.1 °C/s on a substrate with 2° off orientation. The surface features a wire-like morphology where the wires are oriented along the surface steps of the vicinal substrate in the <100> direction. The image in Fig. 1(b) shows a magnification of the hill and valley structure.

Fig.1(b): AFM image of InGaAs layers grown with a temperature decrease rate of 0.1°C/s (growth temperature: 500-450°C) on a (001) GaAs substrate with 2° off orientation.

Shown in Fig. 2 is the surface of a sample grown under similar conditions, except that a substrate without off orientation was used. The hill-and-valley structure forming on the planar substrate clearly shows preferential orientation along the 'soft' <100> direction [3]. Fig. 3 (a) shows an AFM image of a structure with a nominal In content of $x=0.03$, grown with a rate of temperature decrease of 0.3 °C/s. The surface shows islands with an average diameter of 22 nm and an area density of $\approx 2 \times 10^{10}/cm^2$. The cross sectional HRTEM in Fig. 3 (b) shows a highly coherent single quantum dot in GaAs matrix.
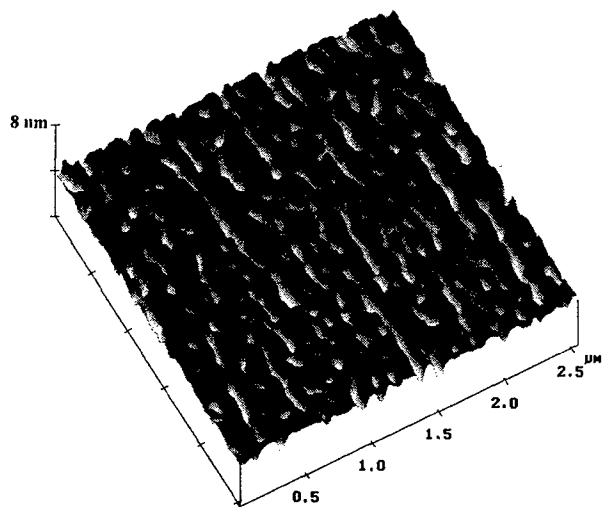
Fig.2: AFM image of InGaAs deposited under similar conditions as the sample shown in Fig.1, on a substrate without off orientation. The height range is 8 nm.

(a)

(b)
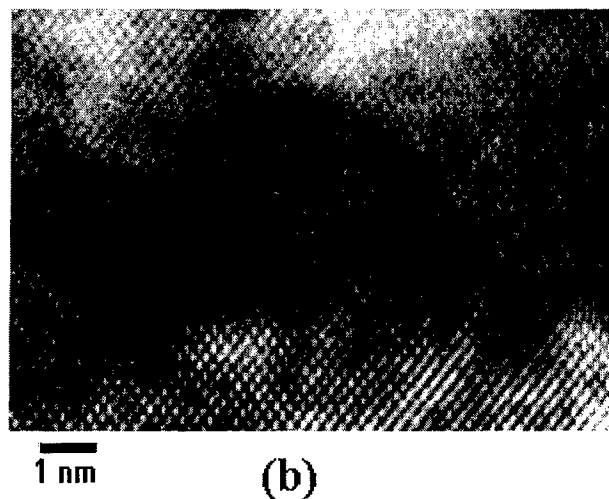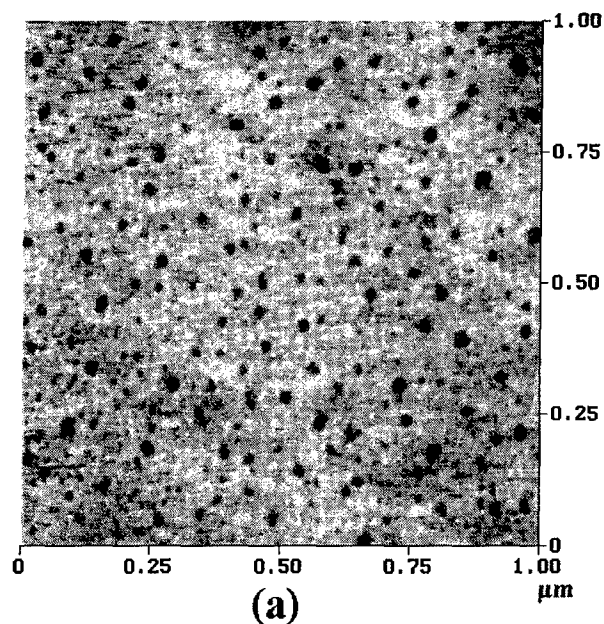
Fig.3: (a) AFM image of quantum dots formed by spinodal phase separation. The height range is 6 nm. (b) HRTEM cross section of a single dot.

The occurrence of phase separation in $In_xGa_{1-x}As$ layers where the In content is as low as $x=0.03$ is very surprising since thermodynamic calculations do not indicate a miscibility gap for the investigated growth temperatures. The morphology of temperature-gradient grown layers points to the existence of a spinodal type of reaction at the growth interface [2, 4], indicating a change in the phase diagram for InGaAs grown at decreasing temperatures. It is assumed that lowering the temperature during epilayer deposition induces an enhancement of the surface diffusion. Phase separation was

88

observed to have a much lower activation barrier for surface diffusion as compared to bulk diffusion, leading to spinodal decomposition at the surface even far above the bulk miscibility gap temperature [4]. The potential for quantum dot formation by spinodal phase separation could well be present also in other semiconductor alloys and is suggested as a promising avenue for the realisation of zero-dimensional carrier confinement.

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Molecular Beam Epitaxial Growth of Quantum Wire Heterostructures Using (GaP)$_x$/(InAs)$_y$ Short Period Superlattices on InP

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Semiconductor quantum wires (QWR) are of great interest for their theoretically predicted advantages over the current quantum well (QW) technology. We report the application of the strain-induced lateral-layer ordering (SILO) process to a novel material system, spontaneously creating GaInAsP QWRs *in situ* on InP. Through molecular beam epitaxy, combinations of short-period superlattice (SPS) constituents are deposited on the growth surface. The two constituent layers each are strained with a force nearly equal in magnitude but opposite in direction (tensile/compressive) with respect to the host lattice. Thus, the strain forces compensate one another and the overall mismatch of the SPS is near zero. Due to the localized strain effects however, lateral composition modulation in the growth plane occurs, resulting in lateral quantum wells. Carrier confinement in the standard transverse growth direction, coupled with the lateral confinement, yield the two-dimensionally confined QWRs. In this study, pairs of (GaP)$_x$/(InAs)$_y$ SPS were grown in the QWR region on an InP substrate, using elemental group III and hydride group V sources. The transverse barriers consisted of InP. Initial growth condition studies, where the substrate temperature was varied from 480 to 520°C, revealed room temperature photoluminescence (PL) emission around ~1.57 μm (Fig. 1(b)) using 6 pairs of (GaP)$_1$/(InAs)$_{2.2}$ SPS. Evidence of the QWR formation is supported by the spectra observed through polarized photoluminescence at room temperature. The amount of polarization was seen to decrease as the growth temperature was increased. This trend is explained due to the fact that the higher temperatures will increase the overall mobility of the surface atoms, tending to slightly disorder the alloy and counteract the lateral composition modulation induced by the strain forces. The wavelength emission for the QWRs grown at 500°C shifted from 1.582 μm (0.7837 eV) for measurement at 300 K to 1.52 μm (0.8157 eV) at 77 K, for a net shift in emission of 32 meV. This shift is almost half that observed for a typical InGaAs/InAlAs QW, which could yield devices with more stable emission wavelength versus operating temperature. Additional experiments with different SPS pair compositions and thicknesses have resulted in varying the PL emission wavelength. QWRs using 4 pairs of (GaP)$_1$/(InAs)$_{1.95}$ (Fig. 1(a)) demonstrated polarized emission near the 1.16 μm wavelength. This method of applying the SILO process with (GaP)$_x$/(InAs)$_y$ SPS on InP is a viable and novel method for fabricating QWRs with emission wavelengths in the technologically important 1.1 to 1.6 μm range.
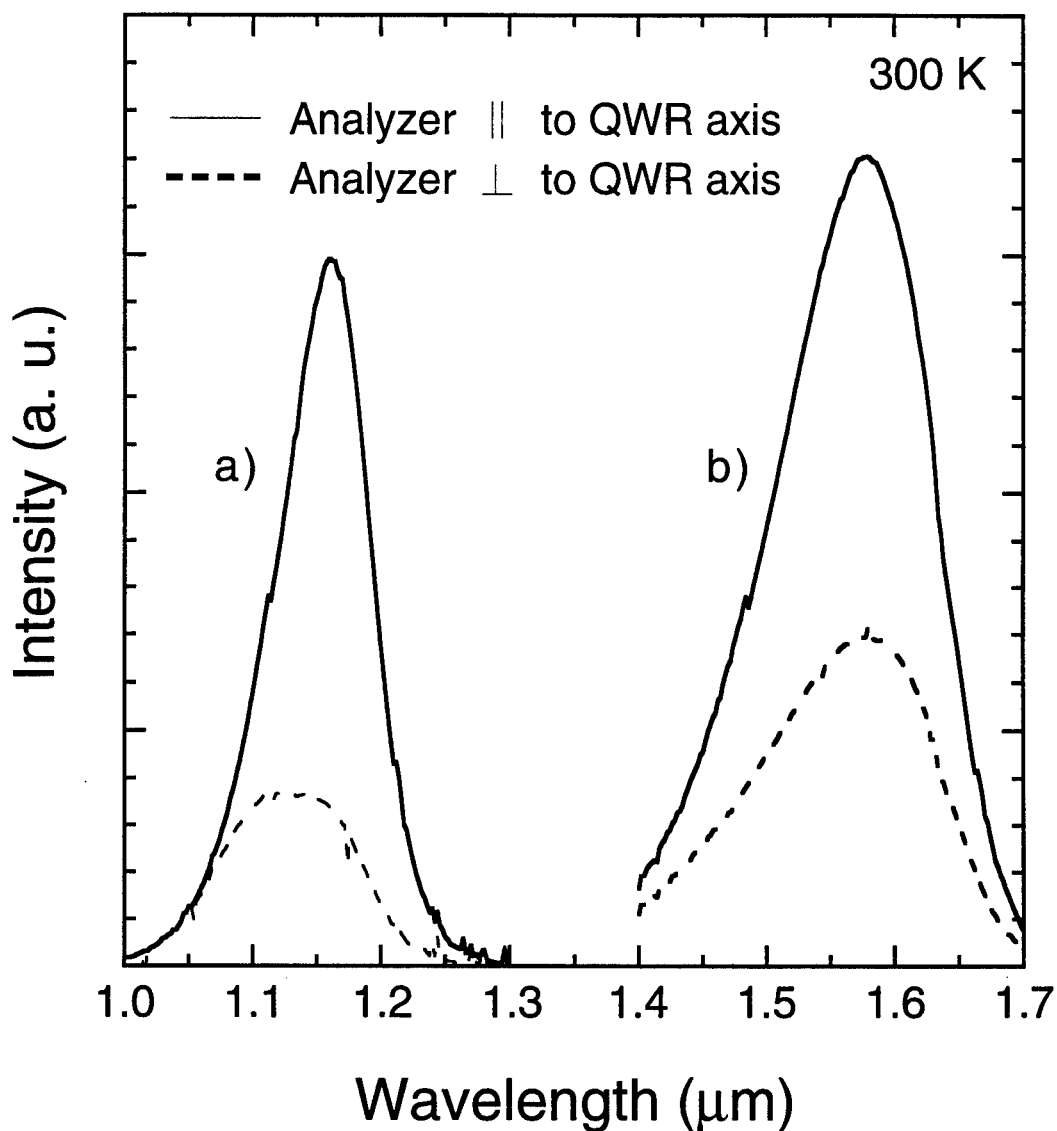
Figure 1. Polarized photoluminescence spectra of short period superlattice quantum wire (QWR) structures consisting of a) 4 pairs of $(GaP)_1/(InAs)_{1.95}$ and b) 6 pairs of $(GaP)_1/(InAs)_{2.2}$ on InP using InP transverse barriers. For the polarized measurements, the axis of a rotatable polarization analyzer was aligned either parallel or perpendicular to the QWR axis. The growth temperature was 500 °C.

DIRECT CALCULATION OF TUNNELING CONDUCTIVITY PROFILES OF NOVEL InP/InGaAs SUPERLATTICE STRUCTURES, BY MEANS OF THE GREEN'S FUNCTION

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Introduction

We propose a first principles method of calculating the tunneling conductivity of superlattice (SL) InP/In(x)Ga(1-x)As structures. The method we follow is based on the generalized Kubo-greenwood formulation and on the causal form of Green's function. The perpendicular (along the growth direction) conductivity, involves a group of parameters directly connected to the geometry of the device (hence upon one's disposal), such as (I) quantum well width (II) potential barrier thickness and (III) selective doping of potential barrier regions in order to increase carrier collection and pin the Fermi level within the minibands. Such an alignment provides a tunneling transport from layer to layer, making the barriers potentially transparent for the electrons, thus increasing the tunneling conductivity.

I. Background

In this paper a method of calculating the perpendicular conductivity is proposed. InP/InGaAs modulation doped hetero-structures have emerged as excellent systems for the design and fabrication of field effect transistors. A lesser known quantity of interest is the tunneling conductivity in such structures. The multilayer nature of these structures offers advantages in transport properties, by essentially making the carriers free along the growth direction of the field effect device. Quantum size effects are explored by selection of *thin* layers of wide gap material grown on top of a narrow gap material, in the sense that it offers another degree of freedom for the carriers, namely, freedom in tunneling through the layers. Thin layers of wide gap material (InP) grown on narrow gap material (In(0.53)Ga(0.47)As) form a sequence of quantum wells. (1) We explicitly derive the conductivity $\sigma(T)$ primarily as a function of temperature T, by means of the Green's function for superlattice structures (2) We explore the variations of conductivity for various repeat distances at fixed temperatures and (3) we find that the conductivity is greatly enhanced and reaches an average maximum level above 12 periods. The conductivity of the carriers is calculated by means of the Green's function $G[E(k_z)]$, where k_z and $E(k_z)$ (discussed later) are the wave vector and the energy dispersion relation of the superlattice structure respectively. In section II we present a detailed calculation of $\sigma(T)$. The derived conductivity formula besides the temperature T, includes a number of "band-gap engineering" parameters, namely, the repeat distance of the superlattice, the width of the minibands, and the pinning of the Fermi level within the quantum wells. The latter is a very

convenient feature for such device design, since it provides to the electrons an essentially free tunneling path through the otherwise impenetratable thin barriers. In reality the wavefunctions of the trapped electrons in the quantum wells overlap, thus providing communication channels from [superlattice] cell to cell. Section II deals with the derivation of the DC conductivity of the superlattice structure. In section III, numerical results are presented at fixed dopings and layer thicknesses for the InP/In(0.43)Ga(0.47)As novel heterostructure. Conclusions and insights are in section IV.

II. Calculations

The real part of the DC conductivity is given by the generalized Kubo-Greenwood formula [1] and is:

$$\sigma_{zz}(T) \equiv 2e^2 \frac{\hbar}{\pi\Omega} \int dE(\ \partial f(E)/\partial E) \times$$

$$\Sigma |\langle k_z| \frac{P_z}{m} |k_z\rangle|^2 |ImG^+(E,k_z)|^2 \qquad (1)$$

The sum is over the discrete spectrum of k_z, which is the wave vector of the superlattice structure, defined by the superlattice Brillouin zone : $-(\pi/d) < k_z < (\pi/d)$ [2], and bound by Born-von Karman conditions [3], d is the repeat distance (period) of each superlattice-cell with N superlattice periods. P_z is the momentum operator, m is the mass of a carrier, and f(E) is the Fermi-Dirac (F-D) distribution function. Since

$$\langle k_z| \frac{P_z}{m} |k_z\rangle \equiv \frac{1}{\hbar} \frac{\partial E(k_z)}{\partial k_z} \qquad (2)$$

For moderate dopings F-D distribution is

$$f(E) \cong \exp\frac{E_F - E}{kT} \qquad (3)$$

Also, the imaginary part of the Green's function is

$$|ImG^+(E,k_z)|^2$$

$$((E - \Sigma_1 - E(k_z))^2 + \Sigma_2^2)^2 \qquad (4)$$

where in (4) the imaginary part of the Green's function is given in terms of the self energy of the carriers, and the energy dispersion relation of the superlattice. Inserting (2), (3) and (4) in (1) and in the weak scattering limit [1,3] one obtains

$$\sigma_{zz}(T) \cong 2e^2 \frac{\Sigma_2^2}{\pi\Omega\hbar} \gamma^2 d^2 \beta \times$$

$$\Sigma \frac{\sin^2(k_z d) \int dE \exp(\beta(E_F - E)}{(E - E(k_z))^4} \qquad (5)$$

where β is the temperature factor equal to 1/kT. The dispersion relation is [4]

$$E(k_z) \equiv E_n + \gamma_n \cos(k_z d) \qquad (6)$$

γ_n is the miniband width which is calculated from tight-binding overlap integrals [5]. E_n is the nth miniband energy level n the quantum well.

93

We impose the following condition: We want the Fermi level to be pinned within one of the miniband levels in the quantum wells. Given that the system under consideration, InP/In(0.53)Ga(0.47)As, is comprised of narrow wells and barriers, one may expect tunneling through the minibands E_1 and E_2 ($E_2 > E_1$, relative to the bottom of the wells). In the tight-binding approximation E_2 is wider than the E_1 miniband, and by imposing the condition mentioned above we restrict the tunneling process in the E_2 energy zone, thus making the hetero-layers in essence transparent . In this case tunneling through E_2 dominates and having this in mind condition (5) may accept the following replacement: the Fermi level is replaced by the band energy E_2, which is the second energy level in the quantum wells. It is up to the designer's disposal [6] to select the appropriate doping and the rest of the superlattice parameters. In fact, in this specific case, the InP/InGaAs alloy is assumed to be having a sequence of quantum wells with a conduction band step at 210eV [7]. Moderate doping levels are assumed to be at ~5 x 10^{18} cm^{-3}, while the energy miniband E_2 is at ~ 42meV within the quantum well, measured from the bottom of it. The spread of the miniband is taken at ~4-5meV, and the numerical integration is done over this spread, where tunneling is expected to dominate.

The prefactor of the conductivity includes beyond the temperature factor kT, the spread of the minibands, the superlattice periods the imaginary part of the self energy and a normalizing volume, which is the volume of the device region where the tunneling takes place. The repeat distances d are comprised of well widths d_1 and barrier widths d_2 at 50A and 25A respectively.

III. Results

Starting from (1) we derived a satisfactory result for the tunneling conductivity of a device that includes an active superlattice region, and along the growth direction. Fig. 1 shows the variation of the normalized conductivity (in arbitrary units a.u.) as a function of temperature from about 50K to 300K. The number N of the repeat distances is N=5, at well/barrier ratios at 50A/25A. The conductivity increases in a rather smooth way resembling I-V characteristics of multilayered devices. Relying upon a relatively weak scattering limit, the overall pattern makes sense if one takes into account that the carriers become more energetic as the temperature increases. If the number N of the superlattice periods increases, the general form-response of the tunneling conductivity is not dramatically changed. In Fig. 2 we see the same type of response, but now the number of periods has been increased to 7 , and for the same device geometry. The conductivity profiles remain the same. Fig. 3 depicts a similar to the previous situation, with N=11 periods. Comparing the three results at 300K we observe a substantial increase from N=5 to N=7 periods (i.e. from 0.7 to 1.35a.u.), and a 5% increase from N=7 to N=11 periods. In spite of any "gray" points in the numerical process of evaluating the conductivity, it seems that σ(T) stabilizes at about 1.4 (a.u.) at 300K, and for N above 11 periods. Further numerical calculations show that as N increases far above 11, stability of (normalized) conductivity values is achieved. Recalling that a superlattice cell was taken at 75A ($d_1 + d_2 = d$), it seems that a stabilization of maximum conductivity is expected at hetero-structure thicknesses above 83nm.

Conductivity with number of Periods N=5

Fig. 1. σ (T) vs T, N=5 periods

Fig. 2. σ (T) vs T, N=7 periods

Conductivity with number of Periods N=11
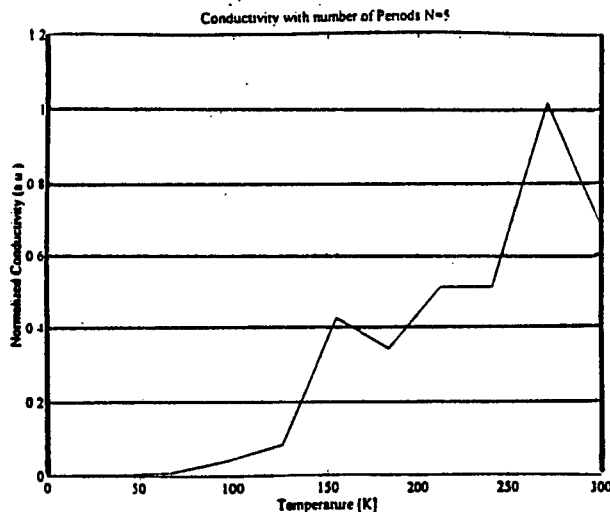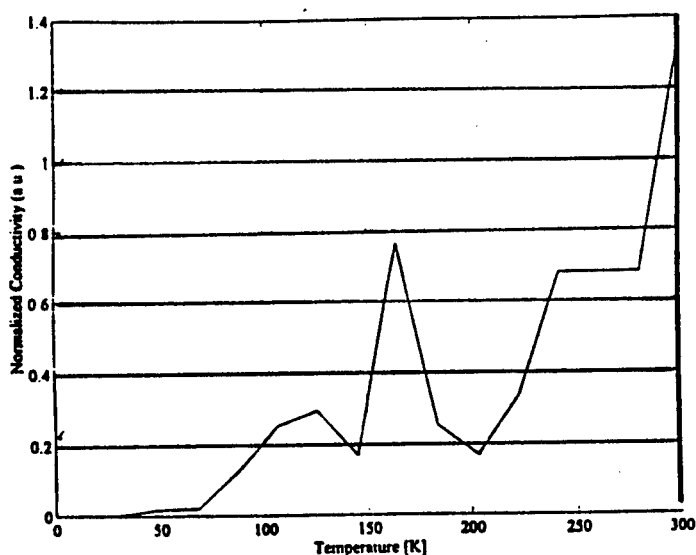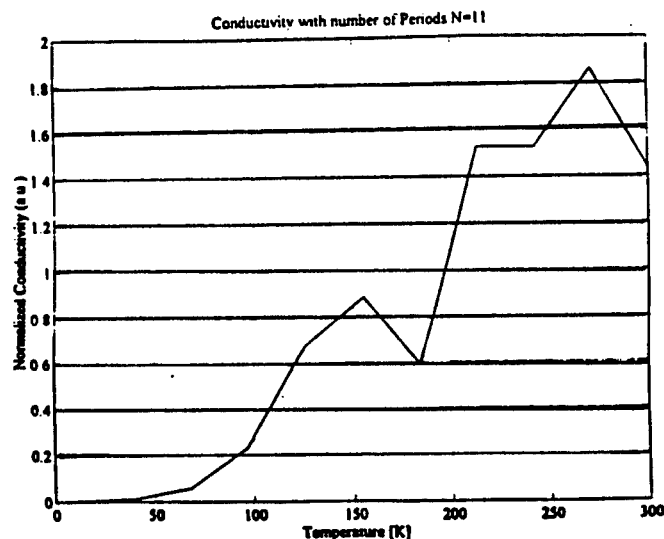
Fig. 3. σ (T) vs T, N=11 periods

IV. Conclusions

We have presented a first principles method of calculating the tunneling conductivity of superlattice (SL) structures. We have selected a specific InP/InGaAs alloy structure where quantum size effects are pronounced dramatically. Appropriate geometry of the SL active- region of a FET-like device allows tunneling of carriers through potential barriers. It is found that the *normalized* (a more thorough discussion of the prefactor is under study) *conductivity* is increasing with temperature, in the weak scattering limit, and for moderate dopings. A task to probe further is under way, namely, to generate I-V curves of novel SL-FET devices.

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CUBIC PHASE GALLIUM NITRIDE EPITAXIALLY FORMED ON GaAs OR GaInAs AT LOW TEMPERATURE WITH A NH3 DECR PLASMA

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Introduction

GaN is a compound semiconductor attractive for its blue band gap (3.45 eV) and its large saturated electron drift velocity.Unfortunatly, because of its large ionicity, GaN condense in the Wurtzite structure. It has been shown, that it was possible to obtain an epitaxial zinc blende structure using an appropriate growth technics(1,2).
In this paper it is shown that a simple interaction of a NH_3 DECR Plasma with a GaAs or InGaAs surface can result in a surface transformation in which an important amount of nitrogen is incorporated at the place of the As, leading to the formation of epitaxial cubic nitrides. The temperature of the treatment is as low as 450°C for GaAs and 220°C for GaInAs. X- ray difffraction, AFM and high resolution TEM are utilized to analyse the growth process.

I) Background

GaN is one of the most promising wide band gap material for micro as well as optoelectronic applications.One of the most severe drawback in the fabrication of thin nitride films is the requirement of very high temperature to obtain them through a pyrolitic CVD process. Typical deposition temperature of GaN has been reported to be 1000°C using NH3 as a nitrogen source (3,4). A lower growth temperature is obtain with MOCVD when dimethylhydrazine is used for the nitogen source (5).The use of a plasma- assisted molecular beam epitaxy to grow epitxial cubic phase GaN on GaAs has also been reported (1). In this paper it is not proposed a growth technic but a surface modification one. The column III element is provided by the surface etching of the substrate by an amonia DECR plasma, the nitrogen being formed at the same time. Both GaAs and GaInAs surfaces have been studied resulting in GaN and GaInN formation.

II) Experimental

In previous studies, it has been shown that the surface of GaAs and GaInAs could be treated under a NH3 plasma flow for passivation purpose (6). The plasma reactor is a Distributed Electron Cyclotron Resonant Multipolar Microwave Plasma (DECR). The reactor concept is based upon the use of several microwave applicators working at the ECR mode along the multipolar confinement magnet. This confinement decreases the electron temperature to about 5eV and increases the ion density to about $10^{10} cm^{-3}$. The resulting treated surface showed a clear native oxyde reduction, an As loss and a nitrogen pick up. This has been illustrated with an Auger analysis reported in reference (6). This surface reaction can be driven further with an increase in plasma energy and/or a increase of substrate temperature. In this case it is obseved that GaN is epitaxially formed on GaAs where as GaInN is formed on InGaAs layers epitaxially grown on InP. These nitrides have been studied to understand their growth mechanism and try to control the epitaxial cubic phase growth with reduced damage induced plasma processing. For this purpose X-ray diffraction, Atomic Force Microscopy (AFM) and high resolution TEM analysis were performed.

III)GaN Growth on GaAs.

A NH_3 plasma is formed at the surface of a (100) semi insulating GaAs substrate at a pressure of 5mTorr, and a substrate temperature of 450°C. A plasma power of 400 and 1200 Watts have been utilized and a treatment time varying from 15 to 30 minutes. Zinc blende GaN is formed at the surface of GaAs as can be seen by X-ray diffraction pattern and high resolution TEM. The X-ray diffraction pattern of a sample treated at 400W for 30 min is shown in figure (1). Close to the (002) réflexion peak seats a well defined peak attributed to GaN with some traces of As. From this peak, it is possible to calculate a lattice parametter of 4.6Å and with Vegard's law a nitrogen composition of more than 90%. A high resolution cross section analysis of this sample is shown in figure (2a). Evidence of the presence of two cubic networks is seen in the moire pattern resulting from the interference of the diffracted electrons from the two
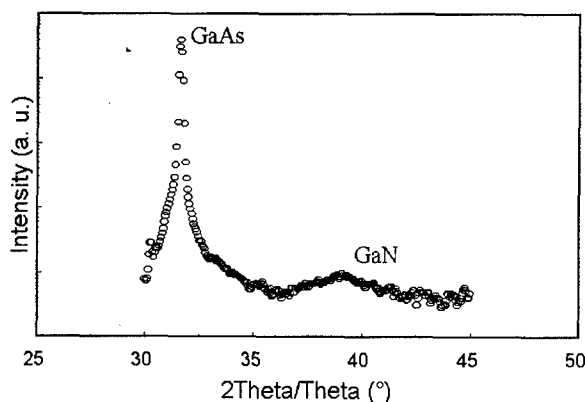
Figure 1 : X-ray diffraction pattern from the surface of a GaAs sample treated with an amonia plasma of 400W for 30min. Epitaxial cubic GaN is clearly seen.

(1a)
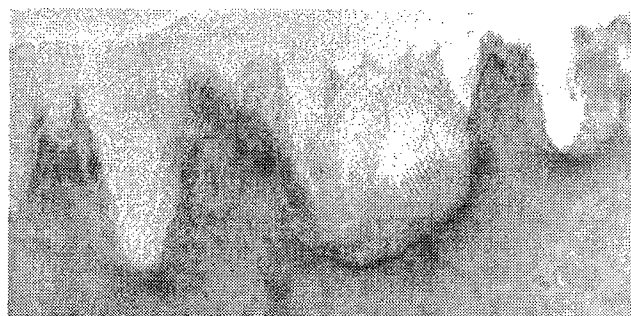
(1b)

Figure 2 : High resolution cross section TEM micrographof a GaAs surface treated with an amonia plasma of a) 400W/30min or b) 1200W/30min

cubic networks. The surface is covered relatively uniformly and the rugosity created by the plasma etching is on the order of 80 Å. When the plasma power is set to 1200W, the surface damage are more important as shown in the TEM micrograph of figure (2b). The resulting rugosity (peak to peak) is on the order of 250Å. If the power is set back to 400W and the time of interaction reduced to 15 min, the surface is then represented in the AFM picture of figure 3, were the mesured rugosity is about 30Å. In that case the epitaxial coverage is not uniform.
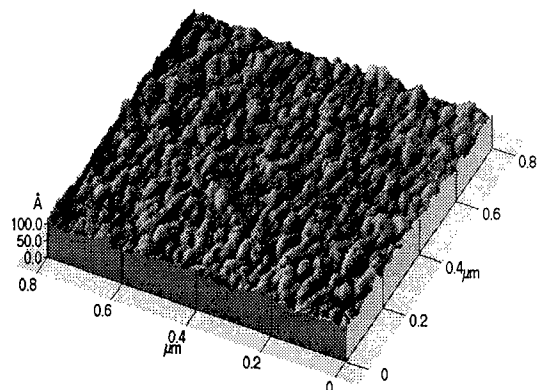
Figure 3 : AFM micrograph of the surface of a GaAs substrate treated in an amonia plasma of 400W for 15 min.

IV) GaInN Growth on GaInAs

A lattice matched GaInAs layer grown on an InP substrate was introduced in the plasma reactor. The power was set at 400W, the pressure at 5 mTorr, the substrate temperature was reduced to 220°C and the interaction time was set between 1 and 5 min. Above any of these specification the layer would be visually damaged. The result appear in figure 4 to 6. In figure 4, the X-ray analysis of the 400W/5min treatment, clearly shows the formation of a cubic GaInN layer epitaxially grown on GaInAs that coexists with another peak that could not be identified. The high resolution cross section TEM micrograph of figure5 shows the existance of an epitaxial coverage on the top of GaInAs. The lattice parameter of this material is coherent with $Ga_{0.5}In_{0.5}As$. One can also observe non epitaxial growth, that could be attributed to non cubic nitride material. Finally AFM studies were carried out on 400W/5min and 400W/2min treated GaInAs surfaces. The micrographs are shown in figure 6. From the 2min exposure surface it is possible to observe an etching that has just started with a nitride growth that nucleates in the etched holes. After 5min (figure 6a) the InGaAs is uniformely etched and only nucleated nitride domes are observed.

V)Conclusions

The interaction of GaAs and GaInAs with a DECR amonia plasma has resulted in epitaxial cubic nitride formation at amazingly low temperature. The mechanism

97

6a)
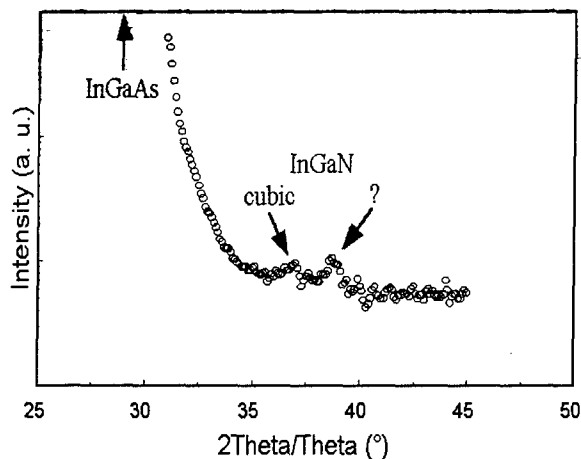
Figure 4 : X-ray diffraction pattern from the surface of a GaInAs sample treated with an amonia plasma of 400W for 5min. Epitaxial cubic GaInN is clearly seen, with another material that could not yet been identified

6b)

Figure 6 : AFM micrograph of the surface of a GaInAs surface treated in an amonia plasma of a)400W/5 min.and b)400W/2min

Figure 5 : High resolution cross section TEM micrographof a GaInAs surface treated with an amonia plasma of 400W/5min. Epitaxial and non-epitaxial crystalline material are observed.

of growth are still under investigation but they are clearly associated with the etching process

VI)Acknowledgements

VII)Référence

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Improvement of self-organized quantum wire structures formed in $(GaP)_n(InP)_m$ superlattices by the growth on GaAs(011) substrate

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Self-organized quantum wire (QWR) structures are formed by the gas source molecular beam epitaxy growth of $(GaP)_n(InP)_m$ short period superlattices (n/m-SLs) on GaAs(011) substrate. Transmission electron microscopy observations show that the formed structures are elongated along the $[01\bar{1}]$ direction with improved straightness and uniformity compared with those on GaAs(100). QWRs formed in $(GaP)_n(InP)_m$ SL/$In_{0.49}Ga_{0.51}P$ multilayers (n/m-SL/InGaP MTLs) by self-organization exhibit a strong polarization dependence of the photoluminescence (PL) emission intensity for the fixed incident beam polarization. Temperature insensitive variation of the PL peak energy is also observed in these self-organized QWR structures.

1. Introduction

Self-organized quantum wires (QWRs) and quantum dots (QDs) are attracting great interest for novel device applications and physical studies. Lower threshold current density, increased differential gain and improved stability are expected by using these structures in laser diodes. However, it is difficult to control their sizes and structures by utilizing the self-organized phenomena and by only regulating growth conditions.

Recently, we have reported the substrate orientation dependence of lateral composition modulation in the $(GaP)_n(InP)_m$ short period superlattices (n/m-SLs) grown by gas source molecular beam epitaxy (MBE) [1, 2]. It was shown that SLs grown on GaAs(100) and (N11)A (N=2~5) substrates form self-organized wire and dot structures, respectively, by the strain-induced lateral composition modulation. On the other hand, SLs grown on GaAs(111)A and B substrates showed quasi-perfect SL structures with no lateral composition modulation. In the case of 1/1-SLs, the band gap reduction as large as 321 meV (large red-shift) was observed, due to the long-range ordering along the $\pm$ [111] direction (CuPt-type ordering [3]). In the wire structures formed on GaAs(100), their straightness and uniformity were insufficient.

In this paper, we report on the improvement of the wire structures by growing n/m-SLs on GaAs(011) substrate by gas source MBE. Optical properties for the QWRs formed in the $(GaP)_n(InP)_m$ SL/$In_{0.49}Ga_{0.51}P$ multilayers (n/m-SL/InGaP MTLs) are also discussed.

2. Experimental

n/m-SLs (thickness: 0.3 μm) and n/m-SL/InGaP MTLs were grown on GaAs(100) and (011) substrates at 420 °C and 480 °C, respevtively, by gas source MBE. Elemental Ga, In and thermally cracked PH_3 were used as group-III and group-V sources, respectively. PH_3 flow rate was 1.2 SCCM during growth of SLs and InGaP. In order to obtain smoothing surface, a 0.1 μm-thick GaAs buffer layer was grown at 600 °C after thermal cleaning at 620 °C. Formed structures were investigated with photoluminescence (PL) and transmission electron microscopy (TEM). TEM observation was conducted with a 100 kV acceleration voltage. 488 nm line of an Ar^+ laser was used as an excitation source.

3. Results and Discussion

3.1 TEM observation of self-organized wire (vertical superlattice) structures formed in $(GaP)_n$ $(InP)_m$ short period superlattices(n/m-SLs)

Plan-view TEM image for the 1.5/1.88-SLs grown on GaAs(100) showed wire (vertical superlattice) structures by lateral composition modulation along the [011] direction with a period of 12 nm, as shown in Fig.1(a). Wire structures with a length of over 0.3 μm were formed along the $[01\bar{1}]$ direction. As shown in the insets of Fig.1(a), $(01\bar{1})$ cross-sectional TEM image clearly shows lateral composition modulation along the [011], but $(01\bar{1})$ cross-sectional TEM image shows no composition modulation, consistent with the plan-view TEM image.

As shown in Fig. 1(b), the 1/1-SLs grown on GaAs(011) substrate also showed wire structures elongated along the $[01\bar{1}]$ direction with a length of over ~1μm and a lateral composition modulation with a period of 16 nm occurs along the [100] direction. The length of wires on GaAs(011) substrate is much longer than that (~300 nm) on
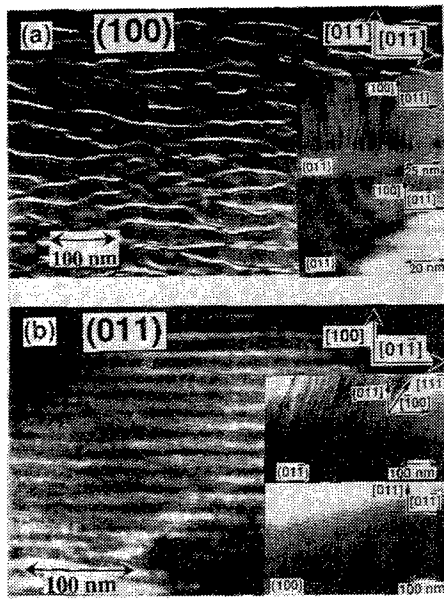
Fig.1 (a) Plan-view TEM image for the 1.5/1.88-SLs grown on GaAs(100) substrate (Inset: bright-field cross-sectional TEM images for (01$\bar{1}$) and (011) planes). (b) Plan-view TEM image for the 1/1-SLs grown on GaAs(011) substrate (Inset: bright-field cross-sectional TEM images for (01$\bar{1}$) and (100) planes).

Table I. Dependence of the self-organized vertical superlattice /columnar structure direction on the growth direction. The growth direction is perpendicular to the substrate surface and the angle described below is the angle difference from the [100] direction.

Growth direction (N)	Self-organized structure	Vertical direction of the structure (M)	N - M	[100] - N	[211] - N	[11$\bar{1}$] - N
[100] 0°	wire/vertical SL	[100]	0°	0°	35.3°	54.7°
[511] 15.8°	dot/columnar	[100]	15.8°	15.8°	19.5°	38.9°
[411] 19.5°	dot/columnar	[100]	19.5°	19.5°	15.8°	35.2°
[311] 25.2°	dot/columnar	[211]	10.1°	25.2°	10.1°	29.5°
[211] 35.3°	dot/columnar	[211]	0°	35.3°	0°	19.4°
[011] 90°	wire/vertical SL	[11$\bar{1}$]	35.3°	90°	54.7°	35.3°

GaAs(100) substrate. Uniformity and straightness are also significantly improved. This result shows that the growth of n/m-SLs on GaAs(011) substrate improves the straightness and uniformity of the self-organized wire structures. Insets of Fig.1(b) confirm the formation of vertical SL elongated along the [11$\bar{1}$] direction.

As can be seen in Table I, vertical SL or columnar structures elongated along the [11$\bar{1}$] direction have never been observed in the n/m-SLs grown on GaAs(100) and (N11) substrates, where the wire/vertical SL and dot/columnar structures were self-organized, respectively [4]. The [11$\bar{1}$] direction is one of the CuPt-type ordering directions for the natural SLs formed in InGaP alloy [3]. The vertical SL and columnar structures are formed in order to stabilize the strain-induced composition modulated self-organized structures. The vertical directions of the vertical SL/columnar structures may be selected so as to minimize the strain energy, and may be determined to one of the [100], [211] and <111> directions where the difference in angle between the growth direction and the vertical SL/columnar structure direction has minimum value.

The lateral direction [01$\bar{1}$] of the vertical SLs (wires) on GaAs(011) coincides with that on GaAs(100). The mechanism of lateral periodic composition modulation is considered to be similar to that on GaAs(100), because the lateral direction of the wires coincides with the migration direction of the adatoms. On GaAs(100), adatoms migrate along the [01$\bar{1}$] direction because of the formation of the missing dimer rows along this direction showing (2 x 4) reconstruction in order to minimize the backbonding strain under the group-V stabilized surface condition [5]. On the other hand, GaAs(011) surface shows (1 x 1) reconstruction showing no dimer rows along any direction. However, the (011) plane is perpendicular to the (100) surface, contains the preferable direction [01$\bar{1}$] for the adatoms migration on the (100) surface. On the (011) plane, the dangling bonds from both Ga and As atoms directed to the <111> directions. These directions give anisotropy between [01$\bar{1}$] and [100] directions on the (011) plane. Because of this anisotropy, adatoms migrate more easily along the [01$\bar{1}$] direction than along the [100] direction. Therefore, the elongated island formation occurs along the [01$\bar{1}$] direction during growth even on the (011) surface similar to that on the (100) surface.

PL spectra for the n/m-SLs grown on GaAs(011) substrates showed that the PL peak energy shifts toward lower energy (red-shift) due to the large lateral composition modulation by increasing n. PL peak energies at 77K for the 1/1-SLs and 1.5/1.5-SLs are 1.791 eV and 1.777 eV, respectively. These PL peak energies are close to those of the self-organized wire structures on GaAs(100) substrates.

3-2 Self-organized quantum wires formed in the $(GaP)_n$ $(InP)_m$ SL/ $In_{0.49}Ga_{0.51}P$ multilayers (n/m-SL/InGaP MTLs)

Self-organized QWR structures were formed on GaAs(011) substrates by growing 5 or 20 cycles of

100

n/m-SL(5 or 18 periods)/In$_{0.49}$Ga$_{0.51}$P(5 or 20 nm) MTLs. The MTLs were grown on (i) a 0.1 μm-thick GaAs buffer layer and (ii) a 0.3 μm-thick In$_{0.49}$Ga$_{0.51}$P buffer layer lattice matched to GaAs and capped with a 0.3 μm-thick In$_{0.49}$Ga$_{0.51}$P cap layer. (01$\bar{1}$) and (100) cross-sectional TEM images for the QWRs formed in the 5 cycles of 1.2/1.4-SL(18 periods)/InGaP(20 nm) MTLs clearly show the lateral periodic composition modulation along the [100] direction and the QWRs directed along the [01$\bar{1}$] direction, as shown in Fig. 2.
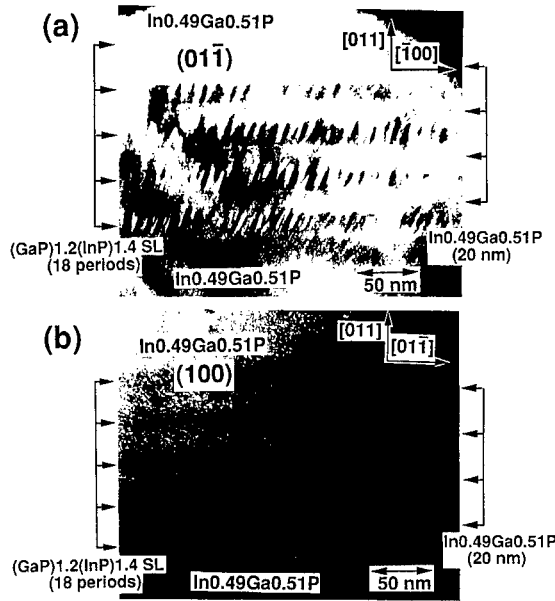
Fig. 2 Cross-sectional TEM images of (a) (01$\bar{1}$) and (b) (100) planes for the QWRs formed in the 1.2/1.4-SL/InGaP MTLs on GaAs(011).

PL spectrum of the QWRs was strong by dependent on the monolayer number n, m due to the degree of composition modulation in the SL region. Figure 3 shows the polarization dependence of the emission spectrum for the fixed incident beam polarization; E-vector E_{IN} parallel to the elongated direction [01$\bar{1}$] of QWRs. In Fig.3, the peak around 690 nm comes from the QWRs and those around 825 nm and 630 nm from GaAs buffer and In$_{0.49}$Ga$_{0.51}$P cap layer, respectively.

For convenience, let us define the polarization anisotropy

$\rho = (I_{[01\bar{1}]} - I_{[100]}) / (I_{[01\bar{1}]} + I_{[100]})$,

so that -1< ρ <1. Each subscripted I refers to the intensity of the polarization component of the emission along the indicated direction by the subscript. For the QWRs formed in the 5 cycles of 1.2/1.4-SL(18 periods)/InGaP (20 nm) MTLs grown on GaAs(011), the dominant polarization component is that in the [01$\bar{1}$] direction, parallel to the direction of the QWRs and the polarization ρ is as large as
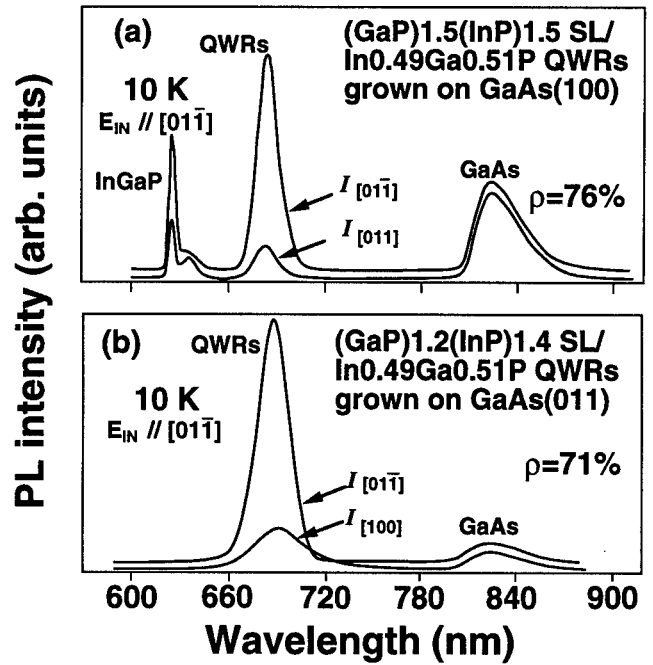
Fig.3 Polarization dependence of the emission spectrum at 10 K for the fixed incident beam polarization; E-vector parallel to the QWRs direction. (a) QWRs formed in the 5 cycles of 1.5/1.5-SL(18 periods)/InGaP(20 nm) MTLs grown on GaAs(100). (b) QWRs formed in the 5 cycles of 1.2/1.4-SL(18 periods)/InGaP(20 nm) MTLs grown on GaAs(011).

71% at the peak energy. This value is nearly the same as that (76%) of the QWRs of the 5 cycles of 1.5/1.5-SL(18 periods)/InGaP(20 nm) MTLs on GaAs(100). This polarization dependence implies the formation of QWRs in the SL region grown on GaAs(011). The PL peaks from the GaAs buffer layer and InGaP cap layer show the usual small polarization because of the bulk crystals with a zinc-blende type cubic symmetry [6]. The polarization for the QWRs formed on GaAs(011) depended on the monolayer number n and m, and increased with increasing n, m.

Figure 4 shows the temperature dependence of the PL peak energy for the QWRs formed in the n/m-SL/InGaP MTLs grown on GaAs(100) and GaAs(011) substrates. InGaP cap layers show the normal temperature variation of the PL peak energy with 1.22 Å/°C in the temperature range of 150 K to 300 K. On the other hand, the QWRs grown here show the temperature insensitive variation of PL peak energies compared with InGaP alloy. PL peak energy variation with temperature for the QWRs on GaAs(011) is similar to that on GaAs(100). PL peak energy variation in the temperature range of 150 K to 300 K for the QWRs formed in the 5 cycles of 1.2/1.4-SL(18 periods)/InGaP (20 nm) MTLs and the 5 cycles of 1/1-SL(18 periods)/InGaP(20 nm) MTLs grown on GaAs(011) were 0.63 Å/°C and 0.70 Å/°C,

101
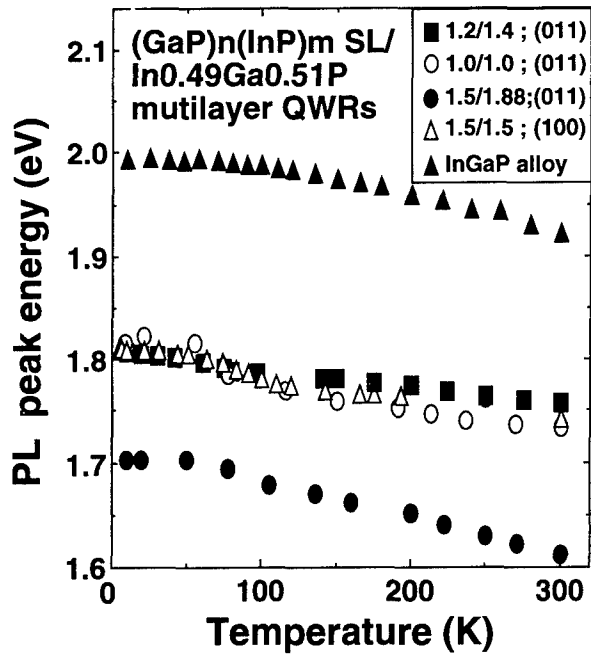
Fig. 4 Temperature dependence of PL peak energy for the QWRs formed in the 5 or 20 cycles of n/m-SL(5 or 18 periods)/InGaP(5 or 20 nm) MTLs grown on GaAs(100) and (011) substrates.

respectively, which is nearly the same as that of 0.72 Å/°C for the QWRs formed in the 5 cycles of 1.5/1.88-SL(18 periods)/InGaP(20 nm) MTLs grown on GaAs(100). The temperature insensitive variation of PL peak energy was also observed for the QDs formed in the n/m-SL/InGaP MTLs grown on GaAs(311)A [7] as well as for the QWRs formed in the $(GaAs)_n(InAs)_m$ SL/InGaAs MTLs grown on InP(100) substrates [8]. However, for the 20 cycles of 1.5/1.88-SL(5 periods)/InGaP(5 nm) MTLs grown on GaAs(011), the temperature variation of PL peak energy (filled circles) is as lager as 1.65 Å/°C in the temperature range of 150 K to 300 K. The temperature insensitive and temperature sensitive PL peak energies are considered to be caused by the multiaxial strain existing in the QWRs regions. For samples with a temperature insensitive PL peak energy, the change in the band gap energy with temperature must be canceled out by the temperature variations from the strains. It means that the strain field is not constant, but is considered to be a function of temperature. This temperature insensitive characteristics is considered to be an another candidate to fabricate the temperature insensitive wavelength laser diodes [9].

4. Conclusions

Self-organized QWRs were grown on GaAs(011) substrates by gas source molecular beam epitaxy. Transmission electron microscopy observations showed that the SLs grown on GaAs(011) has lateral composition modulation along the [100] direction with wire structures along the [01$\bar{1}$] direction. They also showed the improved straightness and uniformity compared with those of QWRs on GaAs(100). The direction of the QWRs by the lateral composition modulation is determined by the migration direction of adatoms. QWRs self-organized in the n/m-SL/InGaP MTLs exhibited a strong polarization anisotropy in the PL emission spectrum. Temperature insensitive variation of the PL peak energy was also observed in these self-organized QWR structures.

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A SURFACE-NORMAL REFLECTIVE OPTICAL MODULATOR AT A WAVELENGTH OF 1.3 μm USING THE WANNNIER-STARK EFFECT OF THE InP/InGaAsP SUPERLATTICE

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A surface-normal reflective optical modulator for the wavelength of 1.3 μm was investigated using the Wannier-Stark effect of an InP/InGaAsP superlattice (SL) . Electroabsorption properties of two devices with different miniband widths were compared. It was found that the modulator with a larger miniband width has a larger extinction ratio. The effect of the electric field distribution in the thick SL region was discussed. A chirped superlattice was introduced to compensate for the electric field distribution.

I. Background

The surface-normal electroabsorption modulator is a promising device for the optical parallel processer [1] and the transceiver of the future optical subscriber systems. [2-4] But the short interaction length between the incident light and the semiconductor, which is limited by the active region thickness, makes it difficult to get a high extinction ratio at a low bias voltage.

The Wannier-Stark effect (WSE) is suitable for the surface normal modulator because the operating electric field is quite low in comparison with the quantum-confined Stark effect (QCSE) . In addition, the WSE can be applied to the wavelength of 1.3 μm which is used by the subscriber system. A clear exciton absorption for the QCSE can not be observed in the quarternary quantum wells in the lattice matched system. [5]

The WSE has been studied mainly in GaAs/AlGaAs superlattices. [6-9] Although the WSE at 1.3 μm was observed at a low temperature, [10] a modulator operating at room temperature has not yet been reported. This paper reports the fabrication of a surface-normal modulator for the wavelength of 1.3 μm which uses the WSE at room temperature for the first time.

II. Device Structure

Figure 1 shows the device structure. It has a p^+-i-n^+ structure with an undoped InP/InGaAsP SL sandwiched by p^+- and n^+-InP layers which were
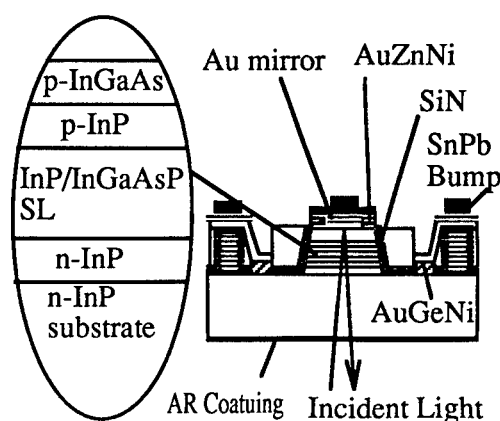
Fig. 1. Device structure.

Table 1. Structure of SL for devices A, B and C

	Well (nm)	Barrier (nm)	Miniband (meV)	SL period
A	5.7	2.0	67	500
B	6.3	2.7	38	500
C	6.5-5.8	2.4-2.0	43-65	500

grown by the gas-source molecular beam epitaxy on n-type (100) InP substrates. All layers were lattice-matched to the InP substrate. The absorption edge of the InGaAsP well layer was 1.4 μm. The residual impurity density of the SL was estimated by capacitance-voltage measurement to be about 5×10^{14} cm^{-3}. Three samples with different miniband widths were prepared (Table 1) . The miniband width was constant throughout the SL region in devices A and B, and was wider for device A. On the other hand, the miniband width was varied by adopting a chirped SL in device C.

A mesa structure with a diameter of 100 μm was formed by chemical etching. Au mirror was evaporated onto the p$^+$-InP to reflect the incident light. The device was flip-chip bonded to a sub-mount and illuminated through the substrate.

III. Experimental Results and Discussion

The reflectance spectra of devices A and B at various applied voltages are shown in Figs. 2. In device A, the reflectance in a wavelength region of about 1.305 μm is enhanced when the applied voltage increases up to 28 V, showing that the absorption coefficient decreases. The step-like dependence of the reflectance on the wavelength appears at bias voltages larger than 15 V. The steps which are indicated by the arrows in Fig. 2 shift to longer wavelength when the applied voltage increases. The photon energy of these steps is
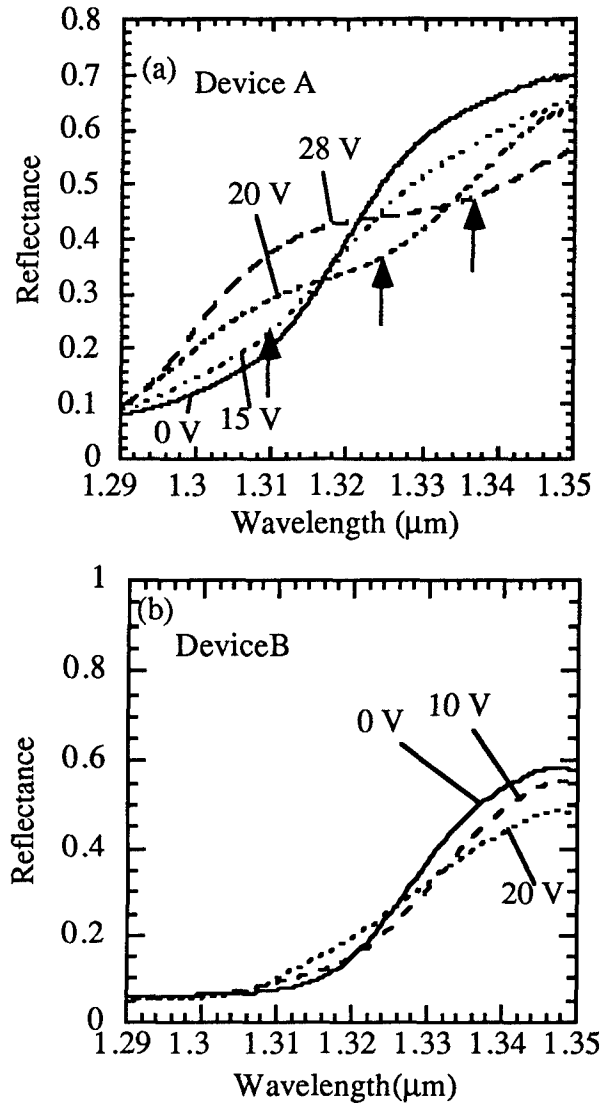
Fig. 2. Reflectance spectra of (a) device A and (b) device B.

plotted versus mean electric field in Fig. 3. The energy decreases linearly with the electric field. The slope of this dependence is -7.5×10^{-7} e-cm. This value is almost the same as ned predicted by the theory of the WSE,[11] where n is an integer index and d is the SL period. In this case, n is -1, showing that the absorption at the wavelength shorter than the step is due to the oblique transition to the nearest neighbor well layer. This result confirms that this reflectance was changed by the WSE. On the other hand, step due to the WSE cannot be clearly seen
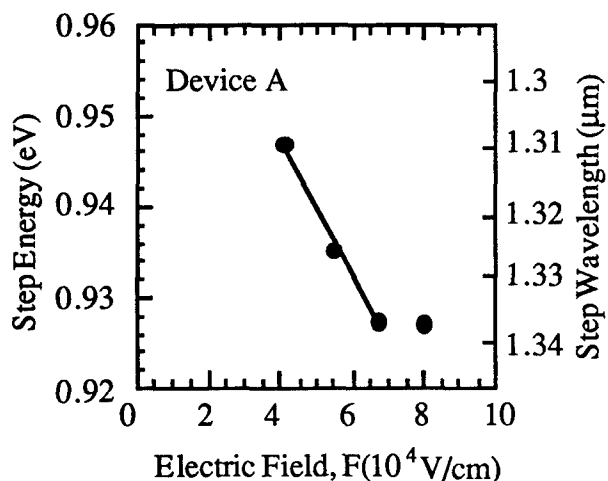
Fig. 3. Photon energy of the step in the absorption spectra as a function of electric field (device A).

in the reflectance spectra of device B as shown in Fig. 2(b).

Figure 4 shows the extinction ratio at the bias voltage which gives the maximum ratio for devices A and B. An extinction ratio of 3.3 dB is achieved at 1303 nm when the applied voltage is 28 V. The insertion loss of device A is found to be 5.1 dB at this wavelength. The extinction ratio decreases

when the bias voltage is larger than 28 V because of the red shift of the fundamental absorption edge. The maximum extinction ratio of device B is, on the other hand, 2.0 dB at a voltage of 20 V. The insertion loss is 8.3 dB. The region where the extinction ratio is positive is wider for device A. This result can be understood considering that the amount of the blue shift due to the WSE is half of the miniband width, $\Delta/2$. [11]

The difference in the characteristics of these devices can be attributed to the electric field distribution. Because the SL region is as thick as 4 μm in order to enhance the extinction ratio, variation of the electric field cannot be neglected even if the residual impurity density is as low as 5×10^{14} cm^{-3}. The change in the absorption coefficient due to the WSE depends on the normalized electric field, $F/ (\Delta/ed)$. [12] The nonuniformity of the absorption coefficient change is more significant in device B because miniband width Δ is small. The poor modulation

Fig. 4. Wavelength dependence of the extinction ratio for devices A and B at the bias voltages which gives the maximum ratio. (Ratio at 20 V for device A was also shown for compraison.)
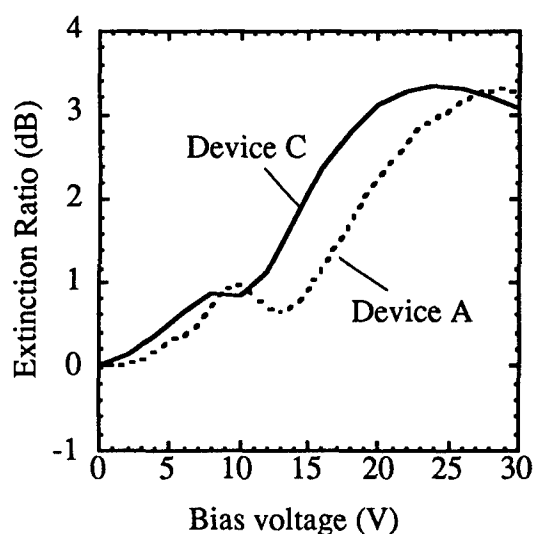
Fig. 5. Bias voltage dependence of the extinction ratio of the device with a chirped SL (device C). The ratio for device A is also shown for comparison.

105

characteristics of device B show that the nonuniform WSE in SL is responsible for the deterioration of the device performance.

In order to make the WSE take place uniformly in the SL region, a chirped SL was introduced (device C in Table 1). At the position close to p^+-InP, where the electric field is at its maximum, the barrier layer was made thinnest so that the miniband width Δ is largest in the SL region. The barrier was made thicker gradually as it approaches the n^+-InP layer. The well layer was also varied so that the absorption edge energy was constant. Because Δ/ed can be made equal to the electric field strength at every position in the SL region at a given bias voltage, WS localization can take place uniformly.

Figure 5 shows the extinction ratio as a function of the bias voltage. The operating bias was reduced by 6 V in comparison with device A with a uniform SL. This shows that the applied voltage is efficiently used to induce the WSE.

IV. Summary

The electroabsorption properties of a surface-normal reflective optical modulator operating at 1.3 μm and using the WSE effect of an InP/InGaAsP ($\lambda_g = 1.4$ μm) SL were studied at room temperature. The modulator with a larger miniband had a larger extinction ratio. An extinction ratio of 3.3 dB was achieved at an applied voltage of 28 V in a sample with a 500-period 2.0-nm-thick InP/5.7-nm-thick InGaAsP superlattice. The chirped SL was introduced in order to compensate the electric field distribution due to the residual impurity. The operating bias voltage was reduced 6 V by the chirped SL.

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TUNABLE NARROWBAND OPTICAL FILTER IN PHOTOREFRACTIVE
InGaAsP:Fe/InP:Fe SINGLEMODE WAVEGUIDE

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Introduction

Recently a new compact WDM spectrum analyser without moving parts was demonstrated using a bulk photorefractive InP:Fe crystal. With the aim of reducing the sweeping time by confining optical energy, a first optically tunable filter on a photorefractive singlemode waveguide was realized on an InP:Fe substrate. The device operates at the 1.55 μm wavelength and the tuning range is given by the tunable laser diode used for the control of the Bragg grating period. The bandwidth is 0.02 nm (2.5 GHz) and the intrinsic reflectivity is 2 %.

I. Optically tunable filter in photorefractive InP:Fe

In semi-insulating InP:Fe crystals, the photorefractive effect is based on generation, drift and finally the trapping of free carriers thus enabling the electro-optic effect to take place. Hence, two counter-propagating coherent beams generate a Bragg reflector. These beams are the control beams of the filter. The grating period is given by the laser wavelength λ_c and the refractive index n of the material. The signal beam has an external angle θ with respect to the control beams as shown in Fig.1.
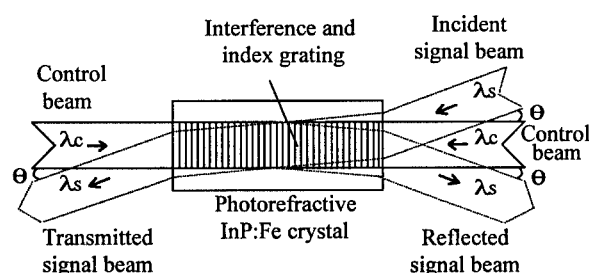
Fig. 1. Principle of the photorefractive filter.

At the Bragg condition, the relation between the signal wavelength λ_s and the control wavelength λ_c is given by:

$$\lambda_s = \lambda_c \sqrt{1 - \left(\frac{\sin \theta}{n}\right)^2} \quad (1)$$

where n is the refractive index of InP:Fe. An angle θ of only 2° or 3° is suitable for a convenient separation of the external beams as well as for a good overlap inside the crystal. The gaussian-shaped beams are formed by fibered collimators leading to typical diameters of 0.5-1 mm. The ratio between λ_s and λ_c is very close to 1 and the filter becomes tunable when using an optical tunable source around 1.55 μm.

A compact filter was previously realized by directly associating a bulk InP:Fe crystal and collimators on a same mount. The minimum required control power was typically 1 mW with a lower signal level in order to avoid partial erasure of the grating. The coupling coefficient κ being low ($< 0.2 cm^{-1}$), the coupling length L must be sufficient in order to yield a significant reflected signal. When taking into account the attenuation coefficient α, the maximum reflection coefficient R is approximately given by:

$$R \approx exp(-\alpha L) \ tanh^2 (\kappa L) \quad (2)$$

For $L = 18$ mm, $\alpha = 0.11 \ cm^{-1}$ and $\kappa = 0.14 \ cm^{-1}$, the calculated reflection coefficient is 5% while it is 1.8% for the measured value due to the insertion loss of the collimators. This bulk InP:Fe crystal filter (BCF#1) has a 3dB bandwidth of 0.02 nm and a sidelobe rejection of 16 dB.

II. Spectrum analysis using a tunable photorefractive filter in a bulk crystal

WDM spectrum analyzers using bulk photorefractive InP:Fe crystals are attractive

appliances due to their compactness and the absence of moving parts (1).

In order to improve the resolution, a narrower bandwidth (BW = 0.015 nm) filter (BCF#2) was developed by using a longer crystal (L = 30 mm). The signal beam being tilted with respect to the grating, the coupling coefficient is non uniform. Thus a 25 dB sidelobe rejection was obtained due to the natural apodization of the filter. The wavelength sweeping range of the first demonstrated device was 13 nm (1547-1560 nm) corresponding to the tunability of the associated DBR laser diode (2). The principle of this type of analyzer is given in Fig.2.
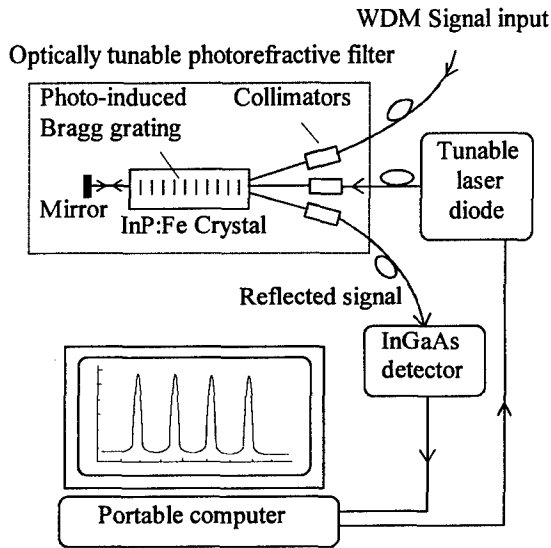
Fig. 2. Principle of the spectrum analyzer using a photorefractive filter.

The sweeping time of this analyzer is about 6 s for the whole wavelength range due to the response time of the filter which is typically around 5 ms. The speed of the grating generation can be improved by increasing the optical intensity either with a more powerful laser diode or by reducing the dimensions of the beams. In order to use a laser diode with moderate power, confining light is probably the more effective solution.

III. InGaAsP:Fe/InP:Fe photorefractive planar waveguide

A. Waveguide structure

The photorefractive slab waveguide was realized on a semi-insulating InP:Fe substrate by Gas Source Molecular Beam Epitaxy (3). The GaInAsP:Fe (gap = 1.13 eV) core layer is 0.2 μm thick; the lower buffer and upper cladding are both InP:Fe layers

(0.5 μm and 0.8 μm thick respectively). The Fe concentration is 10^{17} cm^{-3} in the epitaxial layers and the concentration of ionized traps is enhanced by Si doping (10^{16} cm^{-3}) (4).

The growth is <110> oriented allowing index variations for both TE and TM modes when the propagation is along <001>. The core layer presenting a higher absorption than the other layers, the slab waveguide is designed so that some 75% of the optical energy propagates in the InP:Fe material. Such a mode pattern is also effective for the photorefractive effect in InP:Fe. The waveguide structure and the corresponding mode pattern are shown in Fig.3.
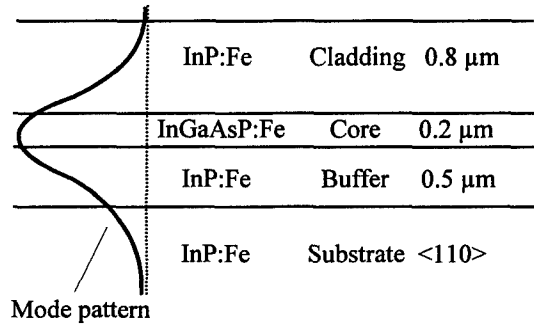
Fig. 3. Waveguide structure[2]

B. Measurement of the photorefractive gain

Two coherent waves interfering in the photorefractive medium induce an index grating. In this quasi contra-directional configuration, the grating period is close to its minimum value:

$$\Lambda \approx \frac{\lambda}{2\,n_{eff}} \quad (3)$$

n_{eff} is the effective index of the propagating mode ($n_{eff} \approx 3.18$). The grating period being 4 times smaller than the diffusion length ($L_D \approx 1$ μm), no external field is needed.

The waves undergo coupling known as two-wave mixing. Depending on the polarization and on the crystal orientation, one beam is amplified while the other one is depleted. The evolutions of the beams in the crystal are related to the attenuation α and to the photorefractive gain Γ given by:

$$\Gamma = \frac{4\,\pi\,\Delta n}{m\,\lambda\,cos\varphi} \quad (4)$$

where Δn is the amplitude of the index variation which is related to the intensity level and to the material properties. m is the fringe modulation ratio $(0 \leq m \leq 1)$, λ is the wavelength and φ is the angle between the beams and the propagation axis (the angle φ is very small as the waves are contra-directional).

108

A simple case is obtained when the pump to signal ratio β is set large so as to consider the pump undepleted with respect to the signal, that is to say for a low value of m. The photorefractive gain can be approximately deduced from the relation:

$$\Gamma \approx \frac{\ln(\gamma)}{L} \quad (5)$$

where L is the interaction length and γ is the measurable ratio:

$$\gamma = \frac{Is_{Pon}(L)}{Is_{Poff}(L)} \quad (6)$$

$I_{sPon}(L)$ is the output signal intensity when the pump is on; $I_{sPoff}(L)$ is the output signal intensity when the pump is off. Equation (6) does not depend on the attenuation coefficient α.

For the two-wave mixing experiment, the beams are slightly tilted in order to easily separate the external beams. The beams are coupled in and out by silicon prisms as shown in Fig.4.

Fig. 4. Contra-directional two-wave mixing.
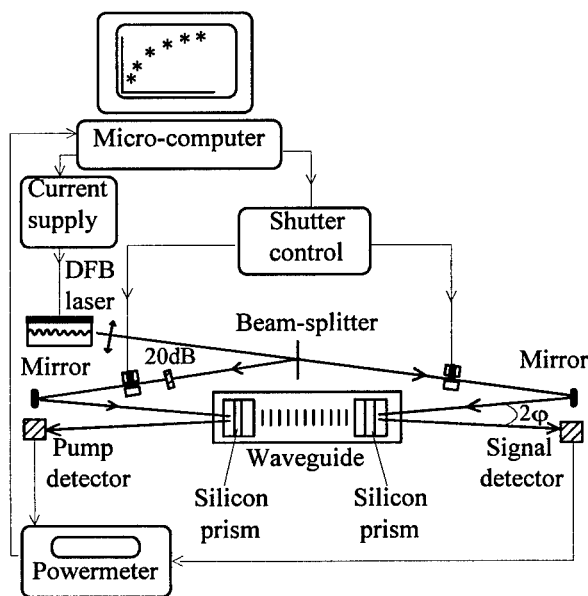
The interaction length L is evaluated as the space between the prisms (18 mm). The intensity in the waveguide is given with arbitrary units because the prism coupling coefficient is difficult to determine. At low optical intensity, the carriers are not all redistributed on the deep-level centers. Thus the space-charge field does not reach its maximum value. In the absence of an external field, the gain increases continuously as a function of the optical intensity and finally reaches a maximum value around 0.53 cm⁻¹ as shown in Fig.5.

Fig. 5. Photorefractive gain versus intensity ($\beta = 200$, $\Lambda = 0.25\ \mu m$, room temperature).
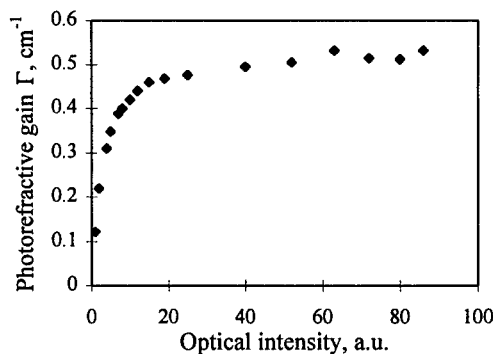
Assuming that the angle φ and θ are very small, the coupling coefficient κ of the generated Bragg reflective filter is:

$$\kappa \approx m\frac{\Gamma}{4} \quad (7)$$

The fringe modulation ratio must be set close to its maximum value for the filtering application. The maximum obtainable value for κ is then 0.13 cm⁻¹.

IV. Tunable filter in photorefractive waveguide

A. Experimental setup

The optically tunable Bragg filter is realized by following the principle described in section I. The angle θ is set to 2.4° for this experiment. Silicon prisms are used for the input and output coupling (Fig.6).

Fig.6. Tunable filter characterization
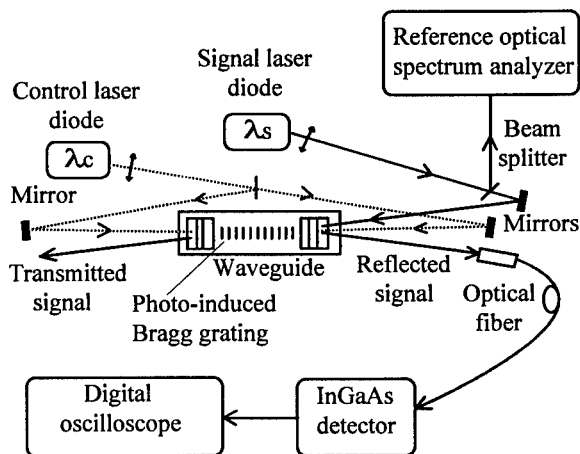
109

The control laser diode is a 3 section DBR laser diode with a continuous wavelength range of 12 nm (1542-1554 nm) (2).

The spectral response of the filter is obtained by sweeping the wavelength λ_s of the signal laser diode (2 electrode DFB) when the control wavelength λ_c is fixed. The reflected signal is injected into a singlemode fiber via a collimator and the InGaAs detector is connected to a digital oscilloscope for direct visualization of the spectral response.

B. Experimental results and discussion

The wavelength of the signal laser as a function of its currents is previously measured with a reference optical spectrum analyser. This gives the wavelength calibration of the filter spectral response.
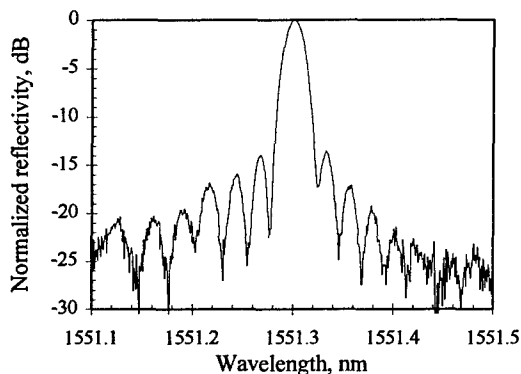
Fig.7. Normalized spectral response of the filter

The measured spectral response (Fig. 7) is very close to the predicted response of a Bragg grating with $L = 18\ mm$ and $\kappa = 0,12\ cm^{-1}$. The measured and calculated sidelobe rejections are 13.5 dB and 13.1 dB respectively. The measured bandwidth is 0.02 nm which is the same as that obtained for the bulk crystal filter BCF#1 with a 18 mm long crystal.

The maximum reflectivity is comparable to the reflectivity of BCF#1. An intrinsic value of 2 % is measured when the reflected signal is compared to the transmitted signal instead of the incident one.

The waveguide structure filter has a polarization dependence of 2 dB whereas it is less than 0.5 dB for bulk crystal devices. For this experiment, the grating is generated with the TE mode and the signal mode is first TE and then TM using a half-wave plate.

The signal wavelength λ_s is fixed for the measurement of the response time of the filter. The control laser wavelength λ_c is periodically changed in

order to establish and to cancel the Bragg condition. The measured response time is 250 µs which is 20 times lower than that obtained for the bulk filter. This will lead to a faster (300 ms) wavelength sweeping of the spectrum analyzer described in section II. Despite the low prism coupling, this result shows that the optical intensity is higher in the waveguide than in the bulk crystal. Using the theoretical model for the photorefractive effect in InP:Fe (5), such a response time corresponds to an optical intensity greater than 25 W/cm². With more efficient coupling, the response time could be greatly reduced. Further work is also necessary for efficient coupling of all inputs and outputs with optical fibers.

Conclusion

This filter for narrowband WDM spectrum analysis is the first application for InP:Fe based photorefractive waveguides. Despite the low prism coupling efficiency, the response time of the waveguide filter is 20 times lower than the previous bulk device. Further work is in progress and new samples have been designed in order to improve filter performances such as polarization dependence and fiber coupling.

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LEAKAGE CURRENT DETECTION IN InGaAsP LASER DIODES BY IMAGING OF THE OPTICAL EMISSION WITHIN THE CONFINING InP LAYERS

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Introduction

The optical emission at 950nm due to charge carrier recombination within the confining InP layers has been measured for buried heterostructure and ridge waveguide 1300nm InGaAsP Multi Quantum Well Fabry-Perot laser diodes as a function of the temperature and of the injected current. Above laser threshold, this emission does only weakly depend on laser current for the ridge waveguide type while it increases exponentially with injection current in the case of Double Channel Planar Buried Heterostructure and Facet Selective Buried Heterostructure laser diodes. At high current densities, the 950nm emission is mainly due to lateral leakage currents. For buried heterostructure laser diodes, a direct correlation has been found between the sublinearity of the optical emission vs. laser current characteristics and the integral of the InP emission. Second harmonic generation with a conversion efficiency below 10^{-9} has been observed.

I. Background

Monitoring optical emission of the recombination within the confining InP layers at a wavelength of 950nm is a useful technique for the evaluation of the leakage currents in InP/InGaAsP based laser diodes (1). It has been shown that in stripe geometry laser diodes, the Auger recombination induces carrier leakage (1, 2) and the theoretical leakage current is proportional to the 950nm emission (3).

In vapor-phase regrown buried hetero-structure lasers a direct correlation between the sublinearity of the optical power - laser current characteristics and the 950nm emission strength has been found (4).

In the present work, we applied such technique to the characterization of the temperature dependent current losses in both weakly and strongly index guided laser diodes.

II. Device structures and measurement set-up

Three different commercial laser diode families with similar optoelectronic performances but different current confining structures have been investigated. All the families have Multi Quantum Well InGaAsP active layers and emit around 1300nm.

Family A devices are Facet Selective Buried Heterostructure (FSBH) laser diodes (5) grown on p-type InP substrate. The family B devices are Double Channel Planar Buried Heterostructure (DCPBH) laser diodes (6) grown on n-type InP substrates and the family C devices have a weakly index guided ridge waveguide structure.

The specified temperature range (T_{op}), the average characteristic temperature (T_o) and the threshold current at 25°C (I_{th25}) of the three families are summarized in Table 1.

Table 1

laser family	T_{op} (°C)	I_{th25} (mA)	T_o (K)
A	-40...85	10	46
B	-40...70	11.5	70
C	-40...85	13.5	63

The electroluminescence measurements have been performed using a microscope mounted cooled silicon CCD camera. Interferential bandpass filters with a spectral width of 70nm have been inserted within the optical path in order to investigate the wavelength dependence of the optical emission.

III. Results and discussion

As shown in Fig.1, the optical emission integral of a FSBH laser diode with a fundamental emission around 1300nm exhibits, in the wavelength range from 650nm to 1000nm, two distinct maxima at 650nm and at 950nm. Plotting the maximum pixel current in place of the integral optical emission, the maximum at 650nm gets more pronunced and exceeds the value of the optical emission at 950nm, indicating that the emission at 650nm is highly confined. A very similar wavelength dependence as demonstrated in Fig.1 for the FSBH laser has also been found for the DCPBH type laser diode.
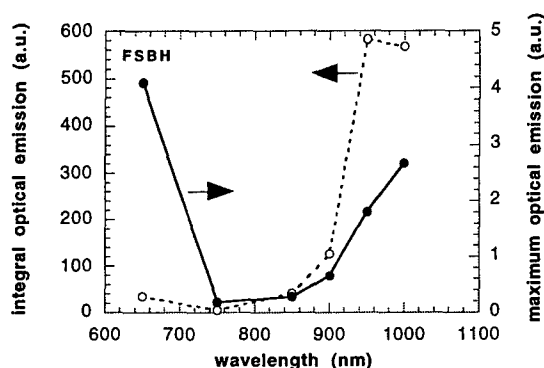
Fig.1 *Maximum and integral values of the secondary emission of an FSBH MQW laser diode with a fundamental emission at 1300nm as a function of the bandpass center wavelength. ($T_m=25°C$, $P_{(1300nm)}=10mW$).*
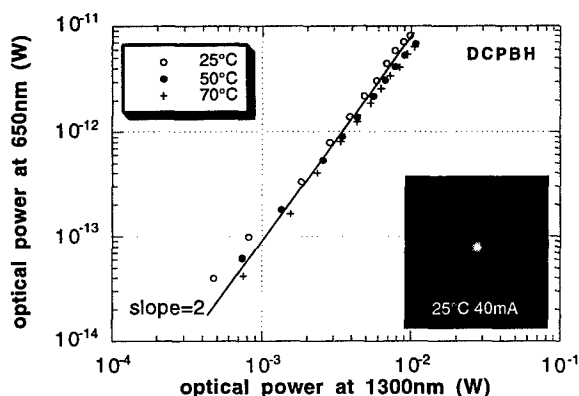
Fig.2 *Emitted optical power at 650nm measured at three different temperatures of a DCPBH laser diode with a fundamental emission at 1300nm.*
Inset: Near field optical image of the 650nm emission measured with a bias current corresponding to 10mW emission at 1300nm.

In Fig.2 it can be seen that the power of the 650nm emission increases with the square of the fundamental optical emission at 1300nm independently of the value of the operation temperature. In the inset of Fig.2 the electroluminescence image at 650nm is shown for a biasing condition corresponding to a 10mW optical emission at 1300nm.

This emission at 650nm is due to second harmonic generation (SHG) within the laser cavity itself, as it has been already observed for GaAs based laser diodes (7). Due to selfabsorption in the cavity only a low conversion efficiency value of 10^{-9} at an emitted power of 10mW at 1300nm has been observed. The 650nm electroluminescence image is strongly localized and the position has been identified with the active area region of the laser diode.

The optical emission integral at 950nm at different temperatures, is shown in Fig.3 as a function of the current for a DCPBH laser. The maximum current has been limited to values corresponding to an optical power of 10mW at 1300nm, which is the specified operating range of these devices. While for the subthreshold regime a power law dependence of the emitted optical power on the laser current has been found, above threshold the emission increases exponentially with increasing laser current. This occurs for the whole observed temperature range. In the inset of Fig.3 it can be seen that, at a fixed bias current of 40mA, the 950nm optical power increases exponentially with temperature, as it can be expected on the basis of an Auger induced current leakage model (2).
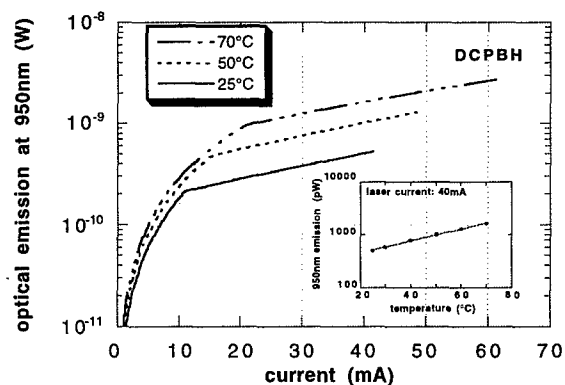
Fig.3 *Laser current dependence of the emitted optical power at 950nm of an DCPBH laser diode measured at three different temperatures.*
Inset: Temperature dependence of the 950nm integral emission at a fixed laser current of 40mA.

In a next step we measured simultaneously the 950nm and 1300nm emission during an upward and downward current ramp, exceeding by far the specified operating power. The results, measured at an operating temperature of 70°C for a FSBH laser, are shown in Fig.4. For a laser current of about 200mA, rollover has been observed and for further increasing laser current values the optical power at 1300nm decreases again. At a current value of 410mA, the device does not lase anymore. No hysteresis between upward and downward current ramp has been observed. The 950nm emission increases monotonically for increasing laser current and reaches a saturation level of 40nW at 410mA.

values the maximum of the emission is found slightly above the active area. It is due to electron heterojunction leakage into the upper confining p-InP layer.
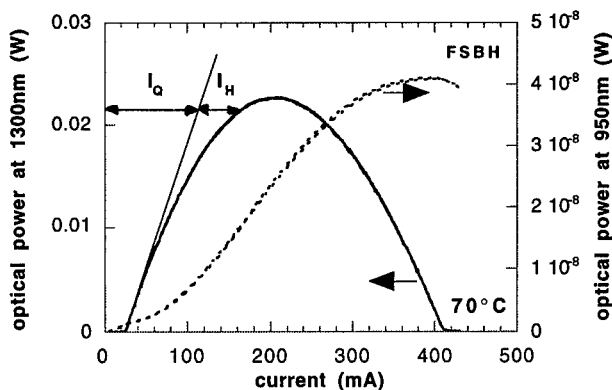
Fig.4 *Emitted optical power at 1300nm (full line) and at 950nm (dashed line) of an FSBH MQW laser diode as a function of the diode current.*

Let I_H be the excess current with respect to the theoretical value I_Q obtained by linear extrapolation of the tangent to the P-I characteristic little above the lasing threshold. A graphical illustration of the method used to obtain these two currents components at a given power (I_Q and I_H) is given in Fig.4. We adopted the technique reported in (4).

The behavior of the quantity I_H as a function of current I_Q has been compared with the integral of the optical power at 950nm for both a FSBH and a DCPBH laser diode (see Fig. 5). It can be seen that in a wide current range, from a value slightly above lasing threshold current to a value slightly below the current at the rollover point, both curves are parallel. This confirms that, in a wide laser current range, the 950nm emission is indeed proportional to leakage currents in buried heterostructure laser diodes.

The two images of the 950nm emission of a DCPBH laser at a temperature of 70°C, displayed in Fig.6, confirm that for intermediate current

Fig.5 *Emitted optical power at 950nm (open circles) and "missing" current I_H (filled circles) as a function of the "theoretical" current I_Q determined for a FSBH and a DCPBH laser diode at 70°C.*

a)

b)
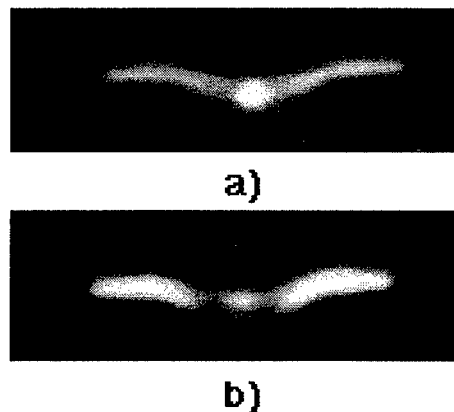
Fig.6 *Image of the 950nm emission of a DCPBH MQW laser (T_m=70°C) for two different laser current values: a) 20mA (P_{1300nm}=5mW), b) 200mA (P_{1300nm}=25mW).*

At very high current injection levels (corresponding to the rollover point of the P-I

characteristics) the maximum emission shifts instead laterally. A comparison with the secondary electron microscopy (SEM) image of the same structure (Fig. 7) shows that the main contribution to the 950nm emission can be attributed to recombination within the different p-layers (8).
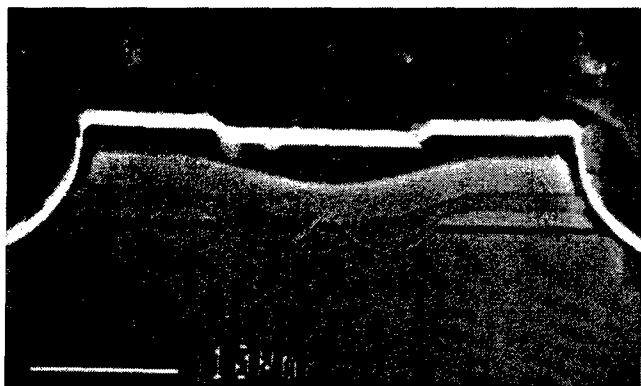
Fig.7 *Secondary electron microscope image of a DCPBH MQW laser diode.*

In contrast to the buried heterostructure lasers investigated so far, for a ridge waveguide laser diode we observed that the 950nm emission was almost pinned above threshold (see Fig.8). This can indeed be expected because of the absence of lateral current leakage paths.
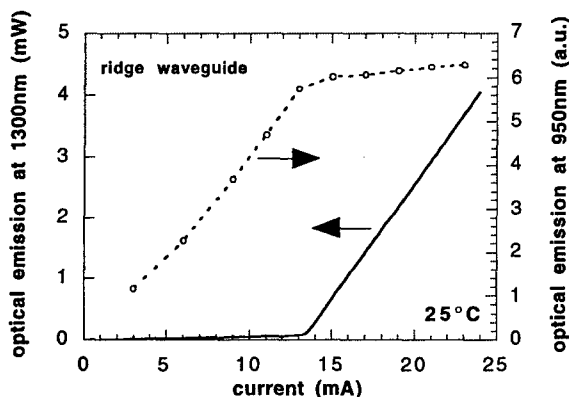
Fig.8 *Emitted optical power at 1300nm (full line) and at 950nm (dashed line) of an ridge waveguide MQW laser diode as a function of the diode current.*

IV. Conclusions

A direct correlation between the high temperature sublinearity of the P-I characteristics and the 950nm emission has been found for two different types of buried heterostructure InGaAsP MQW laser diodes. At low bias currents, the

heterojunction electron leakage dominates in all investigated lasers, while at high operating currents lateral leakage becomes predominant in buried heterostructure lasers leading to an exponential increase of the 950nm emission with increasing current. In ridge waveguide lasers the 950nm emission does only weakly increase with current above threshold. Additionally second harmonic generation within the laser cavity has been observed.

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TUNABLE MONOLITHIC FABRY-PEROT FILTER MANUFACTURED BY SELECTIVE ETCHING OF InGaAs/InP EPITAXIAL FILMS

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Abstract

With this paper we report the successful manufacturing of a monolithic Fabry-Perot tunable filter. The filter consists of an air-gap cavity defined between two high reflectance Bragg mirrors. The top mirror is placed on an InP bridge which can be actuated electrostatically. When biased, the bridge moves towards the substrate, reducing the length of the cavity and tuning the resonance wavelength. The air-gap cavity was manufactured by wet etching of InGaAs epitaxial layers with excellent selectivity to InP and InGaAsP. The bottom mirror is a high reflectance 50 periods InGaAsP/InP Bragg reflector. The resonance dip of the cavity is less than 3 Å wide. A tuning range of 30 nm was demonstrated for a bias voltage of up to 25 V.

I. Introduction

Tunable filters and detectors are of high interest for fiber optics communications at 1550 nm (Wavelength Division Multiplexing). When the communication channels are very close (1.6 nm, or even 0.8 nm), not only narrow bandpass filters (detectors) are required, but also the ability of the detector to track the transmission channel is mandatory. In order to provide a maximum signal to noise ratio and a minimum crosstalk between channels, the detector should be able to compensate for the smallest change in the wavelength of the carrier. It is important that the filters could be integrated with the photodiodes, eliminating the need for relative alignment and providing a cost effective solution.

The InP/InGaAs materials system is very attractive for manufacturing detectors for the 1550 nm band. High quality InGaAs photodiodes are already available. With the aim of producing a monolithic tunable detector, we have investigated the possibility to manufacture a tunable Fabry-Perot filter that can be integrated with an InGaAs based photodiode.

II. Design of the filter

The filter consists of an air-gap Fabry-Perot cavity defined between two high reflectance Bragg mirrors (Fig. 1). The bottom mirror is n-type and the top mirror is placed on a p-type InP bridge which can be actuated electrostatically, by reverse biasing the structure. When the structure is biased, the bridge moves towards the substrate, reducing the length of the cavity and tuning the resonance towards shorter wavelengths.

The cavity is one wavelength long. A short cavity has the advantage of providing a large free spectral range for the Fabry-Perot filter. In order to obtain a narrow resonance, very high reflectance mirrors were used.

The bottom mirror is a n-type Bragg reflector with 50 pairs of quarter wavelength InGaAsP/InP layers. The nominal reflectance of the mirror is larger than 99.7% at the design wavelength ($\lambda_0 = 1550$ nm). The stop band of the Bragg reflector is approximately 100 nm wide.

The top mirror consists of a stack of 3 periods of quarter wavelength Si/SiO$_2$ alternating layers on top of a $9/4\,\lambda\,p$-doped InP bridge. The InP layer was designed to be part of the mirror. The thickness is $9/4\,\lambda$ to improve the mechanical stability. The top mirror should provide more than 99.7% reflectance at the design wavelength of 1550 nm and a wide stop band, characteristic to the Si/SiO$_2$ Bragg mirrors.
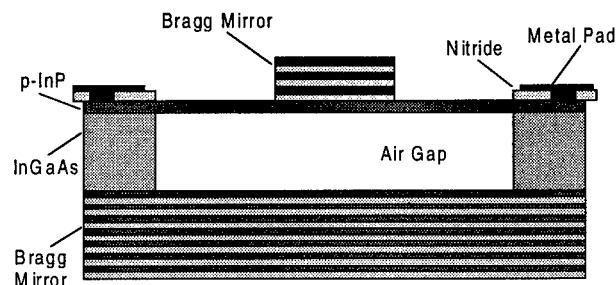
Fig. 1 Schematic drawing of the tunable Fabry-Perot filter.

The calculated spectral reflectance of this Fabry-Perot cavity is presented in Fig. 2. The spectral reflectance was computed using the transfer matrix method (1). The absorption in the materials was taken into account. The structure was considered planar. The reflectance has a very wide stop band, which extends down to approximately 1200 nm. The feature around 1400 nm is due to the integration of the 9/4 λ InP bridge with the top mirror. The resonance dip of the cavity should have a full width at half maximum (FWHM) of 0.9 Å only.

III. Fabrication

The basic structure consists of 50 pairs of n type InGaAsP/InP quarter wavelength layers having on top the sacrificial 1550 nm thick (undoped) InGaAs layer and the 1100 nm (9/4 λ) p doped InP layer (Fig. 1). The structure was grown by MOVPE. Details of the growth process are described elsewhere (2). The quality of the 50 periods bottom mirror is critical. For this reason we have used the mirror structure that our laboratory currently fabricates for the vertical cavity lasers (3).

A 1 μm thick silicon nitride (SiN_x) layer was deposited on top of the basic structure by PECVD. Contact windows were opened in the nitride film down to the InP layer. The contacts were formed by deposition of Au/Zn layers followed by a rapid thermal annealing step. Then, a Ti-W/Au structure was deposited and patterned to form the contact pads.

The mesas were generated by etching rectangular ditches with a width of 56 μm, separated by 18 μm. The ditches are 1.8 μm deep. The resulting mesas are 18 μm wide and 56 μm long (Fig. 3). Fig. 3 shows also the metal pads and the 56 μm wide ditches.
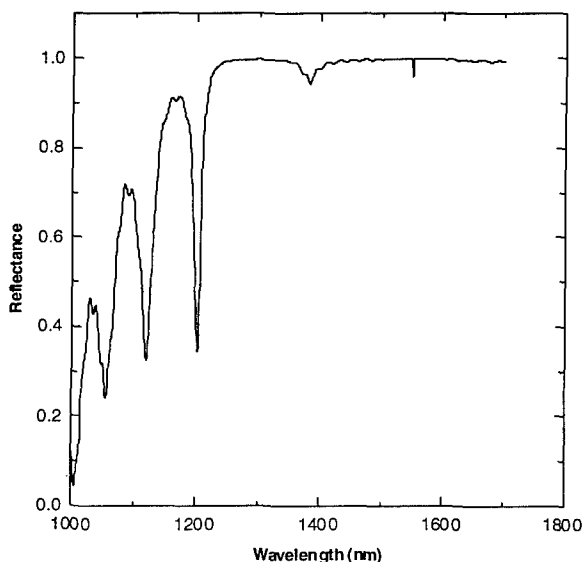
The edge of the silicon nitride layer is visible between the edges of the metal pad and of the ditch.

Three pairs of Si/SiO_2 quarter wavelength layers (111 nm and 267 nm thick, respectively) were deposited on top of the mesas by electron beam evaporation. The Si/SiO_2 stack was then patterned to form square mirrors of 16 μm x 16 μm, centered to the mesas.

The fabrication of the Fabry-Perot cavity was ended by selectively etching the sacrificial InGaAs layer sandwiched between the InP bridge and the bottom mirror.

We have previously demonstrated that selective etching of InGaAs epitaxial layers can be used to manufacture air-gap Bragg reflectors (4) and vertical cavity lasers using InP/air-gap reflectors (5). This etch process has excellent selectivity and the resulting InP/air interfaces present good optical properties.

The same etch process based on $FeCl_3:H_2O$ (1:1) was used now for producing the air-gap of the Fabry-Perot cavity. In this way, the accuracy in the length of the cavity is limited by the epitaxial process only.

After the sacrificial InGaAs layer was removed, the sample was rinsed in H_2O and acetone. In order to avoid the risk of sticking due to the surface tension of the liquid, the sample was dried by sublimation of tert-butanol, according to the procedure described by *Greek et al.* in Ref. 6.

IV. Results and Discussion

The manufactured Fabry-Perot filters were characterized by recording the spectral reflectance for different bias voltages. The spectral reflectance was measured in a spot of approximately 12 μm diameter, centered to the Si/SiO_2 top mirror. The light source used for the measurements was a tungsten filament

Fig. 2 Spectral reflectance simulated for the Fabry-Perot cavity presented in Fig. 1.
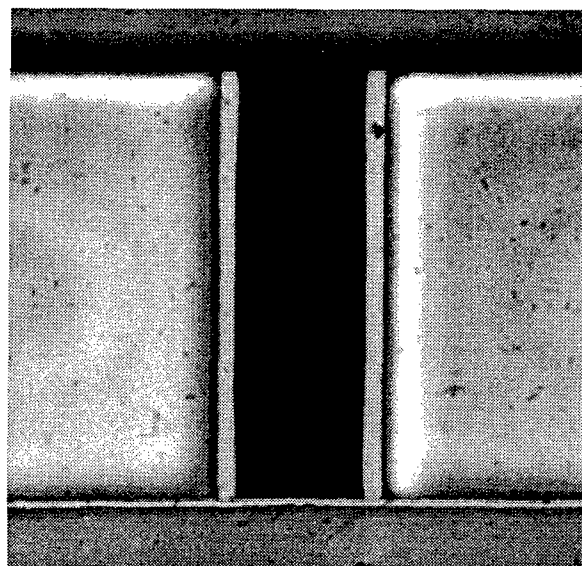
Fig. 3. Optical microscopy image of the structure before the deposition of the top Si/SiO_2 mirror. The 56 μm x 18 μm mesa (black) is surrounded by the ditches and the contact pads (dark grey).

halogen bulb. The detection was performed with a liquid nitrogen cooled Ge PIN detector mounted after a monochromator.

First, the tuning of the top mirror was checked. The eventual detuning of the top mirror can seriously affect the resonance dip and its position. A general spectrum was recorded for the range of 1100-1700 nm with a resolution of 2 nm. The spectrum was compared to the one in Fig. 2. A shift in the position of the edge of the stop band will indicate the eventual detuning of the top mirror.

Then, the resonance dip was located by recording the spectral range of 1450-1600 nm with a resolution of 5 Å. The shift of the resonance dip was measured for different values of the bias voltage in the range of 0-25 V.

A typical tuning characteristic is presented in Fig. 4. The resonance dip was tuned for approximately 30 nm when a bias of up to 25 V was applied. The maximum shift of 30 nm corresponds to less than 2% change in the length of the unbiased cavity (1520 nm).

The exact FWHM of the resonance dip could not be measured. The relatively low spectral radiance provided by the light source limited the resolution of the measurements to 2 Å. The recorded width of the resonance dip was between 2.5-3 Å. In order to resolve the shape of the dip, measurements with higher resolution will be performed, using a tunable laser source.

The filter is intended to be used in a tunable detector. An attractive solution is to integrate the detector in the Fabry-Perot resonant cavity (7). In this case, the absorption in the detector will have a broadening effect on the resonance of the filter.

Transversal modes in the cavity could change significantly the transfer function of the filter. The transversal modes will contribute with resonance dips at wavelengths shorter than the fundamental wavelength of the cavity. The spacing between the fundamental mode and the next one could be roughly estimated by considering that the field is restricted to the geometrical volume of the cavity (metallic wall approximation). The resonance wavelength corresponding to the (m,n) transversal mode, λ_{mn}, will be given by:

$$\lambda_{m,n} = \frac{\lambda_0}{\sqrt{1 + m^2\left(\frac{l_z}{l_x}\right)^2 + n^2\left(\frac{l_z}{l_y}\right)^2}}$$

where λ_0 is the fundamental resonance wavelength, l_z is the length of the cavity and l_x and l_y are the transverse dimensions. For $l_z=1.55\,\mu m$, $l_x=16\,\mu m$, $m=1$, $n=0$ and $\lambda_0=1550$ nm, one obtains $\lambda_{10}=1543$ nm. This result shows that a resonance due to the transversal modes could exist at few nm only from the fundamental resonance. The distance between the fundamental and the next resonance dip could be increased by shrinking the (effective) transverse dimensions of the cavity.

V. Conclusion

In conclusion, we have demonstrated a 30 nm tunable Fabry-Perot filter manufactured by selective wet etching of InGaAs/InP epitaxial layers. The filter is compatible with the InGaAs based photodiodes and work is in progress for manufacturing a tunable detector based on this Fabry-Perot filter.

Acknowledgment

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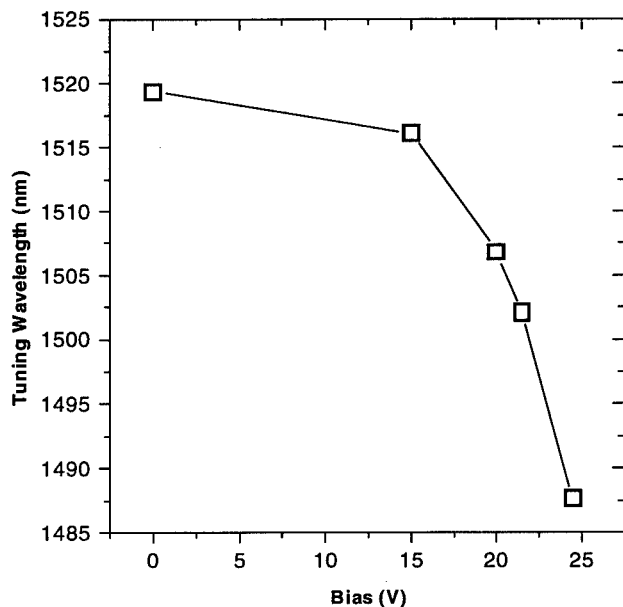
Fig. 4 Tuning of the resonance wavelength of the Fabry-Perot filter as a function of the bias voltage.

OXYGEN CONTROL IN Al-BASED III-V EPIWAFERS BY SIMS FOR YIELD IMPROVEMENT

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Epitaxial growth is a key step for III-V device fabrication. The incorporation of unintentional impurities such as oxygen, carbon hydrogen and metals in epiwafers can affect and degrade the device performance. These impurities can not be measured quantitatively and directly by non-destructive techniques, yet the qualification of epiwafers is essential in the control of precess technology and yield enhancement. SIMS (Secondary Ion Mass Spectrometry) depth profiling can provide this information, as well as information about dopants, alloy composition, thickness and interface quality. The fact that SIMS is a destructive technique and generally considered as expensive, high expertise, and sometime difficult technique has prevented its routine use as an on-line control technique.

In this paper, we show a very successful example of SIMS control to qualify epiwafers for the control oxygen contamination. It is known that oxygen in III-V compounds can compensate dopants and reduce the luminescence efficiency and that the oxygen contamination is a common problem in MOCVD growth of Al-based III-V compounds. Since Al is highly reactive with oxygen, even a very small amount of oxygen in growth system can result a high oxygen contamination. The cause of the oxygen presence is a complex problem and it can come from different sources such as system leakage, memory effects and contaminated source. The tolerance of oxygen contamination can be from low 1E16 to high 1E18 atoms/cm3 depending upon the device type. The challenge for SIMS analysis is to routinely keep such low detection for oxygen and to provide consistent measurements. A protocol for this purpose has been developed. The figure shows a of oxygen detection limits in AlGaAs over 40 weeks, obtained with a Cameca instrument. The implication of such control for LED, Laser and HMET production yield will be presented. The possiblity of analyzing up to 4" wafers by SIMS will be discussed.

HEAVY-HOLE EFFCTIVE MASS AND VALENCE BAND OFFSET ESTIMATED BY CONFINED STATES IN In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As MULTI-QUANTUM WELL STRUCTURES

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Introduction

Interband optical transitions of In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As multi-quantum well structures were observed at room temperature in photocurrent spectra under applied bias voltages. Photocurrent spectra had steplike structures and excitonic resonance peaks corresponding to confined states in quantum wells. A heavy-hole effective mass and a valence-band offset were estimated to be 0.39 m_0 and 0.22 eV by departure from the square-law dependence of confinement energies on heavy-hole quantum numbers.

I. Background

In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As multi-quantum wells (MQWs) lattice-matched to InP substrates have long been studied for application to optoelectronic devices. The two-dimensional exciton resonance have been studied by various means like optical absorptions, photoreflectances, and photocurrents for these 10 years. Parameters for this material system so far reported were ranging. A heavy-hole effective mass and a valence-band offset were distributed between 0.37 and 0.50 m$_0$ and between 0.18 and 0.28 eV[1]-[5]. Numbers of observed states were small on past experiments. So far, confined states near bandedge has only been observed. Therefore band parameters cannot be estimated exactly enough. Photocurrent flows normally to the quantum well plane and carriers go over the MQWs barriers after dissociation of excitons. The peak current levels are modulated by the electric field because of the change in the tunneling probability in the barriers. In this paper, we report steplike structures in photocurrent spectra as well as estimations of a heavy-hole effective mass and valence-band offset in In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As
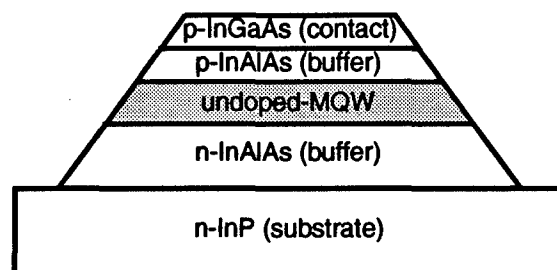
Fig. 1. A structure of a specimen with InAlAs p-i-n junctions including InGaAs/InAlAs MQW layers.

MQWs. The peak assignment was based on steplike structures of spectra and a particle-in-a-box model calculation.

II. Experimental

InAlAs p-i-n junctions including InGaAs/InAlAs MQW layers were grown by MBE on a (100) surface
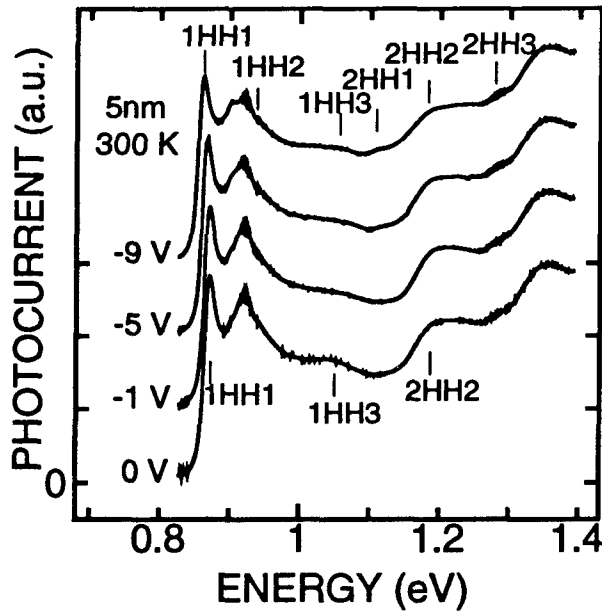
Fig. 2. Photocurrent spectra measured at room temperature in various bias voltages. Minus signs indicate reverse biases.

of n-type InP substrate, as shown in Fig. 1. The width of the InGaAs well and the InAlAs barrier in the MQW layers were 5 nm and 10 nm. The numbers of quantum wells (QW's) were 33. Photocurrent signals were measured as a function of wavelength at room temperature. During the measurements, reverse bias voltage was applied between the p-i-n junction. A metal probing needle was used as an electrode contacting the heavily-doped p^+-$In_{0.53}Ga_{0.47}As$ layer on top of the p-i-n junction. A metal base under the n-type InP wafer was used as a counter electrode.

III. Results and Discussion

Photocurrent spectra were measured in four different biases at room temperature, as shown in Fig. 2. The photocurrent spectra were normalized by wavelength-dependent photo-response of an InGaAs bulk detector. The spectra had steplike structures corresponding to the quantum level formation throughout entire spectra. The structures consisted of the absorption edges and plateaus of each subband originated from the two dimensional density of states [6]. Major combinations of the edges and the plateaus in Fig. 2 corresponded to the two dimensional interband transitions.

Peaks corresponding to the allowed transitions were generally seen clearly in a small electric-field spectrum. On the other hand, peaks originated from forbidden transitions become bigger and sharper when increasing electric field [7]. Types of the transitions were labeled by

using the notation $nHHl$, where n and l were principal quantum numbers of the conduction- and the valence-subbands and the HH stands for the heavy-hole subband.

Absorption edges of the MQW layers were about 0.87 eV. The spectra had a clear peak of the heavy-hole excitons attributed to the ground state transitions, 1HH1. A big peak, 1HH1, and a big hump, 2HH2, around 1.2 eV seen at a zero-bias spectrum, were assumed to parity-allowed transitions. Then energies of the allowed transitions, E_{1HH1} and E_{2HH2}, were determined to be 0.87, 1.19 eV. As increasing reverse bias applied to the MQWs, the 1HH1 shifted to lower energy and become smaller and broader, owing to a quantum confined Stark effect (QCSE), while the exciton peaks remained resolvable. Peak of another allowed transitions, 2HH2, also become smaller and broader.

Other peaks became bigger and sharper at larger biases. These were assigned to be forbidden transitions. The energies of the forbidden transitions, E_{1HH3}, E_{2HH1} and E_{2HH3}, were 1.06, 1.11 and 1.28 eV at a -9 V bias spectrum. No peaks were seen at a higher quantum number ($l \geq 4$) in the valence-subband. The well potential may not be large enough to occur the fourth heavy-hole transition. The transition energies in the square potential were determined by extrapolating the peak energies to a zero bias. Uncertainty of the peak energies at small bias never gives any serious error to the extrapolated energies as the peak shift was proportional to the square of applied bias. The extrapolated energies to the zero bias spectrum E_{1HH2}, E_{1HH3}, E_{2HH1}, E_{2HH3} and E_{3HH1} were 0.94, 1.04, 1.12 and 1.29 eV, respectively.

Based on the theoretical calculation using a infinite potential well, the l-th energy level of the heavy-hole, $E_{HH}(l)$, is proportional to the square of heavy-hole quantum number, l [8],

$$E_{HH}(l) = l^2 E_{HH}(1). \qquad (3.1)$$

In case of a finite well, the above square-law (3.1) holds approximately. In these interband optical absorptions, the above (3.1) is applicable to the ground and the second conduction subbands, $n=1$ and $n=2$. Therefore, the experimental values of $(E_{2HHl} - E_{2HH1})$ and $(E_{1HHl} - E_{1HH1})$ will give the $(l^2-1)E_{HH}(1)$. These energy levels were plotted against the square of quantum numbers in the valence-subband, l, in Fig. 3. These three levels were not fitted on a straight line. The energy of the third level was smaller than energy level expected from the square-law (3.1). The departure between the observed and the expected energy levels was caused by a phenomenon that the energy level was very close to the top of the well. The other explanations are the nonparabolicity of the heavy-hole subband or the mixing of the light- and heavy-hole subbands. Assuming that influence of the nonparabolicity or the band mixing was small, the heavy-hole effective mass, m_{hh}^* and the band offset, ΔE_v, in valence-subband can be

120
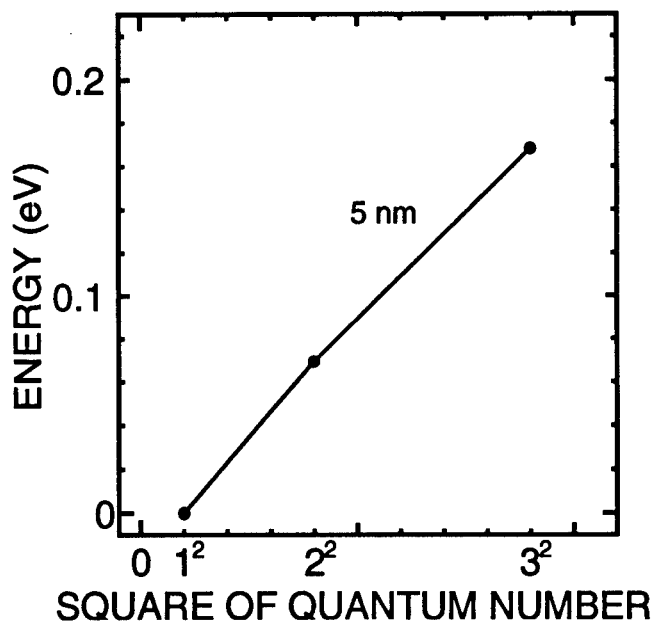
Fig. 3. Energy level differences. Differences of extrapolated energy between each energy level and the ground-state were plotted as a function of square of corresponding quantum numbers, l .

Fig. 4. Correlations of the effective mass ratio and the valence-band offset. Three lines intersect at one point.

estimated from the departure of the energy level near the top of the well. The difference between each energy level, $E_{HH}(2) - E_{HH}(1)$, $E_{HH}(3) - E_{HH}(1)$ and $E_{HH}(3) - E_{HH}(2)$ were 68.4, 167.3 and 98.9 meV, respectively.

The heavy-hole effective mass ratio and the valence-band offset were calculated using a particle-in-a-box model. We solved a following equation [9] with no contradiction for the above energy differences.

$$\tan(\frac{\sqrt{2m_{hh}^* E_{HH}}}{\hbar} \frac{L_z}{2}) = \frac{m_{hh}^*}{m_{bhh}^*} \sqrt{\frac{\Delta E_v - E_{HH}}{E_v}} \qquad (3.2)$$

The L_z refers to the thickness of InGaAs wells. The m_{hh}^* and m_{bhh}^* were the heavy-hole effective masses of the InGaAs well and the InAlAs barrier. E_{HH} was the energy level of the heavy-hole. ΔE_v was the valence-band offset. The parameters used in this calculation were m_{bhh}^*=0.41 m_0 [10] and the energy differences. The m_0 was the free electron mass. The valence band offset was estimated by varying the effective mass of heavy-hole in the well from 0.30 m_0 to 0.50 m_0 using (3.2).

Relations between the effective mass ratio of the heavy-hole and the valence-band offset are shown with three kinds of lines in Fig. 4. Three lines intersect at one point. The effective mass ratio and the valence-band offset were 0.39 m_0 and 0.22 eV. An error range of the effective mass and the valence band offset were about 0.04 m_0 and 0.03 eV because of experimental accuracies.

IV. Summary

In summary, by the photocurrent spectroscopy interband optical transitions of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ multi-quantum well structures were observed at room temperature under applied bias voltages. The photocurrent spectra, that the optical transitions were observed at, had steplike structures corresponding to the quantum level formation. The band parameters were estimated by a particle-in-a-box model calculation. The effective mass of heavy-hole (InGaAs well) and the valence-band offset were estimated to be 0.39 m_0 and 0.22 eV, according to the closeness of the confinement energy to the top of well.

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Optical Determination of In$_x$Ga$_{1-x}$As Composition on InP
Using a Fabry-Perot Test Structure

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Previously we reported on an ex-situ optical reflectance technique for determining precise epilayer thicknesses[1] and Al$_x$Ga$_{1-x}$As composition[2] using a Fabry-Perot test structure. The use of the test structure with the resulting high reflectivity modulation was critical for obtaining the high precision. In this paper, we extend the technique to determine the composition and the lattice mismatch of In$_x$Ga$_{1-x}$As epilayers grown on InP substrates. In our technique, a stack consisting of 7 pairs of In$_x$Ga$_{1-x}$As /InP and a cavity layer are grown on an InP wafer. The optical reflectance spectrum from a 2mm spot is then measured and fitted to a transfer matrix model to extract the composition and thickness. A typical spectrum showing the experimental and fitted curves is shown in Fig. 1.

The selection of the wavelength range of 1600 nm - 2200 nm was critical for extracting the In$_x$Ga$_{1-x}$As properties uniquely. It is the variation of the index of refraction in this range that insures that the optical thickness (= nd, where n is the index and d is the actual layer thickness), the quantity actually determined in the reflectivity measurement, is unique for each In$_x$Ga$_{1-x}$As composition. The reflectivity results was confirmed by comparing the simulated and experimental X-ray rocking curves.

In Fig.2, we show the effect of variation in In$_x$Ga$_{1-x}$As composition ($\pm1\%$) on reflectance spectrum. Our error analysis indicates that this reflectivity technique is capable of determining the In$_x$Ga$_{1-x}$As composition with an accuracy of $\Delta x \sim \pm0.053\%$. This is more than adequate for the determination of lattice mismatch ($\Delta x \sim \pm1.4\%$) for the In$_x$Ga$_{1-x}$As/InP system.

The advantage of using this reflectance fitting technique over other conventional methods is the simplicity of the instrumentation and the potential for fast measurement speed ($\sim$1sec. per point). The fast measurement speed would allow for routine wafer uniformity mapping. The advantages of being able to do routine maps versus single point measurements are discussed. Fig. 3 and 4 show mappings of the thickness and composition of In$_x$Ga$_{1-x}$As on a 2" wafers to demonstrate the utility of the technique.

Fig.3 InGaAs Composition Map
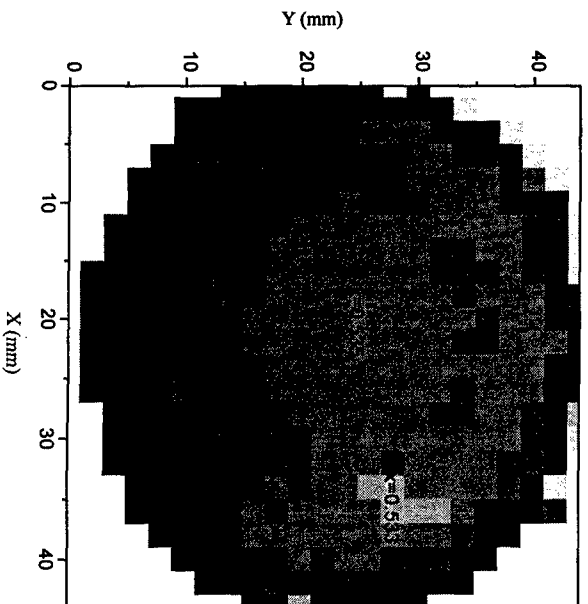
Fig. 4 InGaAs Layer Thickness Map
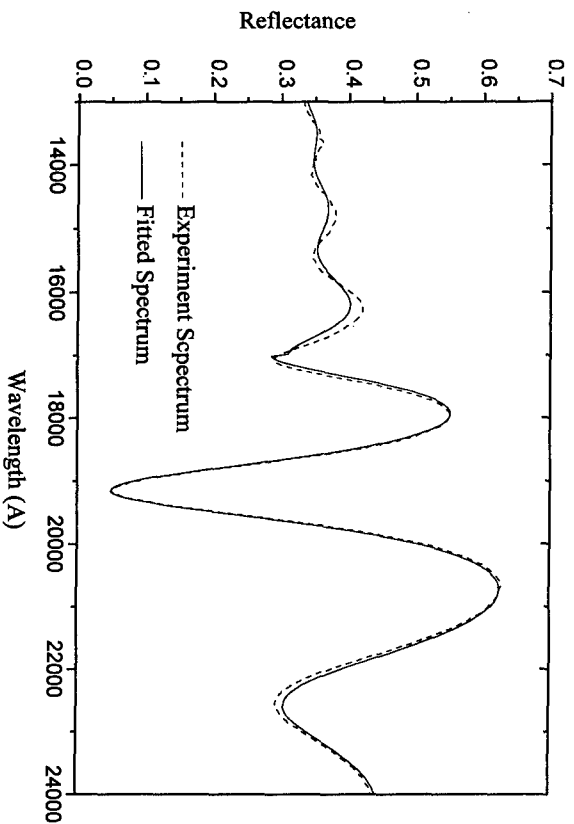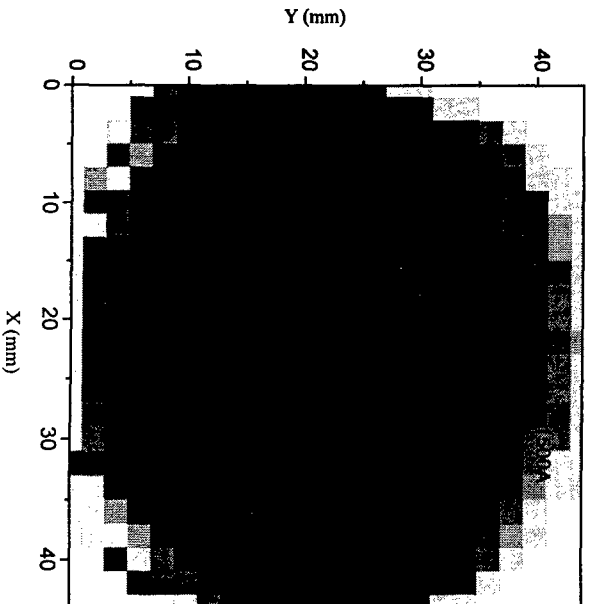
Fig.1 Experimental and fitted reflectance spectrum from 7-pair InGaAs/InP stack with InGaAs cavity layer.
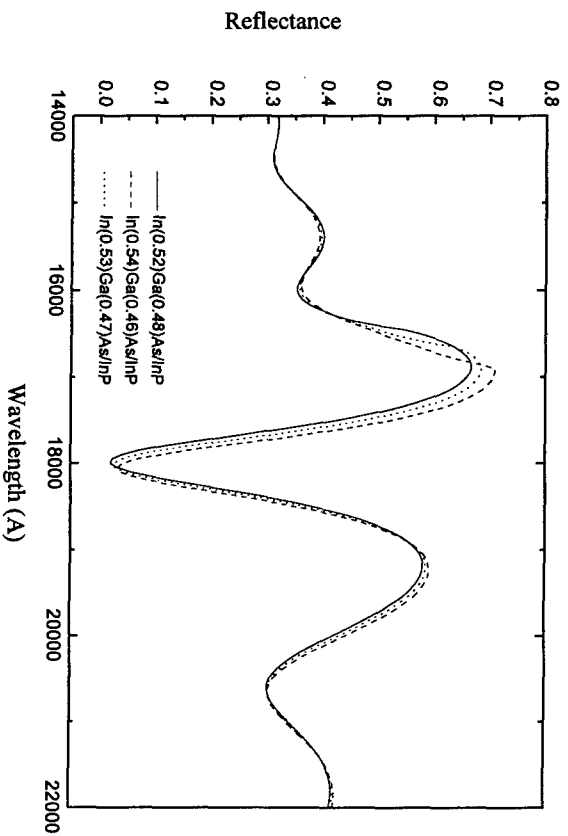
Fig. 2 Simulated reflectance spectra for InGaAs/InP stack with +/- 1% variation of In composition.

124

A STUDY OF BUFFER LAYERS IN A DOUBLE CHANNEL InP-HFET STRUCTURE.

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Introduction

Extremely high frequency performances have been reported on InP Field Effect Transistor [1]. These devices are usually grown by molecular beam epitaxy. The use of the metal organic vapor phase epitaxy offers interesting prospect for their fabrication. However specific problems are related to the growth of an insulating buffer layer under the FET channel. One solution consists in growing low temperature InAlAs or semi-insulating materials such as Fe-doped InP: high resistivity is obtained due to the concentration of deep centers. We have measured the parasitic effects generated by the InAlAs buffer layers on drain current transients, low-frequency transconductance, output conductance. Investigation on emission-type transient by isothermal current relaxation technique has supplied information on trap signatures.

I. Motivation

In recent years, much effort has been made to develop InP-based Optoelectronic Integrated Circuits (OEICs) for optical communications in the 1.3 μm to 1.5 μm wavelength range. InP-based HFETs are used in pinFET receivers as well as in modulator drivers. However, III-V electron devices are submitted to parasitic effects related to the trapping of charge carriers and to the modification of charges by impact ionization. These effects penalize the monolithic integration [2,3] or its system applications [4]. In this paper we report results about the parasitic effects in a InGaAs/InP double channel HFET made by MOVPE.

Gate and drain transients have been investigated together with the frequency dependence of the transconductance and of the output conductance in the vicinity of the kink. The low frequency drain current noise spectra and the frequency dispersion are the consequences of traps. The measurement of drain currents with temperature provides hints to the origin of those traps.

We have studied the double channel since it combines the high mobility of InGaAs at low electric field with the low impact ionization coefficient of InP at high electric field. This type of structure is designed to reach high drain voltage with a minimum gate current, with high mobility in the channel and in the access regions.

II. Details on the HFET structure

The layers were grown on (100) semi-insulating InP(Fe) substrate in the following order :

1) 50nm InAlAs buffer layer,
2) 25nm InP doped channel,
3) 2nm InP spacer layer,
4) 5nm InGaAs undoped channel,
5) 50nm InAlAs undoped barrier layer,
6) 50nm doped InGasAs cap for improved ohmic contacts (Fig. 1).
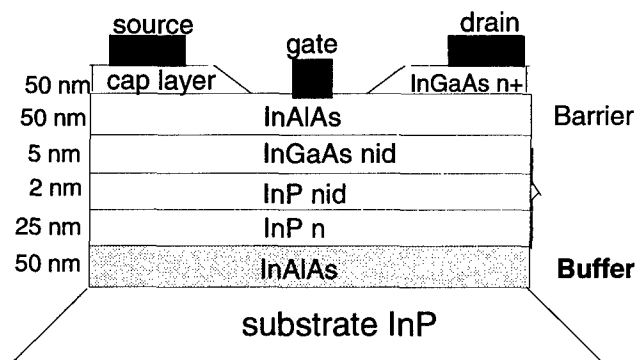
Fig. 1: MOVPE structure of HFET (Structure B).

The InAlAs buffer layer consists of 30 nm grown at 500 °C and 20 nm grown at 650 °C. The value of the sheet resistance of the low temperature InAlAs layer is

of the order of 10 MΩ/□ while for buffer layers grown at 650 °C, it is much smaller, of the order of 50 kΩ/□.

The ouput and gate current characteristics Id(Vds,Vgs) & Ig(Vgs,Vds) of the double channel InGaAs/InP-HFET are shown on Fig. 2 and Fig. 3. Sample B has been grown at optimized substrate temperatures and layer thicknesses.

Typical values of current gain cut-off and maximal oscillation frequencies for 0.8 μm gate devices are ft/fmax = 15 GHz/ 60 GHz. The improved kink and gate leakage of sample B will be discussed below. Earlier structure, sample A, characterized by a thinner InAlAs barrier layer (30nm) and a thinner InAlAs buffer layer (40nm) is compared to the improved structure.

III - Kink effect and gate leakage

The kink effect corresponds to a sudden rise in the drain current slope at a certain drain-to-source voltage (Vkink) (Fig. 2).

Possible mechanisms are:

- kink effect created by interface states and traps[5].
- kink effect induced by impact ionization[6].
- kink effect generated from hole pile-up at a potential barrier in the source of the device[7].

Only our initial technology (sample A) had a pronounced kink effect.

The gate leakage current of sample A was so important that it hides the impact ionization as shown by the characteristic Ig-Vgs curves (Fig. 2).

Id(mA)

Ig(μA)

Fig. 2. Id(Vds, Vgs) and Ig(Vgs, Vds) of InGaAs/InP channel HFET A
(100μm gate width, 0.8μm gate length).
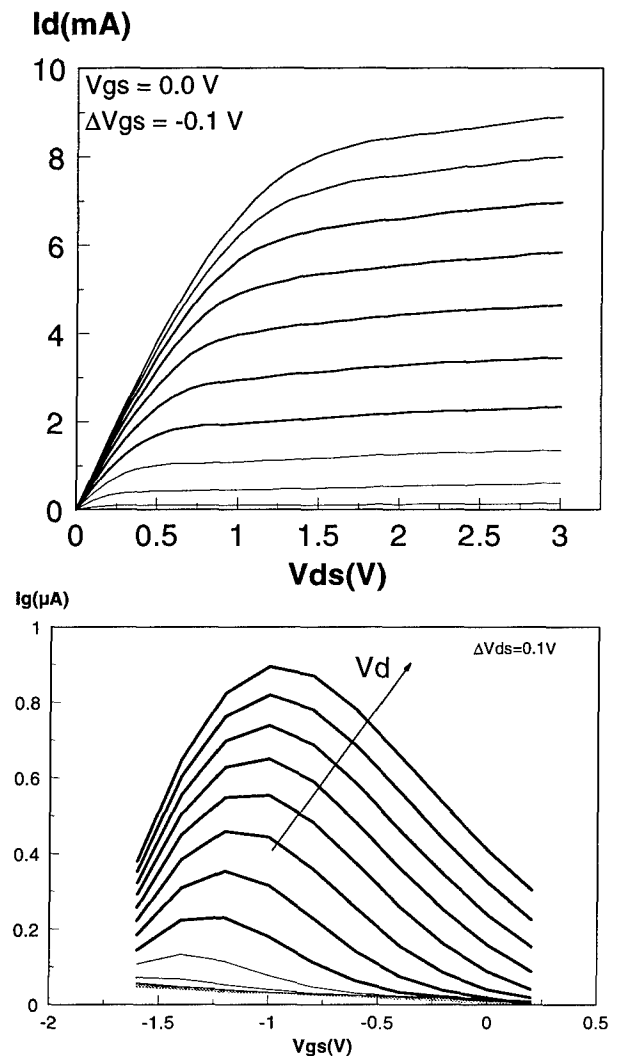
Fig. 3. Id(Vds, Vgs) and Ig(Vgs, Vds) of InGaAs/InP channel HFET B
(50μm gate width, 0.8μm gate length).

126

In the second device (type B), the gate current is mainly due to impact ionization as shown by the bell-shaped characteristics Ig-Vgs (Fig. 3). The 50nm barrier layer leads to a better structure.

IV - Drain lag measurements:

Voltage pulses are applied to the drain keeping the gate-source voltage constant (Vgs = -0.2 V). In the saturation region, at Vds = 1 V (below kink) the effect of the drain lag on the pulse voltage can be seen for sample A with an overshoot for the leading edge and with an undershoot for the falling edge (Fig. 4). The measured emission-type time constant varies between 0.1 µs and 1 ms because of the presence of several levels of traps. The response is of a multiexponential type.

Fig. 5 : Drain current transient above kink (sample A).

At voltages Vds > 4V, the transient effects decrease strongly.

The % drain lag on the pulse voltage for sample B has dropped (Fig. 6), for both below and above kink regimes.

Fig. 4 : Drain current transient below kink (sample A).

Above kink at Vds = 2 V (Fig. 5), the transients in the current pulse are inverted. The simplest model assumes the effect of traps in the buffer :

a) At low electric field, the leading edge of Vds corresponds to the capture of electrons emitted by the source. The negative charge accumulates with a time constant of the order of 1µs and pinches the channel.

b) At large electric field (Vds > Vkink), the buffer potential does not follow Vds and a front edge leads to the emission of electrons from the buffer to the drain.

The buffer layer loses its negative charge and that explains the reverse behavior of the transient current (Ids(t)) (Fig. 5). Capture of holes generated by ionization is the other possible cause of this form of transient.

Fig. 6 : Drain current transient below kink (sample B).

V - Frequency dispersion of Gm, Gd

The frequency dispersion of the transconductance Gm is very small. On the other hand, the frequency dispersion of the drain conductance is significant. Measurements have been done at two different biases over 8 decades of frequencies using: a LCR multi-frequencies bridge (10 Hz - 1 MHz), and a network analyser (30 kHz - 6 GHz). For Vds = 1 V in the

saturation region below kink, we observe a monotonous increase of Gd(f) over the 8 decades (Fig. 7).
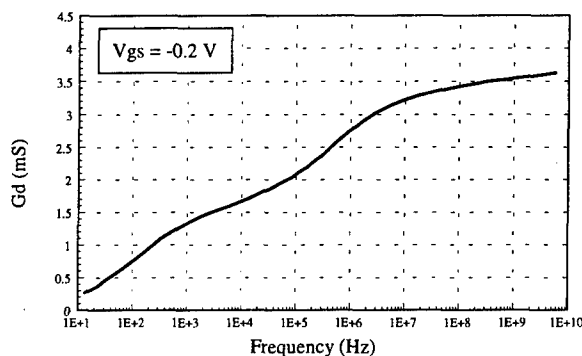
Fig. 7 : Drain conductance dispersion Gd(f) below kink voltage.

At Vds = 3V, above kink, Gd(f) shows a minimum near 30 MHz followed by a less pronounced increase (Fig. 8).
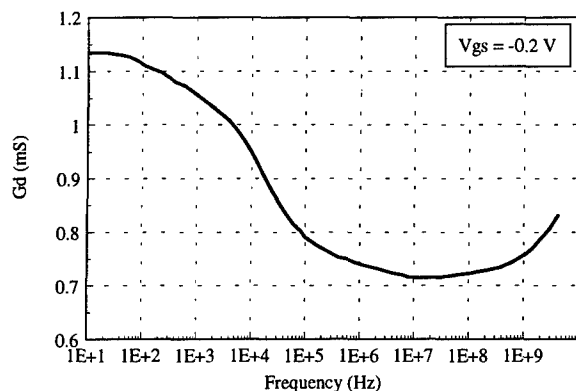
Fig. 8 : Drain conductance dispersion Gd(f) above kink voltage.

The inversion of the Gd(f) slope at low frequency depending on the bias voltage with respect to the kink voltage is consistent with the sign inversion of the drain lag. A comparaison between sample A and B shows a significant improvement for the second structure. At a pre-kink bias point, the 68% drain lag drops to 40% and the 360% $\Delta Gd/Gd_{av}$. to 60%. In the post-kink region, the 24% drain lag drops to 11% and the 58% $\Delta Gd/Gd_{av}$. to 50%.

VI - Isothermal current relaxation on traps signatures

The emission-type transient illustrated in Fig. 4 has been studied by means of isothermal current relaxation between 80 K and 350 K [8]. One major electron trap signature is found in the InAlAs buffer layer with an activation energy of 0.28eV and a capture cross-section of $2.0 \ 10^{-18}$ cm^2.

VIII - Conclusion

We have observed parasitic effects due to slow traps located at the channel-buffer interface, in the buffer side. For a bias point below the kink voltage in saturation region, the traps capture electrons. Above the kink voltage but close to kink, the traps emit electrons and/or capture holes provided by impact ionization. Gd spectroscopy shows the presence of an important density of traps in the buffer layer on a broad frequency band.

This type of analysis makes it possible to search for a good compromise between the high electrical resistance of buffer layers [9-10] and their parasitic effects. The parasitic effects can be reduced to a minimum by controlling the thickness and the growth temperature of the buffer layer. The presence of the thicker (20nm instead of 10 nm) 650 °C InAlAs buffer layer has allowed better electrical results.

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Photoreflectance Mapping of InGaAs HEMT Wafers

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Introduction

Screening of device epilayers is now accepted as a critical issue in the research and development of high-performance semiconductor devices. Photoreflectance (PR) is very attractive for this purpose, since the composition and the built-in dc electric field of wafers can be estimated by analyzing the Franz-Keldysh oscillations (FKOs) in the PR spectra.[1] Additionally, the laser excitation used is extremely weak which makes this method effectively non-invasive.[2,3]

Despite of these advantages, to our knowledge, on-wafer mapping by PR has not been reported. This paper presents PR mapping equipment and its application to InAlAs/InGaAs HEMT wafers. We visualize the non-uniform composition of InAlAs layers to show that PR mapping is a powerful tool for noninvasive wafer screening.

I. Experimental

PR experiments were performed using a standard setup. The probe beam supplied by a monochromatic tungsten halogen lamp was focused on a wafer to the diameter of 1 mm and the reflected light detected by a Si or Ge p-i-n diode. The pump beam, whose diameter was 5 mm, was supplied by a He-Ne laser chopped at 66 Hz. The mapping of the $\Delta R/R$ intensity was performed by scanning the wafers on an X-Y stage at room temperature. The samples were InAlAs/InGaAs HEMTs grown on InP substrates by MOVPE. The layer structure of the samples is shown in Fig. 1.

		Thickness	
		wafer A	wafer B
Ohmic contact	n-InGaAs	120 Å	120 Å
Ohmic contact	n-InAlAs	170 Å	170 Å
	i-InAlAs	30 Å	30 Å
Recess etch stopper	i-InP	50 Å	50 Å
Carrier supply	i-InAlAs	60 Å	50 Å
	i-InAlAs	30 Å	40 Å
Channel	i-InGaAs	150 Å	150 Å
Buffer	i-InAlAs	1967.5 Å	955 Å
	p-InAlAs	12.5 Å	25 Å
	i-InAlAs	20 Å	20 Å
	InP-Substrate		

Si planar doping → Carrier supply

Fig. 1. Layer structure of samples.

II. Results and discussion
A. PR spectra from the HEMTs wafers

Figure 2 (a) shows PR spectra from two different InAlAs/InGaAs HEMT wafers (A and B). These spectra were measured at position X in Fig. 2 (b). The FKOs were clearly observed in each spectrum. These FKOs originate from the InAlAs layers because the fundamental edge (E_0) of the InAlAs layers corresponds to this energy range. We plot the energy of the peak and valleys denoted a, b, and c in Fig. 2 (a) as a function of F_j where j is the index of the peak and the valleys and F_j is given by

$$F_j = \{3\pi[(j-\frac{1}{2})\frac{1}{2}]\}^{\frac{2}{3}}.$$

This draws a straight line whose slope is proportional to the built-in dc electric field F
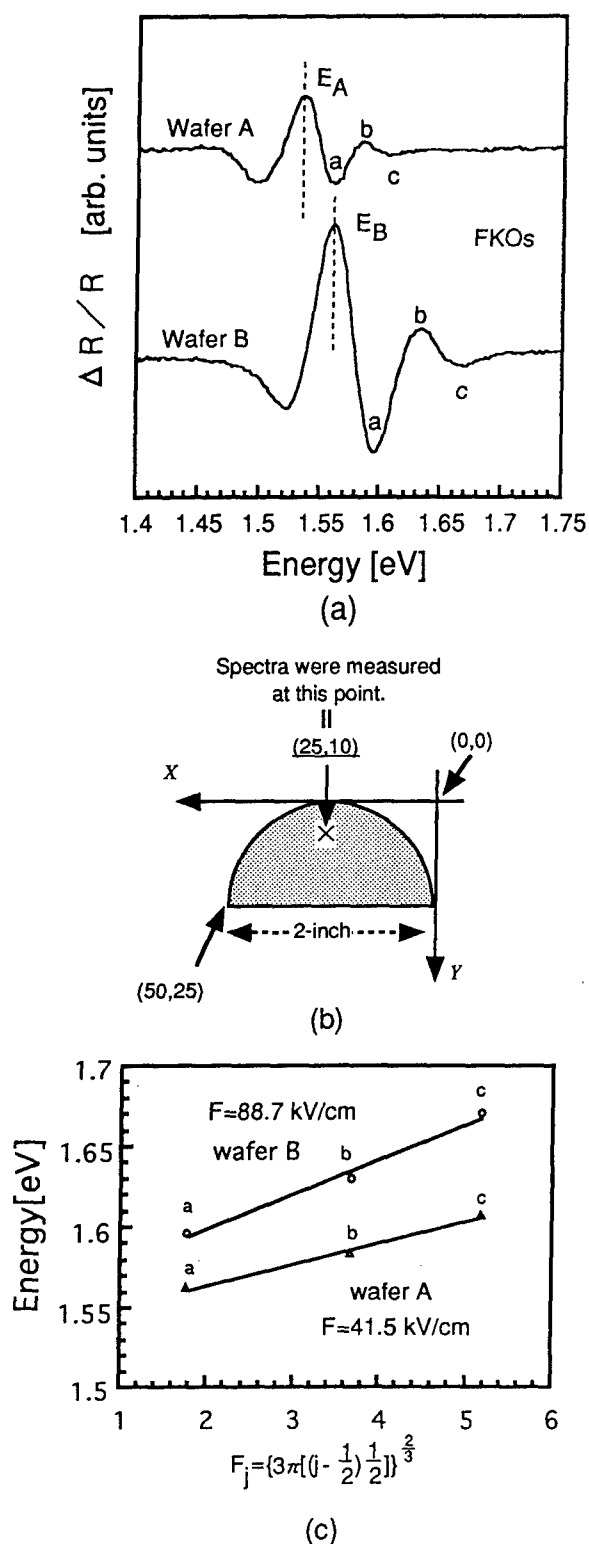
Fig. 2. (a) PR spectra of wafer A and B.
(b) Schematic of the posion where the spectrum was measured. (c) Determination of built-in electric field F.

as shown in Fig.2 (c). At position X, the built-in electric field of wafer B is higher than that of wafer A.

Here, the energy of maximum peaks in each spectrum is marked as E_A and E_B, respectively. Those from the interface between the InAlAs layer and the InP substrate could be detected as well. Peaks E_A and E_B should be located near the E_0 peaks of these InAlAs layers but were not exactly equal to E_0 because of a broadening factor.[4] For convenience, we used E_A and E_B instead of E_0 peaks. It is found from Fig. 2 that the E_B peak is about 27 meV higher in energy than E_A, which corresponds to the higher composition of Al in wafer B by +1% than that in wafer A at this particular position. This indicates that this PR method is highly sensitive to the alloy composition of the wafers.

Unfortunately, the InAlAs layers above the InP-recess etch stopper (20 nm) were so thin that we could not detect PR signals from these InAlAs layers. In principle, there should be two built-in dc fields in the InAlAs buffer layer: Those from the InAlAs buffer/InP substrate (bottom) interface and from the InGaAs channel/InAlAs buffer (top) interface. It was not clarified yet which dc field dominates the PR spectra.

The composition of a InAlAs wafer can be estimated from its PR spectrum. The composition of several wafers was checked to confirm the validity of PR method. For some wafers, on-wafer shifts of the PR peak energy were observed. These results suggest the presence of on-wafer non-uniformity in alloy composition, built-in dc field, and/or the density of defects. In order to reveal this non-uniformity, we mapped PR signals from the wafers.

2-ich

wafer A

(a)

wafer B

1.53 eV

wafer B

(b)
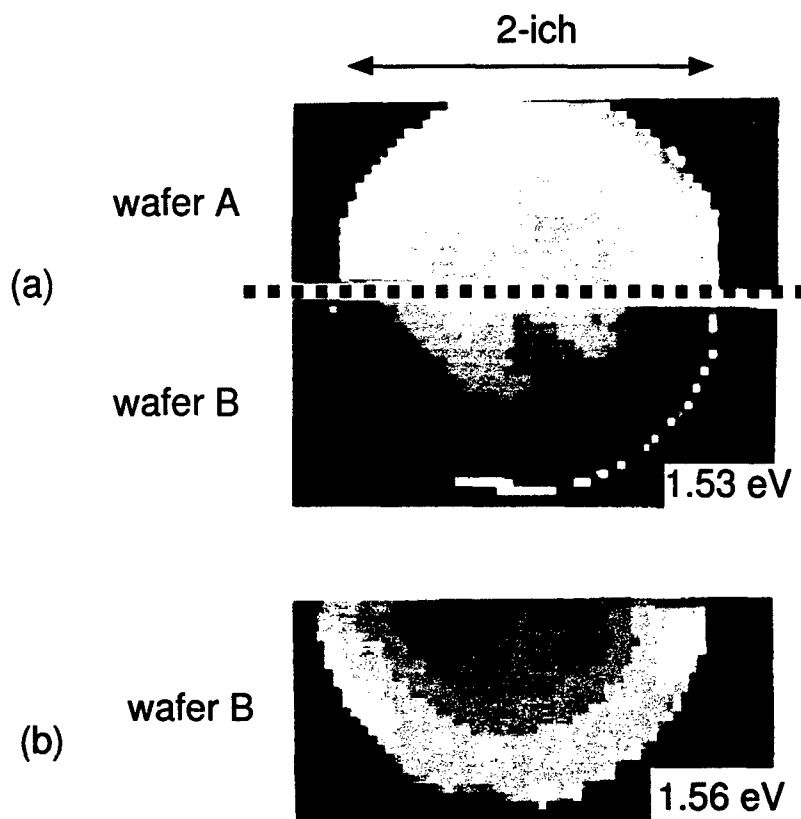
1.56 eV

Fig. 3. Maps of PR signals.
(a) At 1.53 eV (E_A) (b) At 1.56 eV(E_B).

B. PR mapping of InAlAs/InGaAs HEMT wafers

Figures 3 (a) and (b) show the mapping of the $\Delta R/R$ intensities of wafer A and B measured at 1.53 eV and 1.56 eV which correspond to E_A and E_B in Fig. 2, respectively. In Fig. 3 (a), the maps of the PR signals from wafer A and B are shown at the top and the bottom, respectively. Since the central part of wafer B has the same characteristics as is as bright as that of wafer A, the alloy composition of the center of wafer B is similar to that of wafer A $(In_{0.52}Al_{0.48}As)$. It is to be noted that concentric circles like contour lines can be seen in each map. The number of contour lines in wafer A is smaller than that in wafer B, suggesting poor alloy composition uniformity in wafer B.

In Fig. 3 (b), the peripheral region becomes brighter where the peak energy corresponds to E_B. The mapping of wafer B in Fig. 3(a) complements that in Fig. 3 (b). This indicates that the Al composition of the InAlAs layer in wafer B is higher in the peripheral region than in the central region. The difference in composition is estimated to be about 1 point from the difference in the peak energy of 30 meV, as noted above.

This method allows the uniformity of alloy composition in the InAlAs layers to be directly observed by on-wafer mapping of

PR signal intensity. The concentric contours could be related to non-uniform wafer temperatures during the growth process, but this remains to be clarified.

III. Summary

We have developed PR mapping equipment and applied it to InAlAs/InGaAs HEMT wafers. On-wafer non-uniformity of InAlAs layers has clearly been revealed by mapping PR signals. The non-invasive PR mapping method is very effective for screening epiwafers with device structures.

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Manufacturable InP-Based HBT Technology for Low Voltage Millimeter-Wave and Microwave Communications

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Introduction

A manufacturable InAlAs/InGaAs HBT and MMIC technology was developed for low voltage operation of communications. Materials quality control was achieved through photoreflectance technique, while critical device parameters were used in monitoring process uniformity and reproducibility. A few broadband MMICs and linear amplifiers based on statistical SPICE modeling in design accomplished new performance records, and InP-based power HBTs demonstrated promising power performance at L- and K-band frequencies.

I. Background

Recently, the quest for the solid state ICs for both space and mobile communication systems has been focused on monolithic microwave integrated circuits(MMICs) with a high frequency broadband response, low dc power consumption and low voltage operation, high data rate, low phase noise, high linearity, and high efficiency. InP-based Heterojunction Bipolar Transistors (HBTs) have been demonstrated with promising rf performance on many MMICs in our laboratories[1]. The materials and fabrication technology have become mature and reproducible due to simple device structures and an almost GaAs-compatible process. Most recent results from low voltage MMICs, such as direct-coupled amplifiers with high gain-bandwidth product[2], broadband distributed amplifiers[3], high IP3 Ka-band linear amplifiers[4], and 94 GHz VCOs[5] have established benchmarks in our development of communication circuits. All those state-of-the-art performance HBT ICs are fabricated with an optimized baseline epitaxial structure, grown by MBE, and manufacturable 1-μm HBT process technology using wet-etch with end-point control, conventional metal lift-off and PECVD SiN_x or SiO_2 dielectric passivation techniques. In this paper, we report the materials, process and MMIC technology, with emphasis on the manufacturable InAlAs/InGaAs HBT processes. Discussion on quality control and production-readiness is addressed. In addition, the latest low-voltage MMICs at microwave and millimeter-wave, as well as the power transistor performance at L- and K-band are reported.

II. InP HBT Materials and Device Technology

The base line epitaxial structures grown on 2" and 3" semi-insulating InP substrates consist of an n^+ $In_{.52}Al_{.48}As/p^+$-$In_{.53}Ga_{.47}As$ heterostrucutre with a 45 nm N-$In_{.52}(Ga_xAl_{1-x})_{.48}As$ compositionally graded base-emitter interface and an undoped $In_{.53}Ga_{.47}As$ spacer. The InGaAs base/collector homostructures are designed to the intended application in terms of doping profile and layer thickness. The as-grown device wafers were qualified prior to the MMIC fabrication using non-destructive optical characteri-

zation method such as photoreflectance. The built-in dc electric fields and energy band gaps are determined from the Franz-Keldysh oscillations, which in turns provide information of the carrier concentrations and compositions, respectively. The photoreflectance spectra from emitter region of the HBT have been used to monitor composition of the emitter and the amount of base dopant outdiffusion.[6] The spectra shown in Fig. 1, shown as an example, were measured from two HBT wafers grown 10 weeks apart. Both spectra show very little Be outdiffusion and very good material profile control for reproducibility.

The device wafers were then fabricated with stepper photolithography technique and automatic in-procss dc and rf testing were employed at first metallization and post-airbridge steps, respectively. The process steps of InP HBT MMICs are listed in reference 7 reported by Elliott et. al. in this proceeding.
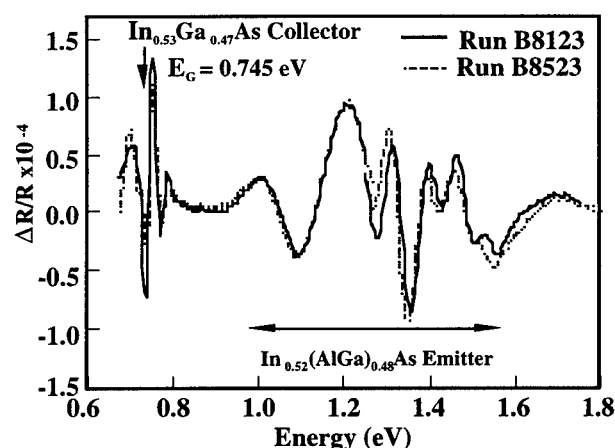
Figure 1. Photoreflectance spectra from two InGaAs/InAlAs/InP HBTs grown 10 weeks apart. The PR spectra shows that the collector and emitter structures are identical between the samples which establishes the repeatability of the MBE growth process.

III. HBT Device Modeling and MMICs

On-wafer S-parameter measurement was also applied on thinned wafers to identify rf functional MMICs. The critical device parameters such as emitter-base junction turn-on voltage, V_{be}, emitter resistance, R_E, and small signal current gain, β, as well as small signal S-parameters and derived H_{21} and maximum available gains (MAG) at selected frequencies were used in monitoring the uniformity, device yield, and reproducibility. Their variations within a 3"-wafer and from wafer-to-wafer are summarized in Table I. More importantly, a proper statistical device modeling effort (Fig. 2) was utilized to accurately extrapolate the intrinsic device parameters and verify the materials or process-sensitive factors in quality control.

The SPICE macro model[8] is composed of a Gummel-Poon bipoalr model and additional capacitances to represent stray capacitance between the device terminals (C_{BE}, C_{BC}, C_{CE}) and the capacitance C_{CG} of the collector region to the metalization on the back of the thinned wafer. The stray capacitances are estimated based on test structure measurements. The backside capacitance is calculated based on empirical fringing data[9]. The saturation currents I_S, I_{SE}, and I_{SC}, and the current gain β_F and β_R are matched to the DC characteristics of the device.
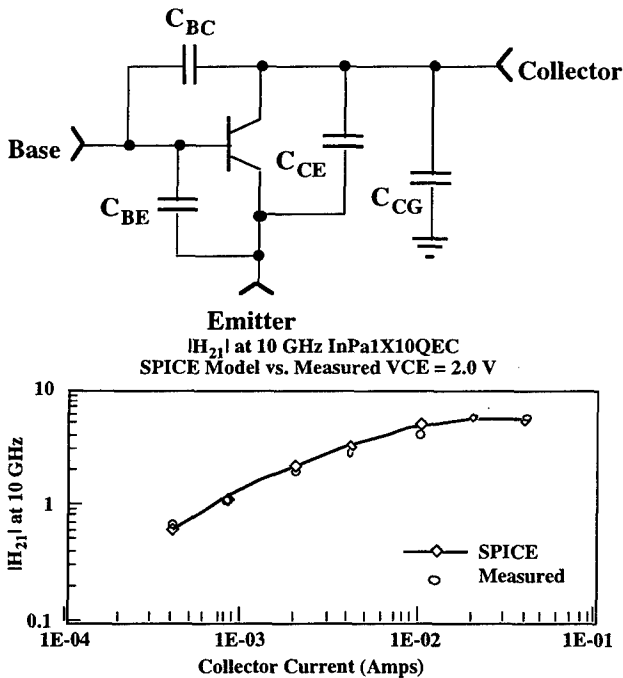
Figure 2. InP-HBT equivalent circuit schematic and comparison of SPICE macro model vs. Measured |H21| at 10 GHz. The model matches device characteristics of more than two decades of current and a wide range of bias conditions.

The junction capacitance is measured on large area structures and scaled to the device size. The emitter resistance R_E, base resistance R_B, the the total base-collector capacitance are directly extracted from the two port parameters which are measured over two decades of collector current. The remaining Gummel-Poon parameters are then fit to these measurements. The resultant model

matches device characteristics of more than two decades of current and a wide range of bias conditions (Fig. 2).
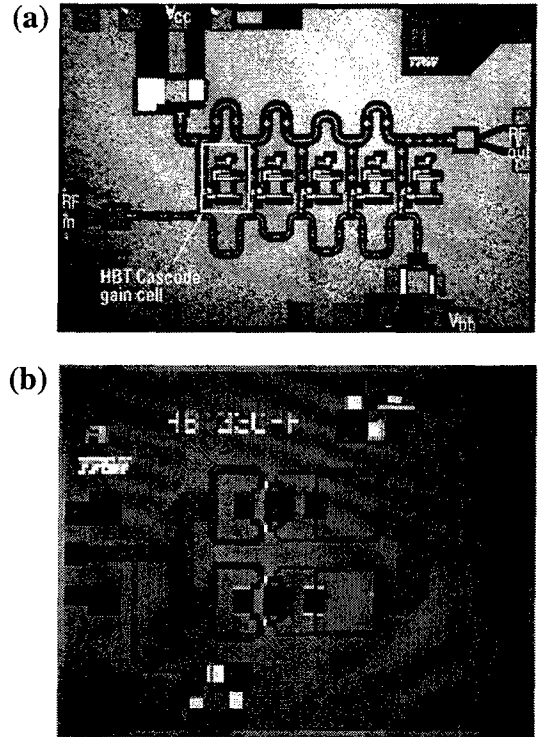
Figure 3. Photo pictures of InP-HBT MMICs; (a) distributed amplifier, (b) Ka-band linear amplifier.
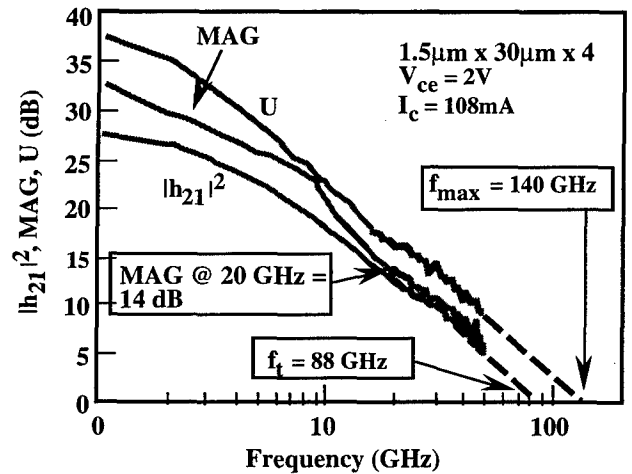
Figure 4. The magnitude of the current gain ($|H21|^2$), maximum satable gain (MSG), maximum abailable gain (MAG), and unilateral gain (U) as functions of frequency. A fT of 88 GHz, and a fMAX(unilateral) of approximately 140 GHz with 14 dB (MAG) at 20 GHz, are obtained from a four-finger power transistor.

Based on this InP-HBT technology, low-voltage broadband MMICs and linear amplifiers were designed and fabricated (Fig.3). A direct-coupled amplifier achieved 25 GHz bandwidth with a record of GBP/P_{dc} >3GHz/mW (GBP:gain band-width product) and a distributed amplifier with 50 GHz bandwidth was accomplished at a bias voltage of 4 V or below (Table II).

134
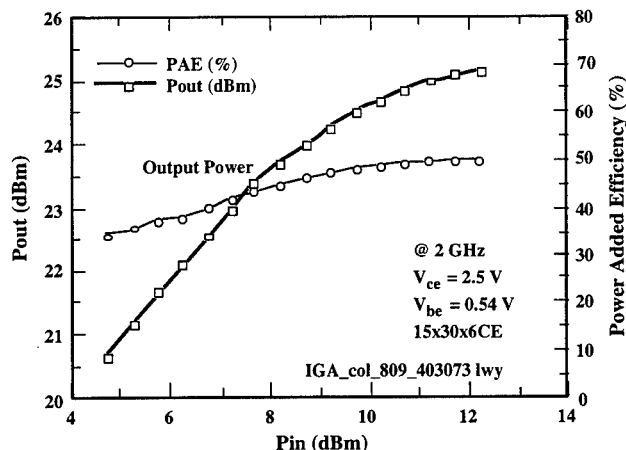
Figure 5. The RF power characteristics of a 6-finger
device (1.5x30x6 μm²) under CW operation at 2 GHz
and Vce = 2.5 V; the output power, PAE as functions of
input power.
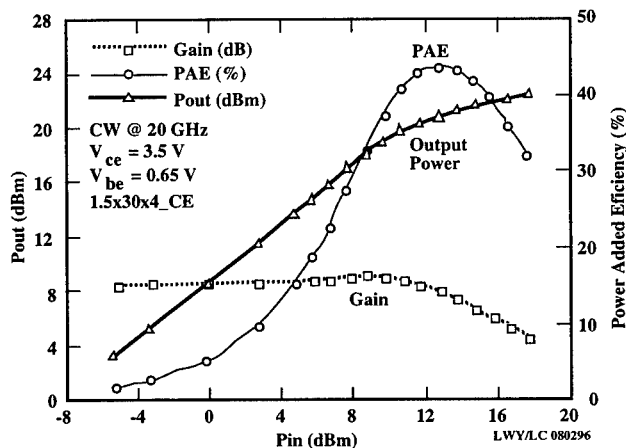
Figure 6. The 20 GHz microwave power characteristics of
and a 4-finger device (1.5x30x4μm²) under CW
operation; the output power, PAE and gain as functions
of input power.

IV. Microwave Power Performance

The power transistors with 700 nm InGaAs collector
have demonstrated very good I-V characteristics with β
≥20 at J_c of $1x10^4$A/cm² or higher. The device achieved a
reasonable breakdown, with both BV_{ceo} and BV_{cbo} > 8 V.
The base-emitter turn-on voltage at J_e of 1 kA/cm² is 0.63
V and the collector offset voltage is only 75 mV,
attributed to the properly designed and grown graded
interface at the emitter-base junction. The resultant low
knee voltage of ~ 0.7V provided a relatively large signal
swing to achieve high efficiency operations at a low V_{ce}
of 3 V. At V_{ce} =2.0 V and J_c = $6x10^4$ A/cm², a four-finger
transistor achieved a high frequency response with a
MAG of 14 dB at 20 GHz, and an extrapolated maximum
frequency of oscillation (unilateral) of ~140 GHz (Fig.
4).

High f_T and high f_{MAX} were simultaneously obtained
from the power transistor with only 1 dB gain reduction
at 20 GHz due to success in low-loss combining of the
two unit cells, each with a dual-finger HBT. Power
performance of a six-finger HBT at L-band delivered > 25
dBm power with 50% PAE at only 2.5 V(Fig. 5), due to
the advantage of low V_{be} and high current drive capability.
This result may provide a thrust for future low voltage
PCS wireless communication.

At 1 dB compression, a two-finger HBT achieved 9.5
dB power gain at 20 GHz with 17.8 dBm output power
and 40.3% PAE, and a four-finger HBT demonstrated 8.0
dB gain with 20.7 dBm output power and a peak PAE of
43.7%.(Fig. 6) These transistors achieved power
densities > 1 W/mm at a modest current density around
3.6 ~ 5.0 x10⁴ A/cm², and low bias voltages of 3.0 ~ 3.5
V, suitable for low voltage, high-efficiency linear
amplifiers.

V. Conclusions

A manufacturable InAlAs/InGaAs HBT and MMIC
technology was developed for low voltage millimeter-
wave and microwave communications. Materials quality
control was achived through the employment of
photoreflectance technique . The critical device parameters
such as emitter-base junction turn-on voltage, V_{be}, and
small signal current gain, β, as well as small signal rf
gains were used in monitoring the uniformity and
reproducibility. Low voltage broadband MMICs and
linear amplifiers based on statistical SPICE modeling
achieved new performance records. The low voltage InP
HBTs also demonstrated promising power performance at
L- and K-band frequencies.

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Table I. Selected device parameters of 3" InP-HBT for in-process control

Device Parameters[+]	E/B turn-on $(V)^+$		dc current gain β^+		Base Rho	H21[*]	H21[*]	MAG (dB)[*]
Unit or freq.	@ J_c (KA/cm²)		@ J_c (KA/cm²)		(ohm/sq.)	@10 GHz	@ 20 GHz	@20 GHz
Current or density.	J_c= 10	J_c= 40	J_c= 10	J_c= 40	420	I_c = 40mA	I_c = 40mA	I_c =40mA
Wafer average	0.722	0.785	12.8	22.4	2.6%	8.55	3.45	13.1
Variation(+/-σ)	0.003	0.002	10%	7.0%	426	1.4%	1.7%	1.5%
Lot average	0.730	0.792	11.8	21.1	1.2%	7.11	3.40	13.1
Variation (+/-σ)	0.011	0.010	4.7%	4.4%		1.7%	1.4%	1.5%

+; measured from 1x10 µm² (GSG_HA1x10-ADEPTZ11)
*; measured from 1.4x10x4 µm² (HA1.5x10QEF-ADEPTZ3)

Table II. Performance Summary of Selected InP-HBT Low Voltage Communication MMICs

MMIC Type	Op. Freq.	BW[+]	Bias	Gain	dc Power	Figure-of-Merit[*]		
	(GHz)	(GHz)	(V)	(dB)	(mW)	GBP/Pdc	ETBP	IP3
Direct-Coupled Amp.	dc ~ 25	> 22	3.0	15.1	34.2	3.66 GHz/mW	5.8 THz-Ω	> 6 dBm
Direct-Coupled Amp.	dc ~ 25	25	4.0	18.6	69.2	3.04 GHz/mW	8.8 THz-Ω	> 10 dBm
Distributed Amp.	2 - 50	50	4.0	4~6.3	89	effective trans. impedance = 39.2 dB-Ω		
Ka Linear Amp.	35	~ 5	2.3	5.0	108	IP3/ Pdc = 4.1		26.5 dBm

[+] BW: Bandwidth
* GBP: gain-bandwidth product, Pdc: dc power in W, ETBP: effective trans-impedance-bandwidth-product

SELECTIVE GATE RECESS RIE ETCHING BY CHF3+BCl3 IN InAlAs/InGaAs HEMTs

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Introduction

The selective dry etching between InGaAs and InAlAs is an essential process for gate recess in InP-based HEMT fabrication, which means that the top n^+-InGaAs layer must be etched away, and the etching process is terminated at the underline InAlAs Schottky layer[1-4]. This etching selectivity between two materials can be realized by the reactive ion-etching, which is not always available from the conventional chemical etching approach. In order to achieve this selectivity, the mixture of CHF3 and BCl3 gases was proposed in this study to replace the role of CCl_2F_2[1], which has an undesirable impact on the environment. This gas mixture approcah has been proven in our previous studies that a high selectivity (~30) can be obtained without a significant surface damage in AlGaAs/GaAs heterostructures[5]. The C_xF_y and non-volatile AlF_3 products generated in the RIE chamber can prevent the further etching in the Al-contented layers[4]. In this study, we explored this concept to investigate the etching process of InAlAs and InGaAs materials by using CHF3+BCl3 gas mixture, and apply this approach for gate-recess etching in InP HEMT fabrication.

II. Characteristics of CHF3+BCl3 Etching on InAlAs and InGaAs

Cl-based gases are the typical sources used in RIE chamber to etch away the III-V coumpounds, where the volatile chlorine related products, such as $GaCl_3$, $AsCl_3$ are generated. The RIE pressure was kept at 55 mTorr with a RF power of 50W in our chamber. By using the conventional Cl-based gas (BCl3+Ar), no significant etching selectivity was found between the InAlAs and InGaAs layers, and the results are shown in Fig. 1. Both etching rates were systematically enhanced by increasing the Ar flow rates. However, by introducing the F-based gas in the RIE chamber, CHF3 in this case, the etching rate of InGaAs shown in Fig. 2 remained (~ 550Å/min) by adding the flow rate of CHF3 up to 20 sccm. This indicates no significant influence of CHF3 gas on the InGaAs etching process. However, the etching rate dropped significantly in InAlAs layers, namely from 460Å/min to 200Å/min, by increasing the CHF3 flow rate to 20 sccm. The etching selectivity between InGaAs and InAlAs shown in Fig. 2 therefore enhanced from 1.2 to 2.7. A nearly vertical side-wall etching profiles examined by the SEM was also obtained by this approach. The decrease etching rate of InAlAs corresponds to the our previous statements that the generation of C_xF_y and non-volatile AlF_3 products retards the etching rate of Al-related materials. Our previous studies in AlGaAs/GaAs heterostructures also demonstrated a selectivity enhancement (~ 30) by adding the CHF3 gas into the BCl3 plasma. The etching selectivity is much lower in InGaAs/InAlAs heterostructures, which may be related to the low vapor pressure of InF_3 products in the high In-content material systems. This non-volatile
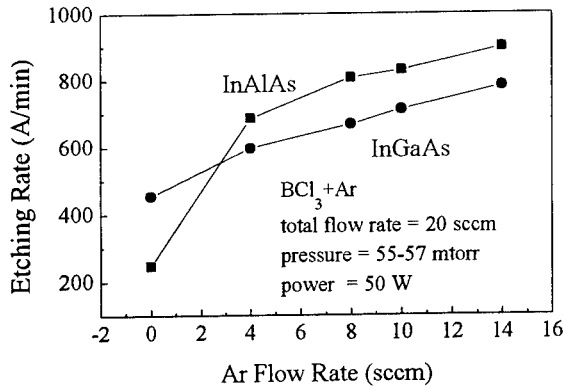
Fig. 1 The etching rates of InAlAs and InGaAs layers by BCl3+Ar.

Fig. 2 The etching rates of InAlAs and InGaAs layers by BCl3+CHF3.

product makes the selectivity lower, and it was confirmed by the etching rate evaluations of various In-content layers in the other studies.

In addition to optimize the etching selectivity by adjusting the gas flow rate ratio, we also carried out the same investigation by changing the pressure and RF power in RIE chamber. Fig. 3(a) shows the etching rates versus operation pressures of InAlAs and InGaAs layers. The flow rate ratio of BCl_3 and CHF_3 was fixed at 12:20. The etching rates systematically decreased by increasing the chamber pressures, which is resulting from a higher concentation of reactive species combined into neutral molecules. However, the selectivity unchanged (~2.5), regardless the lower etching rates. Increasing the RF power in RIE chamber, shown in Fig. 3(b), revealed the

same conclusions that the selectivity is insensitive to RF power (~2.5); however, the etching rates increased under a higher power operation.

III. Gate Recess for InP-HEMT Fabrication

After the etching optimization to achieve a high selectivity, we applied this recipe for gate-recess process to etch away the top n^+-InGaAs cap layer in InAlAs/InGaAs HEMT fabrication. This conventional InP-HEMT structure shown in Fig. 4 was grown by MBE, which demonstrated a mobility of 10200 cm^2/V-sec together with a sheet charge density of 2.8×10^{12} cm at room temperature. Devices was fabricated by the conventional optical lithgraphy technique, and we used the
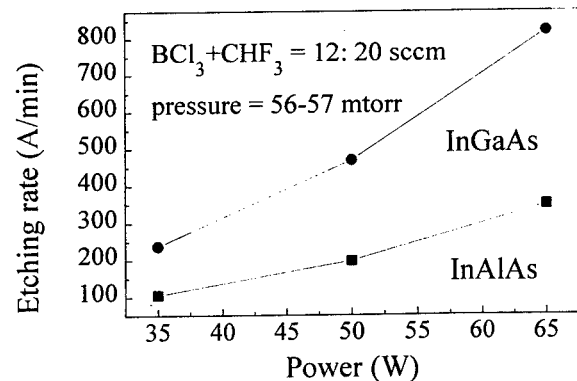
Fig. 3 The etching rates of InAlAs and InGaAs versus the RIE pressure (a), and RF power (b).

138
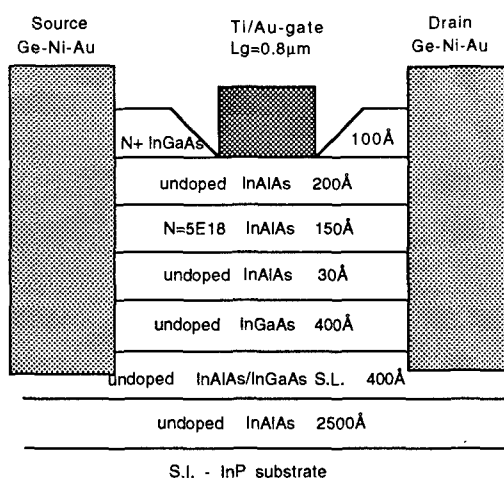
Fig. 4 Device cross-section of InP HEMTs.

deep-UV light source for the gate definition. After developing the photoresist, the wafer was loaded into the RIE chamber for gate recess etching. The flow rate ratio between BCl_3 and CHF_3 is 12:20 with a RF power of 50W.

The DC peak transconductance (g_m) was around 300 mS/mm for a gate-length of 0.8 μm, biased at $V_{ds}= 2V$. The microwave characterisitcs were carried out by measuring the S-parameters in conjunction with the Cascade direct probe. The associated f_T was 34 GHz, and the f_{max} was 75 GHz for a gate-length of 0.8 μm. Both DC and RF performance of RIE-recess InP HEMTs are
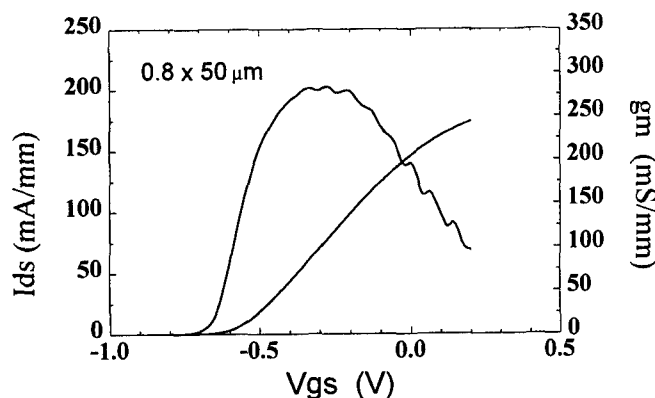
shown in Fig. 5, and these characteristics were similar to the results obtained from the wet-chemical recess HEMT in the same layer structure.

IV. Conclusions

In summary, a new gas mixture of RIE etching to achieve a selectivity between InGaAs and InAlAs layers was proposed. A selectivity of 2.7 was obtained by optimizing the CHF_3 flow rate. The performance of InAlAs/InGaAs HEMTs fabricated by this process demonstrated similar characteristics, comparing with the device fabricated by the wet-chemical process.

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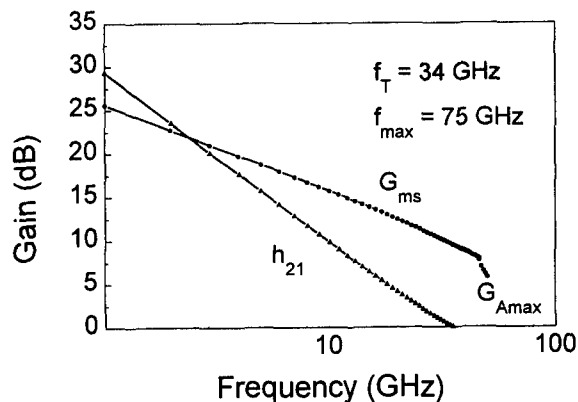
Fig. 5 DC and RF characteristics of InAlAs/InGaAs HEMTs by BCl_3+CHF_3 gate recess (Lg=0.8μm).

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The effect of high temperature annealing on 1.55μm strained GaInAs/AlGaInAs MQW lasers grown by MBE

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Abstract: The effect of high temperature annealing on the characteristics in 1.55μm strained GaInAs/AlGaInAs MQW lasers were investigated for the first time. It was experimentally found that the threshold current densities didn't change by thermal annealing even at 800°C, although the PL intensities were improved. We can say that the crystalline quality of GaInAs/AlGaInAs MQW doesn't degrade by thermal annealing even at 800°C. The MQW structure disappeared completely by Zn diffusion at 500°C. High performance narrow stripe laser can be fabricated by disordering of MQW using Zn diffusion technique.

I. Introduction

The long wavelength AlGaInAs/InP system has two interesting features; those are large conduction band offset and disordering of MQW by Zn diffusion. These features enable us to fabricate low-cost, high performance lasers used in access networks. AlGaInAs/InP strained-layer quantum well lasers has been reported to exhibit better temperature characteristics in terms of threshold current and differential quantum efficiency[1][2] than conventional GaInAsP/InP material due to large conduction band offset. However, the reported device structure in this material system was mostly ridge waveguide structure, and resulted in higher threshold current than that of GaInAsP/InP MQW laser which can use the conventional buried heterostructure. In AlGaInAs/InP MQW, the disordering of MQW by Zn diffusion can be realized without lattice-mismatching with substrate[3][4], which is different from GaInAsP/InP system[5]. Therefore the index-guide waveguide can be fabricated without etching of active layer, which may result in degradation of laser performance due to oxidation of Al-contained materials. The disordering of MQW can be applied for lateral confinement of both carrier and optical field, therefore low threshold current can be expected using this technique. However, reported threshold currents were relatively higher than those expected from threshold current densities[3][4]. One of the causes that degrades threshold current may be thermal instability during the Zn diffusion, which hasn't studied in detail so far. In this paper, we report the effect of high temperature annealing on the laser performance in 1.55μm strained GaInAs/AlGaInAs MQW lasers for the first time.

II. Growth and Annealing Method

We have grown 1.55μm GaInAs/AlGaInAs MQW lasers on n-InP substrates by molecular beam epitaxy (MBE), which consisted of p-, n-AlInAs cladding, quaternary SCH (λ_g=1.15μm), 1% compressively strained MQW active layer as shown in Fig.1. The MQW active region consisted of 1% compressively strained four 4.6nm $Ga_{0.33}In_{0.67}As$ quantum wells with 10.6nm quaternary barrier layers of the same composition as SCH. The thermal annealing was performed in an infrared tube at various conditions. To avoid decomposition of the surface, an undoped GaAs wafer was used as a proximity cap during the whole annealing process.

n-AlInAs   p-AlInAs

BARRIER
10.6nmx3

AlGaInAs   SCH 200nm
SCH 200nm
(λg=1.15μm)

WELL; 4.6nmx4
GaInAs (1%compressive)
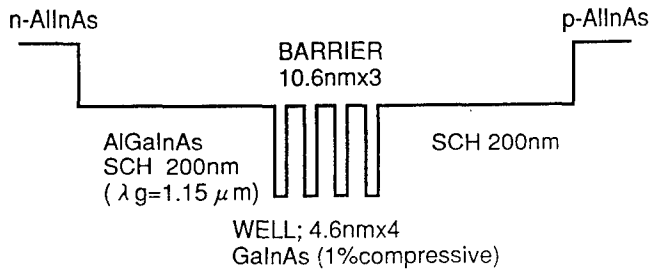
Figure 1 Schematic band diagram of the laser.

III. Evaluation of MQW after Thermal Annealing

Figure 2 shows the room-temperature photoluminescence (PL) spectra before and after annealing. The PL intensities were improved by 2~3 times after annealing without changing FWHM of the peak, although the blue shift of the peak wavelength due to the intermixing of the interfaces of MQW was found after annealing. The improvement of PL intensity could be attributed to a removal of nonradiative recombination centers from the well layers as reported for other material system[6]. Figure 3 shows the five crystal X-ray diffraction patterns before and after annealing, including the simulation analysis result. By comparing experimental and simulated results, we can observe that the periodicity of MQW and peak to

valley ratio originated from diffraction of MQW layer haven't changed except for the disappearance of many fringes observed at around the sub-peak before annealing. This is attributed to the intermixing of the atoms at the interfaces of AlGaInAs SCH layer, which is consistent with the result of PL blue shift.

After annealing, p-InP cladding and p-InGaAs
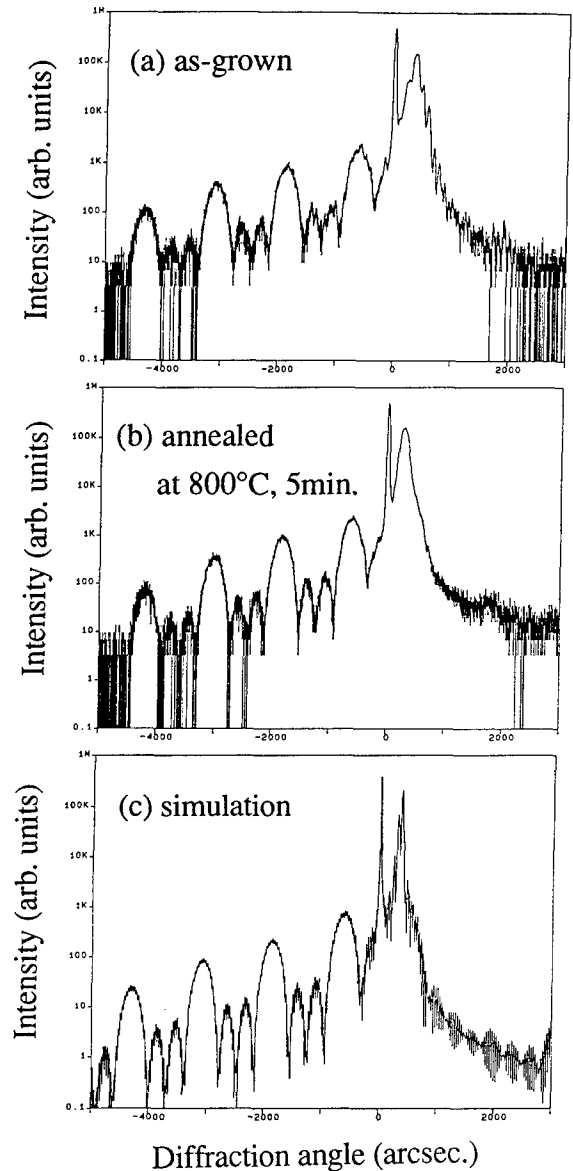
Figure 3 X-ray diffraction patterns before annealing and after annealing, together with the result of the simulation analysis.

Figure 2 Photoluminescence spectra before annealing and after annealing.
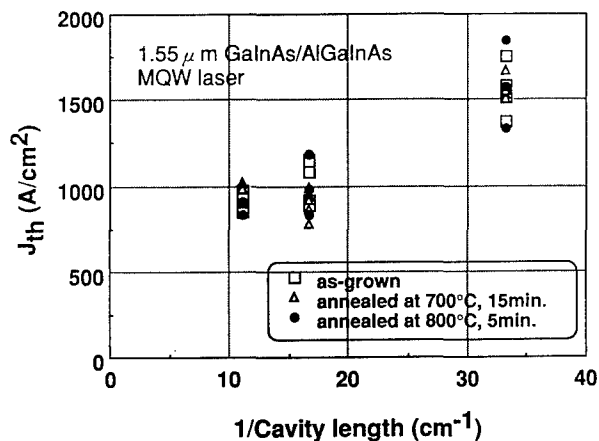
Figure 4 Inverse cavity length dependence of threshold current densities before annealing and after annealing.

Figure 5 Cross-sectional SEM image around disordered region with schematic drawing.

contact layer were regrown by MOCVD. Figure 4 shows cavity length dependence of threshold current densities. The threshold current densities didn't change by thermal annealing, although the PL intensities were improved. We can conclude that the crystalline quality of GaInAs/AlGaInAs MQW doesn't degrade by thermal annealing even at 800°C. These experimental data obtained here imply that low-threshold narrow stripe laser by Zn diffusion can be fabricated at even at high temperature .

IV. Disordering of MQW by Zn Diffusion

For further investigation, GaInAs/AlGaInAs strain compensated MQW lasers were grown on n-InP substrates by MBE. The structure is consisted of p-, n-AlInAs cladding, quaternary AlGaInAs(λ_g=1.0μm), strain compensated MQW (SC-MQW) active layer. The MQW active region consisted of 1% compressively strained twelve 5.8nm $Ga_{0.32}In_{0.68}As$ quantum wells with 0.59% tensile strained 8nm $Al_{0.35}Ga_{0.21}In_{0.44}As$ barriers. The sputtered ZnO film was used as the Zn diffusion source. The diffusion was performed in an infrared tube at 500°C for 30minutes. As the results, the peak

wavelength was blue shifted from 1616nm to 1308nm after the disordering of MQW, whereas FWHM of the PL peak was increased from 33meV to 83meV. The satellite peaks of X-ray diffraction pattern disappeared after Zn diffusion. Figure 5 shows cross-sectional scanning electron microscopy (SEM) image around disordered region. The intermediate disordering area is about 200nm. Figure 6 shows secondary ion mass spectroscopy (SIMS) profiles before and after Zn diffusion. All group III elements interdiffused completely between wells and barriers by Zn diffusion without generation of dislocations. It is noted that disordering of MQW wasn't observed in GaInAsP/InP MQW using the same condition. It is clear from these results that Zn diffusion is very promising method to fabricate buried heterostructure in AlGaInAs/InP MQW laser.

143
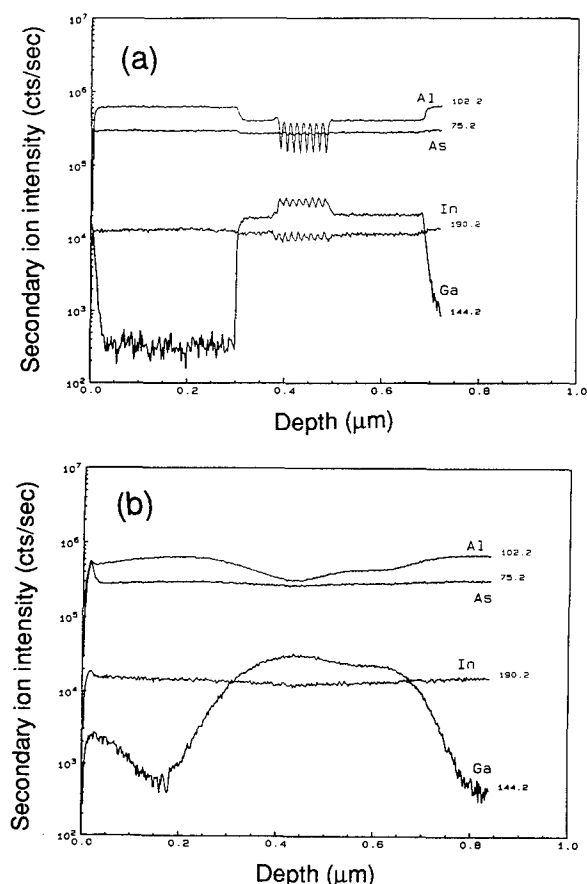
Figure 6 SIMS concentration profiles of GaInAs/AlGaInAs SC-MQW (a) before Zn diffusion, (b) after Zn diffusion.

V. Conclusions

In summary, we studied the effect of high temperature annealing on the characteristics in 1.55μm strained GaInAs/AlGaInAs MQW lasers for the first time. The threshold current densities didn't change by thermal annealing even at 800°C, although the PL intensities were improved. We can say that the crystalline quality of GaInAs/AlGaInAs MQW doesn't degrade by thermal annealing even at 800°C. The MQW structure disappeared completely by Zn diffusion at 500°C. High performance narrow stripe laser will be fabricated by disordering of MQW using Zn diffusion technique.

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FABRICATION AND CHARACTERIZATION OF A REGROWN InP/GaInAs QUANTUM POINT CONTACT

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Introduction

We demonstrate observation of quantized conductance of a regrown 90 nm wide quantum point contact (QPC) in InP/$Ga_{0.25}In_{0.75}As$ at 10K. The QPC is produced using high-resolution electron beam lithography and wet chemical etching to define the structure. PMMA was used as an etch mask during wet etching in $HCl:CH_3COOH:H_2O_2$ solution at 15°C. Proximity effect due to mask exposure by backward scattered electrons decreases masking property of PMMA. To overcome a problem of insufficient masking ability of the resist, a post-development hard baking above the glass transition temperature (T_g) of PMMA was performed. Using this simple approach, we were able to produce the QPCs as small as 50 nm in width.

I. Background

Quantized ballistic transport in a one-dimensional channel has attracted strong interest after its discovery in 1988 [1,2]. Due to a small size of the channel, of the order of the Fermi wavelength of an electron in a two-dimensional electron gas (2DEG), a quantization of conductance in units of $2e^2/h$ can be observed. Most of the approaches for definition of the channel or quantum point contact (QPC) utilize a concept of split Schottky gate on top of GaAs/AlGaAs modulation-doped heterostructure [1,3,4]. The electrostatic definition of a QPC is fairly easy to implement, however, it can only be used with materials which form a good Schottky contact. Besides, electrostatically defined QPCs are not very suitable for device application.

Another approach includes fabrication of a QPC by a geometrical definition of the channel by high-resolution lithography and etching. A regrowth of etched-out QPC would reduce scattering of electrons at the 2DEG interface, allowing formation of a high-quality one-dimensional channel. Such approach allows fabrication of a QPC in InP/GaInAs 2DEG material which has an advantage of having lower electron effective mass compared to the GaAs/AlGaAs system.

In this work we report demonstration of quantized conductance in an InP/$Ga_{0.25}In_{0.75}As$ QPC defined by electron beam lithography and wet etching with subsequent regrowth by undoped or Fe-doped InP.

II. Experimental

As a starting material we used an InP/$Ga_{0.25}In_{0.75}As$ modulation doped QW structure. It was grown by metal organic vapor phase epitaxy (MOVPE) at 600°C and pressure of 50 mbar. The mobility of 2DEG was 520 000 cm^2/Vs, which is the highest mobility achieved in a GaInAs alloy up to date [5]. The sheet electron concentration, measured by Hall effect at liquid helium temperature, was $5*10^{11}$ cm^{-2}. To make wet etching easier, the distance between the surface and the 2DEG was about 50 nm.

The initial structure was cleaved into several pieces about 6x3 mm^2 which were patterned by optical lithography and wet etching to produce Hall-bars. Thermally deposited Au/Ge/Au ohmic contacts alloyed at 440°C for 2 min were used for current and voltage probes. The 80 nm thick PMMA (950K) layer was spun onto the mesas and a QPC structure was defined by electron beam lithography. For this purpose a commercial scanning electron microscope operating at 35 kV and 100 pA was used. The QPC structure was defined as a narrow channel, about 100 nm long, oriented along [1-10] or [110] direction.

For wet etching we used 1:2:2 $HCl:CH_3COOH:H_2O_2$ solution at 15°C, which gives etching rate of InP and GaInAs of about 9-13 nm/s. It is suitable for etching through the 2DEG for a depth of about 100 nm. After a standard cleaning procedure, the QPC structures were regrown by either low pressure MOVPE with undoped InP or by atmospheric pressure hydride

vapor phase epitaxy (HVPE) at 685°C with semiinsulating Fe-doped InP [6].

Both as-etched and regrown QPCs were characterized by transport measurements, using a top gating technique to control the electron concentration in the QPC. To make a top gate, a 1 μm thick positive photoresist (Shipley S-1813) was used as an insulator on top of the structure. After defining the isolation region by optical lithography, the resist was hard baked at 185°C for 2 hours. Such cross-linked resist it stable at liquid helium temperature and has gate leakage current of less than 1 pA. A thick Ti/Au contact was deposited onto the resist and patterned by a lift-off.

Atomic force microscope (AFM) and scanning electron microscope (SEM) were utilized for characterization of the QPC at different steps of its fabrication.

III. Results and Discussion

Etching InP/GaInAs in $HCl:CH_3COOH:H_2O_2$ solution showed fairly good etched surface quality, but etching rate reproducibility was not very good, Fig. 1.
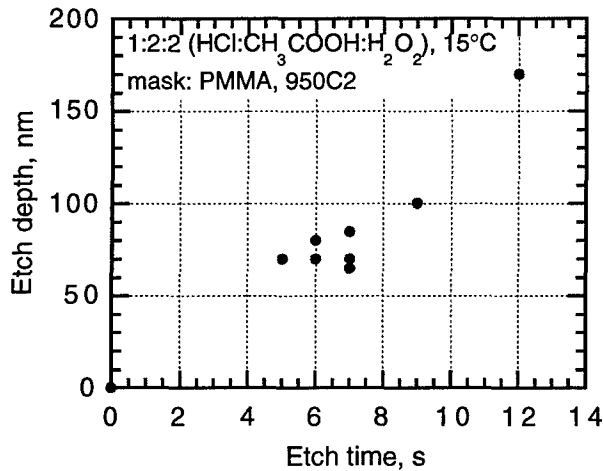
Fig.1 InP/GaInAs etch depth versus time. Etching was performed in $HCl:CH_3COOH:H_2O_2$ solution at 15°C.

Under the same etching conditions, a variation of the etching rate of InP/GaInAs was typically about 20-30%. However, it was possible to produce a 90 nm wide QPC in InP/GaInAs 2DEG, Fig. 2. The channel, connecting upper left and lower right parts of the structure, is a QPC.

Due to etch rate irreproducibility, the etch time had to be increased to 7-10 s in order to etch through the 2DEG. We found that the stability of 950K PMMA with 80 nm in thickness was sufficient up to 15 s of etching, which corresponds to roughly 180 nm depth in InP. This result was based on measurement of masking properties of unexposed PMMA, but in case of QPC the masking properties of PMMA was found to be much less. It results from unwanted proximity exposure by backward scattered electrons from adjacent exposed regions, thus limiting etching time to 10 s. A Monte-Carlo simulation of exposure

under the conditions we used, showed that the proximity effect is determined by the backward scattered electrons collected from a surrounding area of about 2 μm in radius. The observed degradation of the PMMA masking properties is known to be due to increased porosity. The pores of order of 1 nm in size are formed due to release of volatile products of the main chain scission and appearance of excess free volume in the polymer film [7].
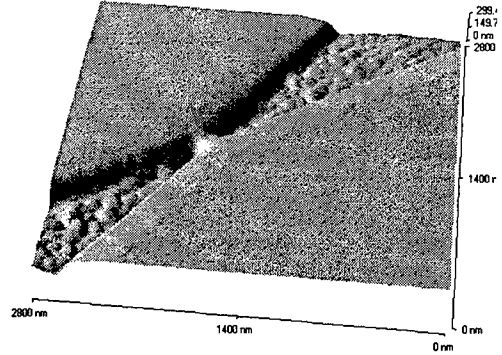
Fig. 2 AFM image of as-etched 90 nm wide QPC in InP/GaInAs 2DEG. The channel is oriented along [1-10] direction. The etching depth is approximately 80 nm, as determined by the AFM. Some unevenness of the etched surface is due to resist residues left after development.

AFM scans of as-etched QPCs revealed a problem related to porosity of PMMA: erosion of top InP cap layer in a QPC channel. Typically it was in the range of a few nanometers, but considering a strong dependence of both 2DEG concentration and mobility on cap layer thickness, it was crucial for performance of the QPC. Table 1 illustrates dependence of QPC cap layer thinning on total etching time for a 90 nm wide channel. One can easily see that at etching time exceeding 10 s the QPC is virtually destroyed by the erosion. For channels smaller than 90 nm, cap layer thinning is so big, that it is impossible to define the QPC by wet etching without any damage.

Table 1. AFM measurement of QPC cap layer thinning as a function of etching time. Nominal width of a QPC channel is 90 nm, orientation is [1-10].

Etch time, s	Etch depth, nm	QPC cap layer thinning, nm
6	70	10
9	100	15
12	170	80

Since masking properties of PMMA are determined by a proximity dose, a test pattern was made with different doses to test PMMA masking properties in $HCl:CH_3COOH:H_2O_2$ solution versus exposure dose. The

test pattern consisted of several squares 20 by 20 μm in size, exposed with doses ranging from 70 to 375 μC/cm². The sample was then etched for 7 s and the etching depth at the squares was measured by an AFM. The results of the measurement are plotted in Fig. 3.

Assuming a contribution from backward scattered electrons about 0.8-1 of a forward scattered dose [8], one can estimate dose in the QPC mask as of 40-50% of forward-scattered one. According to Fig. 3 such dose corresponds to a threshold of PMMA masking ability for 7 s etch.
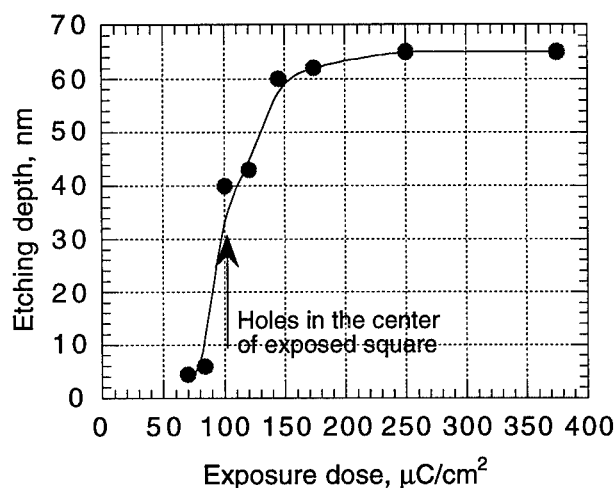
Fig. 3 Masking properties of 80 nm thick PMMA (950K) after etching InP/GaInAs for 7 s in 1:2:2 HCl:CH₃COOH:H₂O₂ at 15°C versus exposure dose. Exposure dose of ≈100 μC/cm² results in formation of pores in PMMA and can be regarded as a threshold of masking ability of the resist.

These results confirm that insufficient masking property of PMMA is a main limiting factor in decreasing size of the QPC. In order to improve masking ability of the resist in wet etchant, we perform a post-exposure bake of PMMA. Baking of PMMA above glass transition temperature (T_g=105°C) results in an increase of its masking ability during wet etching, but also widens the mask. To determine the optimal baking conditions, we performed a series of baking at different temperatures of a test QPC-like structure and measured a widening of the resist mask after baking procedure. It was found that the best baking conditions are the following: temperature between 110 and 130°C, duration 30 min at hot plate. Under these conditions the flow of PMMA was minimal and QPC channel doesn't change its shape.

Investigation of InP/GaInAs etching in 1:2:2 HCl:CH₃COOH:H₂O₂ at 15°C showed that orientation of the QPC channel along [1-10] direction results in etching profile which forms ≈130° angle between channel sidewalls and the surface. It limits achievable channel width to about 100 nm. On the contrary, [110] orientation allows formation of almost vertical sidewalls.

SEM images in Fig. 4 a, b show a [110] QPC channel etched without (a) and with (b) post-exposure

baking at 130°C. Etching time was 7 s and PMMA was removed in hot acetone afterwards.

The results shown above are fairly reproducible. A change of exposure dose by a few percent leads to a small change of QPC width, for example, a 50 nm wide channel can be produced by increasing the dose by 8% compared to normal dose.

The [1-10] 90 nm and [110] 60 nm wide as-etched QPC structures were regrown by either MOVPE or HVPE techniques. Both regrowth techniques showed good surface morphology, as observed by AFM and SEM.
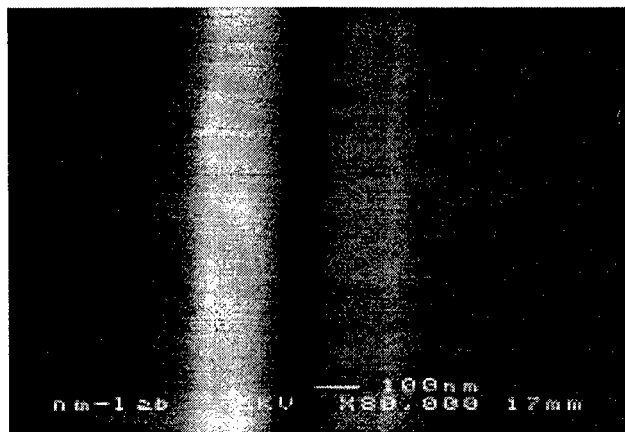
a)
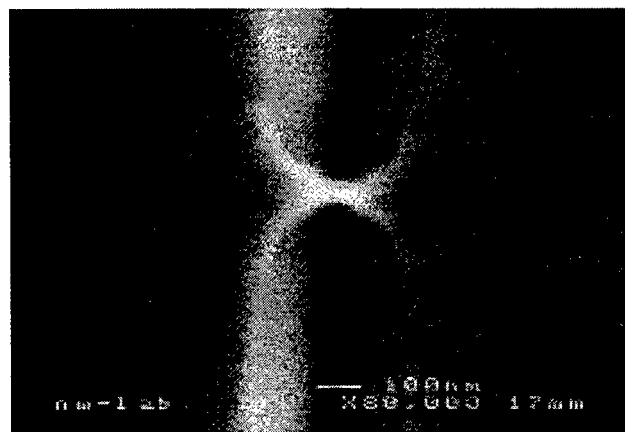
b)

Fig. 4 Influence of post-exposure PMMA baking on formation of QPC in InP/GaInAs. The QPC channel is oriented in [110] direction.
a) No post-exposure baking of the resist. Stability of PMMA was not sufficient to form a QPC.
b) PMMA was baked at 130°C for 30 min. A 60 nm wide QPC channel is formed.

The 90 nm wide QPCs were characterized by the transport measurements before and after regrowth. Typical resistance of the as-etched wire was 100 kΩ, which suggests that the electric width is smaller than 100 nm. It can be readily explained by depletion at the edge of the QPC channel. After regrowth with InP the QPCs showed an overall lower resistance than before, indicating a more

147

defect-free InP/GaInAs interface. Fig. 5 shows the conductance at 10 K as a function of gate voltage for the 90 nm wide InP/GaInAs QPC after regrowth with undoped InP in MOVPE. Two plateaus with integer values and one fractional value of $2e^2/h$ are seen. More detailed description of the transport measurements is reported elsewhere [9].
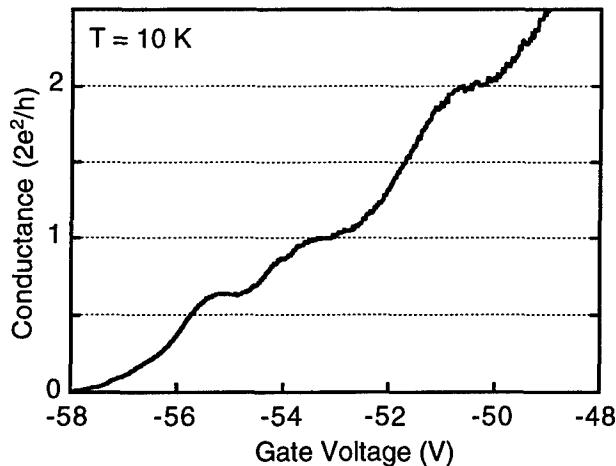
Fig. 5 Quantized conductance of MOVPE regrown 90 nm wide QPC at 10K.

IV. Conclusions

We demonstrated fabrication of an epitaxially regrown QPC in InP/GaInAs 2DEG structure with size as small as 50 nm. In order to improve masking property of PMMA in wet etching solution, a post-exposure bake at 130°C was performed. It has been shown that baking enhances resist masking ability due to elimination of pores, induced by proximity exposure. Transport measurements of a regrown 90 nm wide QPC at 10K demonstrated a quantized conductance in steps of $2e^2/h$. Regrowth of etched QPC resulted in substantial improvement of 2DEG interface properties.

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MEASUREMENT OF HIGH CURRENT DENSITY PHENOMENA AND VELOCITY OVERSHOOT IN InP/GaInAs HBTs

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Abstract

Electron transport in the collector of InP/GaInAs heterojunction bipolar transistors (HBTs) was experimentally studied in the high current density regime. The average velocity of electrons in the collector was obtained as a function of the collector current density and base collector voltage, and found to be larger than the saturation velocity. Phenomena caused by the base push out (Kirk) effect were observed. It is demonstrated that below the onset of the Kirk effect the injected electron space charge in the collector improved the high frequency performance of the HBT. A new result presented is that the average electron velocity in the collector exhibited a maximum when plotted versus the base collector voltage.

I. Introduction

The optimal high frequency performance of HBTs is achieved at very high current density. It is therefore of utmost importance to understand the high current density phenomena, i.e., the velocity overshoot and the base push out (Kirk) effect (1). The electron average velocity in the collector depletion region of GaAs HBTs in the high current density regime was previously estimated from the value of F_T obtained from s-parameter measurements (2-3). Following these experiments, Monte Carlo analysis demonstrated the effect of electron space charge on electron velocity in the collector (4). The variation of the base collector capacitance and the collector transit time with the collector current density in InP/GaInAs HBTs was reported in (5). An additional Monte Carlo simulation of electron transport in the the GaInAs collector clearly demonstrated the velocity overshot effect (6).

In this publication we report on a detailed experimental study of electron transport in InP/GaInAs HBTs in the high current density regime. The electron average velocity in the collector depletion layer was calculated by measuring the base collector capacitance and the electron transit time in the collector as a function of collector current and base collector reverse bias. An interesting result presented is that the average electron velocity in the collector exhibited a maximum when plotted versus V_{BC}. The results are discussed with respect to the physical processes affecting the electron velocity in the collector.

II. Experimental

The epitaxial layers were grown on a semi insulating InP by a compact metal organic molecular beam epitaxy system (7). Conventional wet etching and a self aligned Pt/Ti/Pt/Au

one step metalization process were employed to fabricate the device. Ti/Au pads were evaporated after polyimide passivation. The layer structure of the HBT is outlined in Fig.1. Emitter and base mesa dimensions were $3.3 \times 11 \mu m^2$ and $8.5 \times 22.5 \mu m^2$, respectively. Small signal s-parameters of the HBT were measured on wafer up to 40GHz as a function of collector current density and base collector voltage. F_t and F_{max} of 65GHz and 35GHz, respectively, were measured at $I_C = 20 mA$, $V_{CE} = 2V$.

100nm GaInAs n - 1×10^{19}	Emitter cap layer
200nm InP n - $1 \times 10^{17} - 3 \times 10^{18}$	Emitter
57nm GaInAs p - 3×10^{19}	Base
400nm GaInAs undopped	Collector
200nm InP undopped	
400nm GaInAs n - 1×10^{19}	Sub-collector
InP sub (SI)	

Figure 1 - Layer structure of HBT.

III. Base collector capacitance and emitter to collector transit time

The base collector capacitance was directly extracted from the measured s-parameters using the method outlined in (8). The results are plotted in Fig. 2 as a function of collector current density at different values of base collector reverse bias. The variation of the base collector capacitance with the collector current below and above the onset of the Kirk effect is well interpreted by the change in the depletion layer width caused by the injected electron space charge (3).
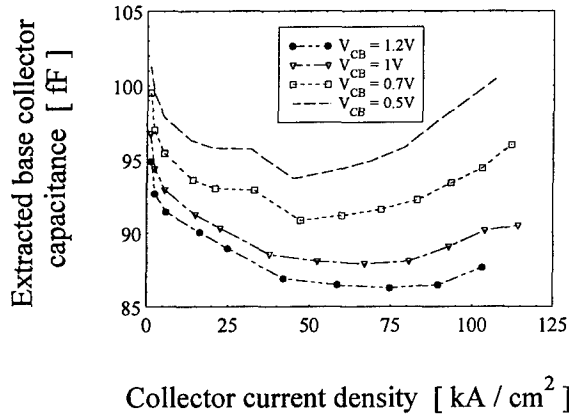
Figure 2 - Base collector capacitance extracted from high frequency s-parameter measurements, as a function of collector current density for different base collector bias values.

Since the lateral dimensions of the base mesa are much larger than the collector layer thickness, the extrinsic base collector capacitance, $C_{bc,ext}$, does not vary with collector current. The collector depletion layer width was therefore calculated using the expression

(1) $\quad W_{dep}(J_C, V_{BC}) = \varepsilon A_E / \left[C_{bc}(J_C, V_{BC}) - C_{bc,ext}(V_{BC}) \right]$.

where ε is the dielectric constant of the collector, and A_E the area of the emitter mesa. The effect of the electron space charge on the depletion layer width below and above the onset of the Kirk effect is clearly shown in Fig. 3.

The presentation of the method employed to extract the emitter to collector transit time is beyond the scope of this publication, and will therefore be described elsewhere. Here, we merely present the obtained results. The extracted emitter to collector transit time ($\tau_B + \tau_C$) is plotted in Fig. 4 as a function of collector current density for different values of base collector reverse bias. The transit time exhibited a

minimum at $J_C \approx 30 kA / cm^2$ for base collector voltages in the range of 0.5V - 0.7V. The onset of the base push out effect varied between $J_C \approx 50 kA / cm^2$ for low reverse bias and $J_C \approx 75 kA / cm^2$ for higher values of reverse bias. At current densities lower than the Kirk threshold current density, the injected space charge broadened the velocity overshoot region, and hence the decrease in the measured transit time (4).

Collector current density [kA / cm^2]
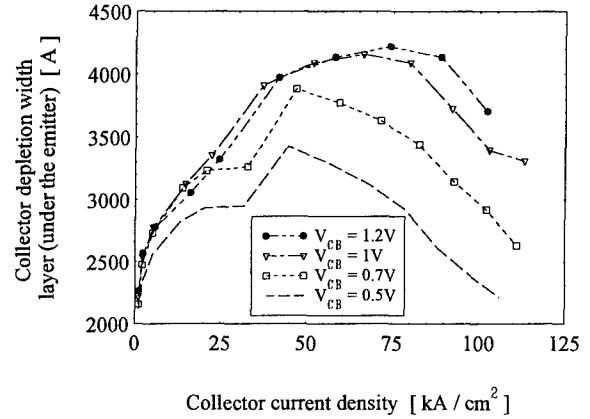
Figure 3 - Collector depletion region width calculated using the value of the *intrinsic* base collector capacitance versus collector current density for different base collector bias values.

Collector current density [kA / cm^2]
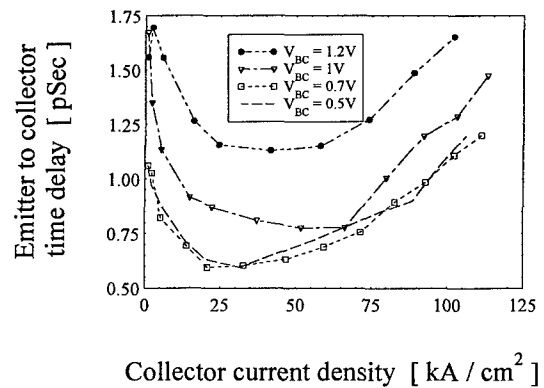
Figure 4 - Sum of base and collector transit time extracted from s -parameter measurements versus collector current density for different base collector bias values.

IV. Electron velocity in the collector

The velocity of the electrons in the collector was calculated by the expression

$$(2) \quad v_{av} = \frac{W_{dep}}{2\tau_C}.$$
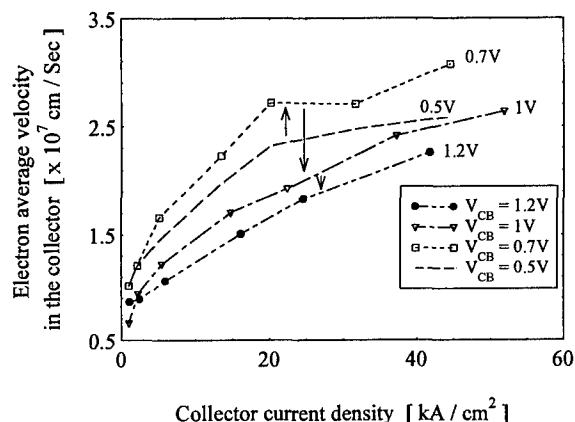
Figure 5 - Calculated electron average velocity in the collector as a function of collector current density for different base collector bias values. The arrows indicate the bias direction.

We have limited the calculation of the electron velocity to a current density lower than the Kirk effect onset current density. At these current densities the base transit time does not vary with collector current. The base transit time was estimated as 0.25psec, using an approximate expression given in (9) with electron minority carrier mobility value obtained in (10). The collector transit time was calculated by subtracting the base transit time from the data presented in Fig. 4.

The obtained average electron velocity is plotted in Fig.5 as a function of collector current density (before the onset of the Kirk effect). The average electron velocity is found to increase with the collector current density since the injected space charge broadens the velocity overshoot region (3). Note that due to the velocity overshoot near the base collector interface the average electron velocity is much higher than the saturation velocity in GaInAs.

The average electron velocity is found to vary with V_{BC} in a non-monotonous manner. The maximum average velocity is obtained at $V_{BC} \approx 0.7V$, and a decrease in the average velocity is found for higher values of V_{BC}. This behavior was not predicted in previous theoretical modeling (5), but is clearly seen here. We attribute the observed maximum to the opposite dependence of the overshoot velocity and the saturation velocity on the magnitude of the electric field in the collector.

V. conclusions

The electron average velocity in the collector depletion region is calculated from high frequency s-parameter measurements in an InP/GaInAs HBT as a function of the collector current density and the base collector reverse bias. The effect of the injected space charge on the velocity overshoot in the collector and the base push out (Kirk) effect, are experimentally observed. It is shown that the injected electron space charge in the collector improves the high frequency performance of the HBT, below the onset of the Kirk effect. An optimum in the average velocity with respect to base collector reverse bias is observed and attributed to the opposite dependence of the overshoot velocity and the saturation velocity on the magnitude of the electric field in the collector.

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THE EFFECT OF PASSIVATION ON THE HOT ELECTRON DEGRADATION OF LATTICE-MATCHED InAlAs/InGaAs/InP HEMTs

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I. Background

As InP-HEMT technology is maturing, increasing attention is being devoted to reliability issues[1-7]. Researchers identified surface degradation as one of the critical points for device stability, and various passivation techniques were investigated and shown to contribute to device robustness[5-7]. However, the published reliability experiments used temperature as the accelerating factor, thus overlooking another possible source of device instabilities, i.e., hot electrons (HEs).

HEs and impact ionization play a role even at relatively low drain bias in InP-HEMTs, due to the very small channel bandgap and high electron mobility[8,9]. Room temperature stress at high V_{DS} was recently shown to degrade both the dc and rf performance of SiN-passivated InP-HEMTs[10]. Since the degradation observed was attributed to negative charge capture at the interface between semiconductor and passivation or in the SiN itself, the aim of this work is to extend such experiments by presenting for the first time a comparison between non-passivated and passivated samples from the point of view of HE reliability.

II. Experiments

The devices we tested are δ-doped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ (i.e., lattice-matched) HEMTs designed and fabricated at IMEC; they feature a gate length of 0.25-0.3 μm (unless otherwise noted) and width of 100 μm.

For devices with the same layer structure and geometry, whether they are passivated or not, the nature and magnitude of the degradation brought about by HE stressing turns out to depend to some degree on differences in processing. For instance, since channel electron heating and impact ionization are directly governed by the high electric field of the gate-drain region, the gate recess shape can be expected (and is known) to play a very important role; therefore, different recess etching techniques generally yield different hot electron robustness and gate-drain breakdown behavior. It is thus most important, if a fair comparison is to be made between passivated and non-passivated (bare) devices, that all the remaining processing steps be exactly the same. The easiest and most reliable way of ensuring this is to carry out all the processing steps preceeding the deposition of SiN, cut the wafer in two pieces, passivate one of them and leave the other one bare. This is the procedure that we followed, obtaining what will be hereafter referred to as lot P-1 (passivated) and B-1 (bare) devices.

In addition to that, in order to give a more complete picture of hot electron degradation in InP HEMTs and its relationship with device passivation, we show results obtained on two more lots, indicated as P-2 (passivated) and B-3 (bare). These lots underwent different process steps, hence a direct comparison of the respective hot electron robustness from the viewpoint of passivation is not possible; nevertheless, the results will give some more insight of this matter.

The passivation layer we used is made of 200 nm thick PECVD SiN, deposited in 25 min at 250° C under growth conditions optimized for minimal stress. The index of refraction and dielectric constant are 1.86 and 7, respectively.

We performed all the stress experiments at room temperature.

III. Results and Discussion

A. Lots P-1 and B-1

These two lots come from a wafer that was processed using a selective (succinic) etch for the gate recess. This results in a wide lateral etch of the InGaAs cap layer. Passivated (P-1) and bare (B-1) devices have two-terminal gate-drain breakdown voltage (defined as the value of V_{DG} that yields 1 mA/mm reverse gate current with source floating) of about 4 and 5 V, respectively. The breakdown voltage is higher in the bare devices probably due to lower surface potential[11,12], which tends to reduce the lateral electric field[13,14].

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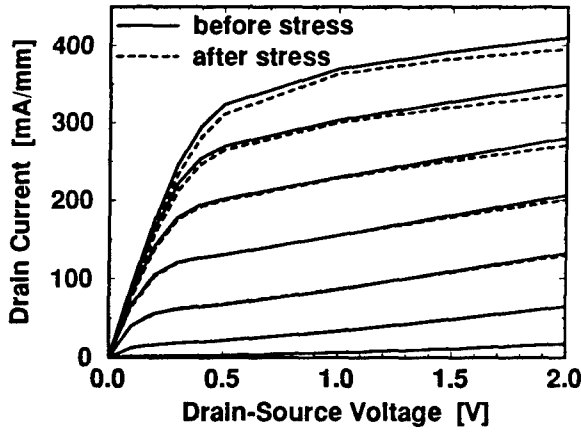
Figure 1: Output characteristics of a P-1 device before and after HE stress up to $V_{DG} = 4.3$ V. V_{GS} ranges from -0.2 V to 0.4 V with 0.1 V increments.
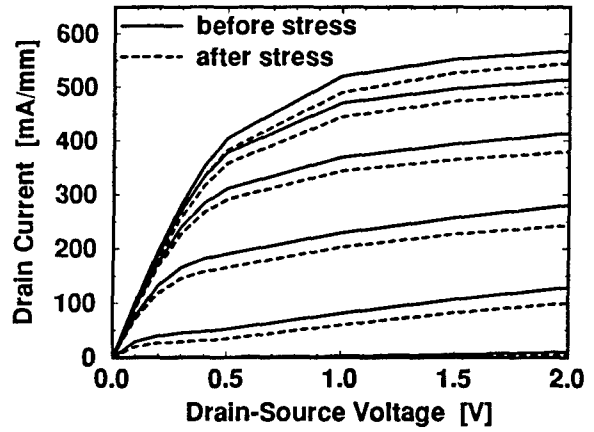
Figure 2: Output characteristics of a B-1 device before and after HE stress up to $V_{DG} = 4.3$ V. V_{GS} ranges from -0.6 V to 0.4 V with 0.2 V increments.

As previously observed[11], the deposition of the passivation layer has a twofold effect on the device dc characteristics: it increases the threshold voltage and the peak g_m. In particular, when it comes to designing the stress experiment, the different values of V_T make it necessary to bias the devices at different V_{GS} if the comparison has to be meaningful. Our choice was to set the stress gate bias at the value corresponding to the peak g_m in saturation, because it allows for the different V_T's, and represents the most interesting case from the practical viewpoint, since it is the bias condition where the devices will likely operate. The peak g_m occurs at $V_{GS} = 0.2$ V and -0.3 V for P-1 and B-1 HEMTs, respectively. As for the V_{DS} value to be chosen for stress acceleration, since the peak longitudinal electric field in the channel is known to roughly scale with $V_{DS} - V_{GS}$, we stressed the two lots at V_{DS} values such that the resulting V_{DG} was the same in both cases. The duration of the stress steps ranged from 5 to 15 min, since we observed that the device degradation practically saturates after the first few minutes of stress. The stress procedure featured an initial step at $V_{DG} = 2.8$ V (corresponding to $V_{DS} = 3$ V and 2.5 V for P-1 and B-1, respectively), then V_{DG} was gradually increased at every step until the HEMT failed catastrophically. The device characteristics were measured after each step of the sequence.

With this procedure we have stressed 3 HEMTs per lot. The P-1 devices died at V_{DG} ranging from 3.8 to 4.55 V (V_{DS} ranging from 4 to 4.75 V), while the HEMTs of the B-1 lot failed at V_{DG} between 4.3 and 5.8 V (V_{DS} ranging from 4 to 5.5 V). Although the number of devices tested so far is too small to give significant statistical knowledge, this tendency of the passivated HEMTs to die at lower voltages than the bare ones may be related to the above mentioned difference between the respective gate-drain breakdown voltages.

Before catastrophic failure, the HEMTs undergo a
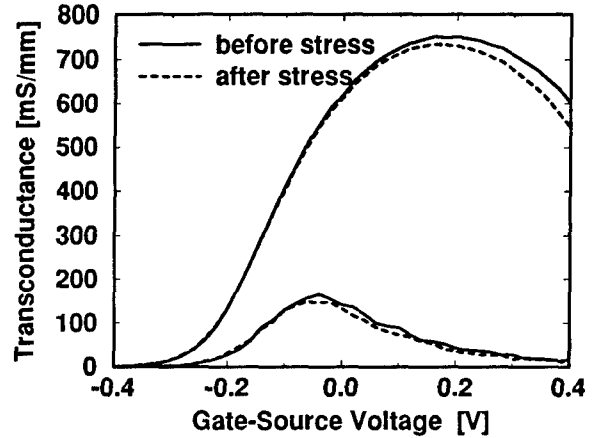
Figure 3: g_m vs. V_{GS} curve of a P-1 device, measured at $V_{DS} = 50$ mV and 1 V, before and after the HE stress of Fig. 1.

gradual degradation that is increased by each subsequent stress step. All the devices of the same lot show the same degradation mode. Fig. 1 and 2 illustrate the effect of the HE stress on the output characteristics of passivated and bare HEMTs, respectively. The two devices were stressed up to the same $V_{DG} = 4.3$ V. Larger shifts of the characteristics were observed for higher stress voltages. In both cases the drain current decreases after the stress, although in a different fashion. The different degradation mode of the two lots is better illustrated by Fig. 3 and 4, where we plot the linear and saturated transconductance as a function of V_{GS} before and after the stress.

The effect of the stress on the passivated devices (Fig. 1 and 3) is a decrease of I_D and g_m at high gate bias, in agreement with the results obtained on a different lot[10]. This effect can be attributed to electron trap creation and/or negative charge capture at the device surface, i.e.,

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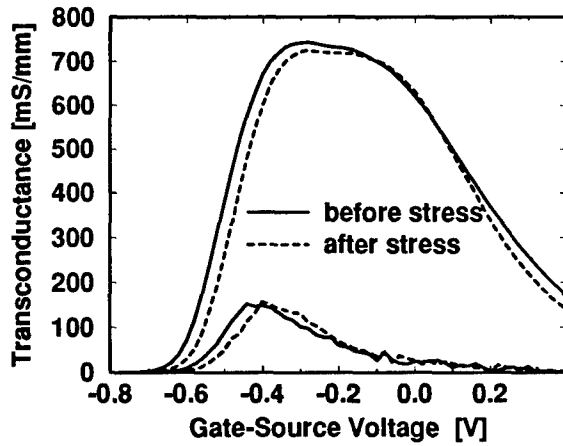
Figure 4: g_m vs. V_{GS} curve of a B-1 device, measured at $V_{DS} = 50$ mV and 1 V, before and after the HE stress of Fig. 2.
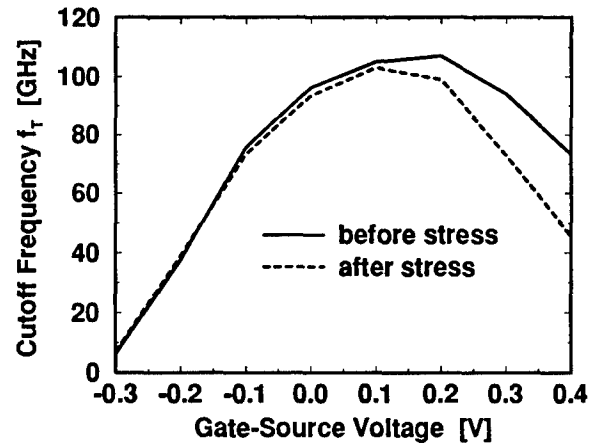
Figure 5: f_T vs. V_{GS} curve of a P-2 device, measured at $V_{DS} = 1$ V, before and after a HE stress up to $V_{DG} = 4.5$ V.

at the interface between the semiconductor and the SiN or in the SiN itself, which produces or enhances cap depletion.

On the other hand, when we stress bare devices (Fig. 2 and 4) the current decreases due to both a g_m reduction at high V_{GS} and to a positive shift of the threshold voltage ($\Delta V_T \simeq 30$ mV for the stress of Fig. 2). While the g_m compression can be due, as in the P-1 case, to electron storage at the device surface, the V_T shift may be linked with the (much larger) threshold voltage increase that takes place during the passivation deposition. This is probably a thermally driven sinking of Pt from the gate into the Schottky layer, yielding a reduction of the gate-channel distance[15]. In bare devices, which have not undergone the high temperature passivation process, this gate contact annealing may be initiated by device self-heating, that can easily lead to temperatures in excess of 150-200 °C under the stress bias conditions we adopt. On the other hand, we can rule out that the ΔV_T is due to some change of the gate barrier height, because we observed practically no difference in the gate forward and reverse I-V characteristics measured before and after the stress.

For both passivated and bare devices, the observed degradation is permanent.

B. Lots P-2 and B-3

The devices of these two lots underwent a nonselective (phosphoric) gate recess. This means that the lateral cap etch is very limited (about as large as the cap thickness), i.e., the cap covers nearly all of the device area lying between gate and source and gate and drain. The dc effect of stressing a HEMT of lot P-2 (passivated) up to $V_{DG} = 4.5$ V for 30 min is qualitatively the same as in the case of P-1 HEMTs, i.e., I_D and g_m are permanently degraded at high V_{GS}. However, the degradation is larger than
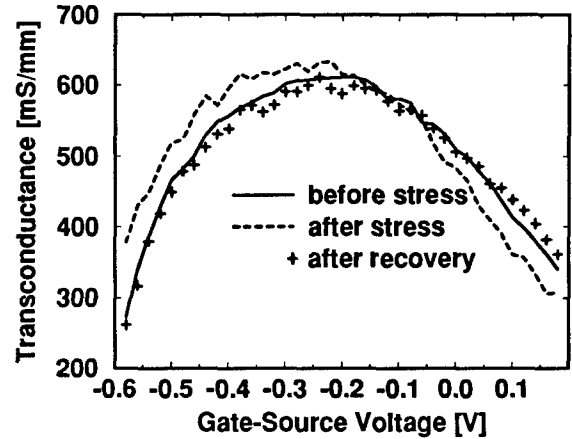
Figure 6: g_m vs. V_{GS} curve of a B-3 device, measured at $V_{DS} = 1$ V, before and after a HE stress of 30 min at $V_{DG} = 2.25$ V, and after recovery.

in the P-1 case. This is consistent with the explanation proposed above, and with the different cap situation. If the reduction of I_D and g_m is due to cap and surface depletion, this effect is expected to be weaker in P-1 devices, where the cap layer has been laterally etched away much more. The g_m compression directly affects the device microwave performance, as Fig. 5 demonstrates for f_T (f_{max} undergoes similar degradation).

Finally, 0.15 μm bare HEMTs from lot B-3 were stressed for 30 min at voltages in the range $V_{DS} = 1.75$-3 V; in all cases we observed a negative ΔV_T ranging from -5 to -38 mV. A representative example is given in Fig. 6. We measured no g_m compression after the stress. Negative V_T shifts have been observed before in GaAs-HEMTs[16] in connection with a storage of positive charge (that can be supplied by holes generated by impact ionization) in traps located under the gate. It is

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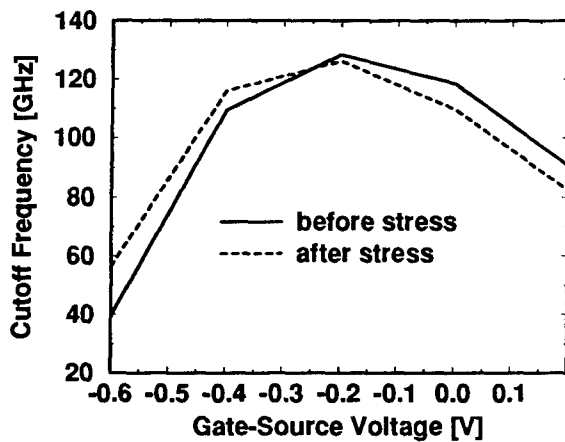
Figure 7: f_T vs. V_{GS} curve of a B-3 device, measured at $V_{DS} = 1$ V, before and after the HE stress of Fig. 6.

important to stress that ΔV_T will not degrade the device performance when, as generally happens with HEMTs, the device is current-driven, because it will be automatically compensated by the bias circuit[17]. The data of Fig. 6 also indicate that ΔV_T is recovered after a few days of storage at room temperature. This complete recovery supports the proposed degradation mechanism. Fig. 7 shows that the V_T shift is visible also at microwave frequencies. The absence of g_m reduction probably comes from the fact that in bare devices the cap is already depleted before the stress by the lower surface potential.

IV. Conclusions

Our results indicate that under hot electron conditions both SiN-passivated and bare InP HEMTs have a tendency to degrade from the point of view of dc and rf characteristics.

Passivated devices show a permanent decrease of drain current and transconductance at high gate bias. The degradation is attributed to negative charge accumulation at the surface leading to cap depletion, and tends to be weaker in selectively etched gate devices, where the cap is laterally etched away much more. This dc effect is mirrored by a reduction of the current gain cutoff frequency in the same bias range.

Bare HEMTs display a variety of degradation modes, depending on the particular device geometrical and process features. The gate recess process, as can be expected, is particularly critical from this standpoint. Some devices (selectively etched) experience, as a consequence of the stress, a permanent threshold voltage increase (probably due to Pt sinking, activated by device self-heating, from the gate into the InAlAs) and a transconductance compression similar to that of the passivated samples. Others (non-selectively etched) show a temporary (i.e., recoverable) reduction of the threshold voltage

(originated by hole capture under the gate) resulting in an increase of the drain current for fixed gate and drain bias.

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Ring Oscillator Using InAlAs/InGaAs/InP Enhancement/Depletion-Mode High Electron Mobility Transistor Direct-Coupled FET Logic Inverters

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Introduction

The monolithic integration of enhancement- and depletion-mode (E- and D-mode) high electron mobility transistors (HEMTs) lattice-matched to InP is of interest in the area of circuits for low power, high speed communications. When compared to circuits implemented in depletion-mode (D-mode) only technology, circuits implemented in E/D-mode technology enjoy a number of advantages. D-mode only circuits require level-shifting between successive cascaded stages, where E/D-mode circuits do not. The extra level-shifting circuitry increases power consumption and chip area, as well as circuit design and layout complexity (1). In addition, E/D-mode circuits can operate on a single power supply, whereas such operation of D-mode only circuits can be achieved only through increased circuit complexity. There has been some modest success in the development of an integrated E/D technology on lattice-matched InP (2). Recently, a process for the fabrication of high speed E-mode HEMTs on lattice-matched InP has been reported (5), as well as for the monolithic integration of E- and D-mode devices on a common substrate (6).

In this paper, the performance of this process is demonstrated by the fabrication and characterization of E/D-mode 0.5 μm gate-length direct-coupled FET logic (DCFL) inverters, and an 11-stage ring oscillator with a 3-stage output buffer, based on these inverters. Testing of discrete 0.5 μm devices gave threshold voltages of 195 mV with a standard deviation of 9 mV for the E-HEMTs, and -365 mV with a standard deviation of 19 mV for the D-HEMTs. RF testing yields unity current gain cutoff frequencies (f_t) of 70 GHz and 67 GHz for the E-HEMTs and D-HEMTs respectively. The inverters were tested for DC performance and the voltage transfer curve shows noise margins of 145 mV at supply voltages as low as 0.6 V. The ring oscillator was tested using a spectrum analyzer and shows propagation delays as low as 20.66 ps/stage, power dissipation as low as 120 μW/stage, and power delay products as low as 2.65 fJ/stage. The fabrication process, inverters, and ring oscillator are described in detail.

I. Devices

The devices were fabricated on a heterostructure grown by molecular beam epitaxy (MBE) on a semi-insulating InP substrate. The buffer consists of 200 nm of InAlAs followed by a 20 nm undoped InGaAs channel. A 3.5 nm undoped InAlAs spacer layer rests on top of the channel followed by a Si δ-doping plane, a 12 nm undoped InAlAs Schottky barrier layer, and a pseudomorphic 1.5 nm AlAs etch stop layer. Another 10 nm-thick InAlAs layer is grown on the etch-stop layer followed by a 1.5 nm AlAs layer and an n^+ InGaAs cap. Using Hall measurements, a 2 DEG concentration of 0.7×10^{12} cm^{-2} with an electron mobility of 8500 cm^2/V-s was measured at room temperature. The etch-stop

layers, combined with the high selectivity of a citric acid/hydrogen peroxide solution for gate recess etching, ensures a uniform and repeatable threshold voltage across the wafer.

Mesa and ohmic levels were patterned simultaneously for both E- and D-mode devices. Following the ohmic contact formation, electron beam lithography was first used to pattern mushroom-shaped gates for the E-mode devices. A selective etching process was used to etch to the bottom etch-stop layer followed by the deposition of Pt/Ti/Pt/Au gate metallization. After the E-HEMT gate deposition, the devices were annealed at 350 °C for one minute to increase the threshold voltage (2-5). The D-mode gates were then fabricated by etching the InGaAs

Fig. 1 E/D layer structure. The D-mode gate metallization is Ti/Au while the E-mode gate metallization is Pt/Ti/Pt/Au.

cap to the top etch stop followed by a Ti/Au gate metallization. Using this technique, gate lengths of 0.5 μm were fabricated for both E- and D-mode HEMTs. A schematic of the device heterostructure illustrating E- and D-HEMTs is shown in Fig. 1. The source to drain spacing was 2 μm.

Discrete devices, on wafer with the oscillators, were tested at both DC and RF. Histograms of the threshold voltages for the E-mode and D-mode HEMTs are shown in Fig. 2 and Fig. 3, respectively. The measurements show threshold voltages of 195

mV with a standard deviation of 9 mV for the E-HEMTs, and -365 mV with a standard deviation of 19 mV for the D-HEMTs. The RF testing indicated unity current gain cutoff frequencies (f_t) of 70 GHz and 67 GHz for the E-HEMTs and D-HEMTs respectively.

II. Circuits
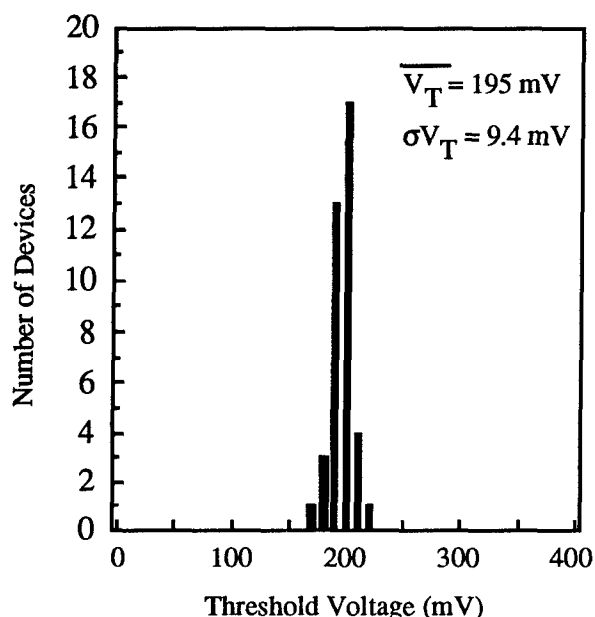
Fig. 2 Histogram of E-mode HEMT threshold voltages.
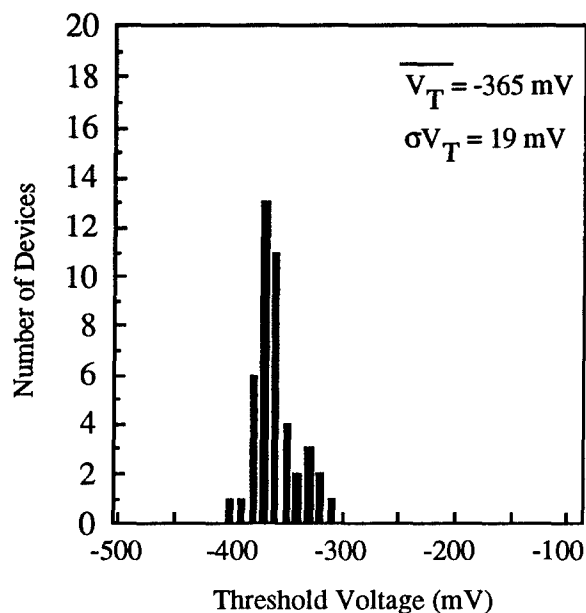
Fig. 3 Histogram of D-mode HEMT threshold voltages.

The inverter load consists of a 5 μm-wide gate-to-source shorted depletion-mode FET. The driver is a 10 μm-wide enhancement-mode device. Gate lengths on all devices are 0.5 μm. The voltage
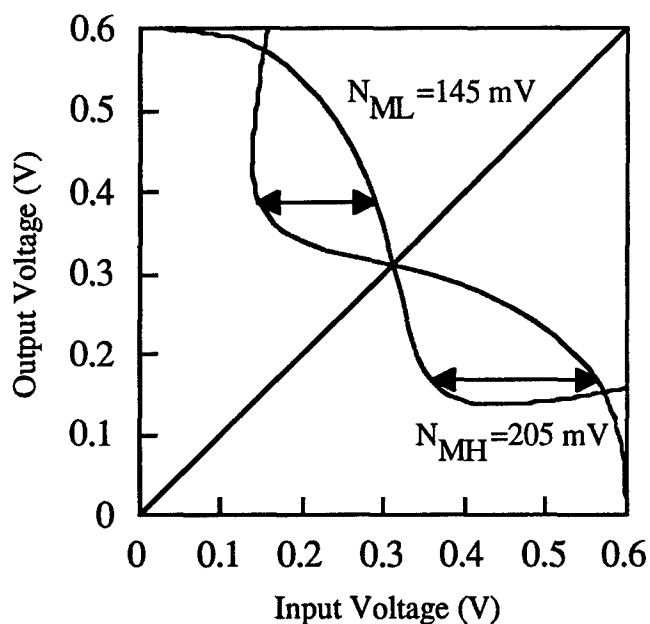
Fig. 4 Voltage transfer curve of E/D inverter at Vdd = 0.6 V.
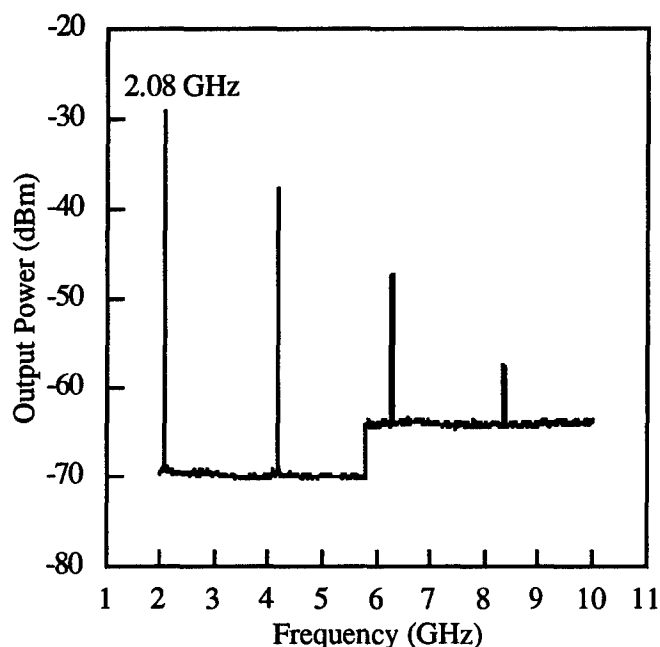
Fig. 5 Spectrum of oscillator output at Vdd = 0.6 V.

transfer curve for the inverter with a supply voltage of 0.6 V is shown in Fig. 4. At this supply voltage, the static logic swing is 0.45 V, and the noise margins, defined by the maximum width method, are 145 mV for N_{ML} and 205 mV for N_{MH}, as indicated on Fig. 4.

The oscillator consists of 11 of the E/D inverters in a ring. The output is provided by a 3-stage buffer to prevent loading of the ring oscillator during testing. The buffer is made up of a 1.5 μm-load/3 μm-driver inverter, followed by a 7.5 μm-load/15 μm-driver inverter, ending in a 50 μm-load/100 μm-driver inverter. The total device count for the
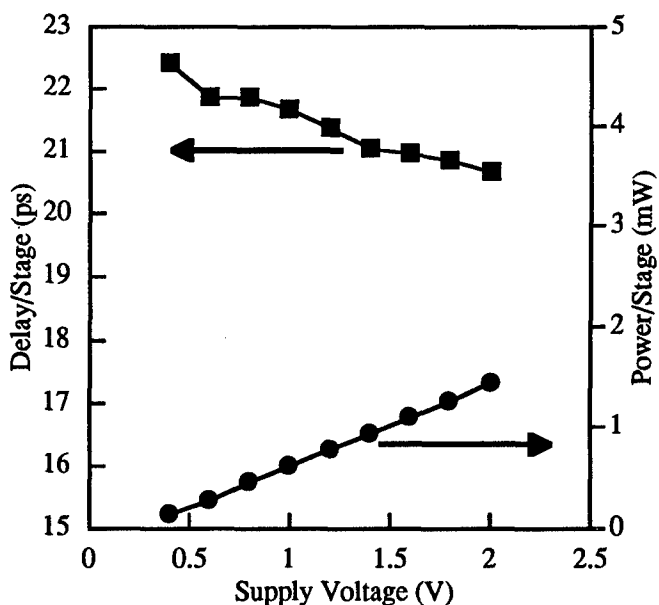
Fig. 6 Delay per stage and power per stage versus Vdd.

ring oscillator with buffer is 28 devices. The oscillator and buffer have separate voltage supplies, so that the oscillator power consumption could be measured directly. The spectrum of the ring oscillator's output for a supply voltage of 0.6 V is shown in Fig. 5. The fundamental frequency of the oscillator output is at 2.08 GHz, indicating a propagation delay time of 21.85 ps. Delay per stage and power consumption per stage of the oscillator are shown in Fig. 5 as a function of supply voltage. The minimum propagation delay of 20.66 ps was observed for a supply voltage of 2 V. Power-delay product per stage of the oscillator as a function of supply voltage is
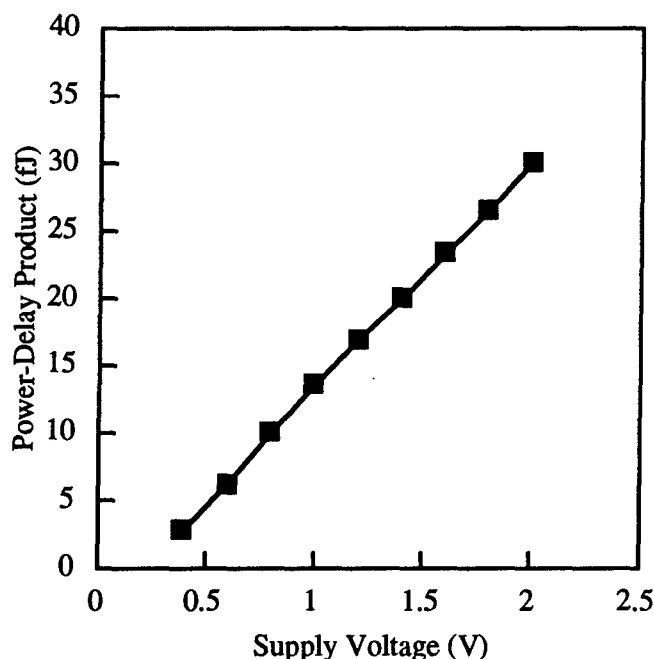
Fig. 7 Power-delay product versus Vdd for one stage of the ring oscillator.

shown in Fig. 7. The minimum power per stage is 120 μW and the minimum power-delay product is 2.65 fJ. Both of these occur at a supply voltage of 0.4 V.

III. Summary

The monolithic integration of E/D-mode 0.5 μm gate-length HEMTs on lattice-matched InP has been demonstrated by the fabrication of a ring oscillator. The circuit consists of 28 devices. Control over threshold voltage for both the E-HEMTs and D-HEMTs in this process is excellent. E-HEMT threshold voltage is 195 mV with a 9 mV standard deviation and D-HEMT threshold voltage is -365 mV with a 19 mV standard deviation. The inverters that make up the oscillator exhibit a 450 mV static output voltage swing and noise margins of 145 mV at a supply voltage of 0.6 V. The ring oscillator showed a minimum propagation delay of 20.66 ps, a minimum power consumption/stage of 120 μW, and a minimum power-delay product of 2.65 fJ/stage. The

demonstration of this oscillator shows the integrated E/D-HEMT process to be suitable for more complex, larger-scale integrated circuits.

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DETRIMENTAL EFFECTS LIMITING THE PERFORMANCES OF InP HEMT-BASED OEICs.

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Introduction

An investigation has been carried out on InAlAs/InGaAs HEMTs dedicated to monolithic optoelectronic integrated circuits (OEICs) for receiver as well as transmitter applications. The monolithic integration on InP semi-insulating substrates can be penalized by several parasitic effects related to trapping/detrapping mechanisms originated in the substrate and/or buffer layers. These parasitics have been studied in three MBE-grown HEMT structures, one of them previously demonstrated as efficient in the reduction of the gate current induced by an impact ionisation mechanism developping in the InGaAs channel layer.

I. Background

The InAlAs/InGaAs HEMT is a key electron device used in OEICs operating in the 1.3 and 1.5 μm optical wavelength ranges for digital systems and microwave/optical interface applications. Similarly to GaAs FET-based ICs, the performances of InP HEMT-based OEICs are degraded by detrimental (parasitic) effects. They are induced by the HEMT itself or by interactions between active adjacent devices (HEMT-to-HEMT and/or HEMT-to-optical device). We are carrying out an investigation of these effects versus different key fabrication process steps on the basis of a rapid feedback to technological improvements. HEMT test structures together with a major parasitic, the side-gating effect, have been already presented (1). In this communication, we report results about several other important detrimental effects :
- the gate current which degrades the optical receiver performances (2),
- the drain current transients which penalize the direct or external laser modulation (3).

II. Studied devices

The material has been grown by molecular beam epitaxy (MBE) and the studied structures are illustrated in Fig. 1. 0.3 and 0.5 μm $\times$ 100 μm TiPdAu recessed gate are deposited with T and Π topologies. AuGeNi ohmic contacts are used with TiPdAu overlayers. A ultra violet chemical vapor deposited (UVCVD) Si$_3$N$_4$ layer insures the surface passivation. Typical electrical characteristics are given in Table 1.

Structure N°1	Structure N°2	Structure N°3
	GaInAs Cap	*GaInAs* Cap
GaInAs Cap	*Al$_x$In$_{1-x}$P* Barrier	*AlInAs* Barrier
AlInAs Barrier	x=0.25 Eg=1.90 eV	*AlInAs* Donor layer
Planar doping	*AlInAs* Barrier	*Al$_x$In$_{1-x}$As* Barrier
8 10^{12} cm^{-2}	*AlInAs* Donor layer	x=0.75 Eg=2.22 eV
AlInAs Spacer	*AlInAs* Spacer	*AlInAs* Spacer
GaInAs Channel	*GaInAs* Channel	*GaInAs* Channel
AlInAs Buffer	*AlInAs* Buffer	*AlInAs* Buffer
InP Substrate	*InP* Substrate	*InP* Substrate

Fig. 1 : Studied MBE-grown epilayer structures.

The difference in *Idss* values as a function of the gate topology is somewhat difficult to understand, the gate width being along the same direction for all the devices. The drastic reduction in *Idss* in structure N° 3 can be explained by the electron screening effect of the high bandgap InAlAs layer.

Table 1 : Typical electrical characteristics.

gate		Structure N°1				Structure N°2				Structure N°3			
gate	Wg	100 μm		100 μm		100 μm		100 μm		100 μm		100 μm	
	Lg	0,5 μm		0,3 μm		0,5 μm		0,3 μm		0,5 μm		0,3 μm	
	Topology	T	Π	T	Π	T	Π	T	Π	T	Π	T	Π
Idss	(mA)	33	25	48	41	53	45	73	57	19	17	21	11
Vp	(V)	-1	-1	-0,6	-0,4	-1	-1	-1,8	-1,4	-0,3	-0,3	-0,4	-0,6
Gm_{max}	(mS/mm)	630	550	650	370	500	450	480	465	290	290	295	200

III. Gate current improvement

Holes generated by impact ionization in the GaInAs channel of conventional structures (Fig. 1 - Structure N°1) can increase the gate current, Igs, by several tenths of μA at the HEMT operating point (Fig. 2). In order to reduce the hole flow to the gate, high bandgap barrier layers have been inserted between the channel layer and schottky gate (Fig. 1 - structure N°2 and 3). The increase in the valence band discontinuity (ΔEv $\cong$ 0.5 eV towards the lattice-matched AlInAs in structure N°3) reduces the hole flow and consequently Igs by two orders of magnitude in structure N°3 (Fig. 2). But an additional leakage current appears in structure N°2.

conditions and exploitation of results can be found (4). The devices did not exhibit the gate lag phenomenon confirming the surface access regions are properly passivated. The gate lag corresponds to drain current transients in response to gate switching in the saturated region of the I-V characteristics. The drain lag phenomenon affects the HEMTs with high bandgap barrier layers (Fig 3 and 4). The drain-lag ratio increases when driving the gate bias towards pinch-off conditions (Fig. 4). Values as high as 40 % are measured on structure N° 3. One can note that high laser drive voltage shifts have been measured at 622 and 2500 Mbits/s for similar ratio in GaAs devices (3). These results clearly indicate the channel-to-buffer interface and buffer layer are involved, especially in the strained structure N°3.

Fig. 2 : Gate current characteristics ; (Igs, Vgs).
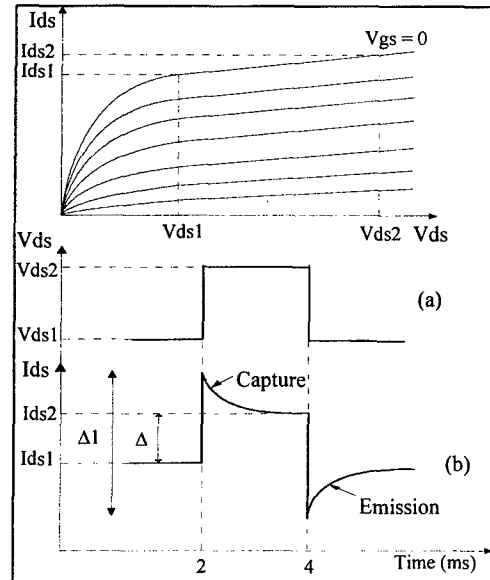
Fig. 3 : Drain lag effect. It corresponds to drain current overshoot and transient related todrain-to-source pulses in the saturated I-V characteristic of the device. $\Delta I/\Delta$ is the drain lag ratio.

IV. Drain current transients

Drain current responses have been investigated under gate and drain switching conditions and the related current transients are known as gate and drain lags. Detailed measurements
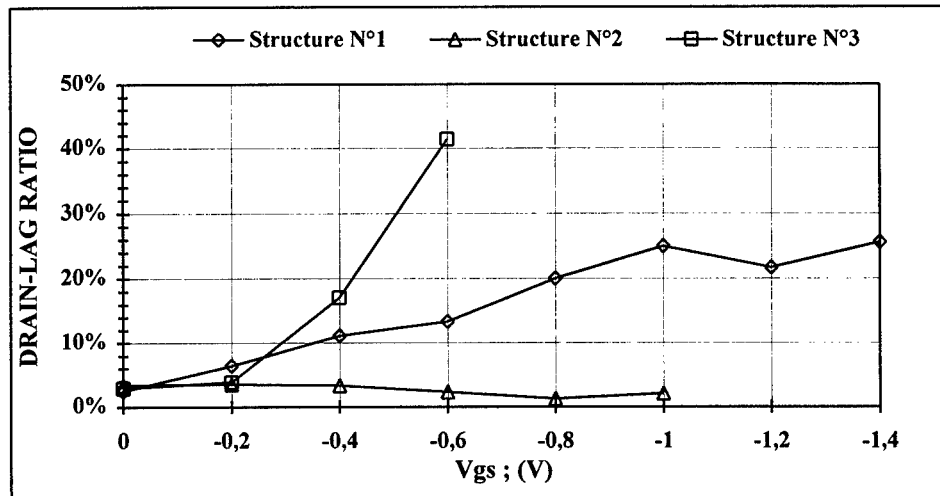
Fig. 4 : Drain lag ratio versus gate bias.

V. Traps investigation

Then, trapping mechanisms in the AlInAs buffer layers were expected to be responsible for the drain-lag effect. The signatures reported in Fig. 5 brought a confirmation : they all have been previously identified in MBE-grown AlInAs layers (5). They have been measured using the isothermal relaxation experiment (6). It digitized the drain current transients obtained under gate and drain voltage switching in the saturated I-V characteristics. Then, it discriminates the different exponential contributions to the current transients as a function of temperature. As a consequence it is expected that the measured signatures are really those governing the current transients.
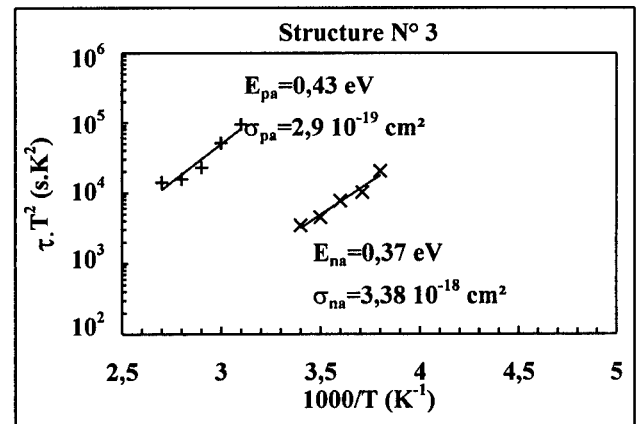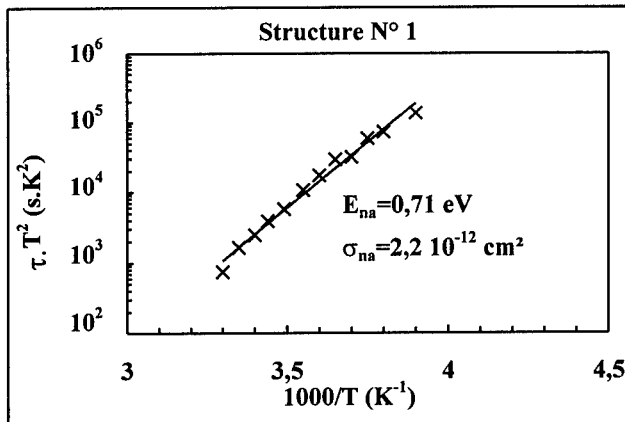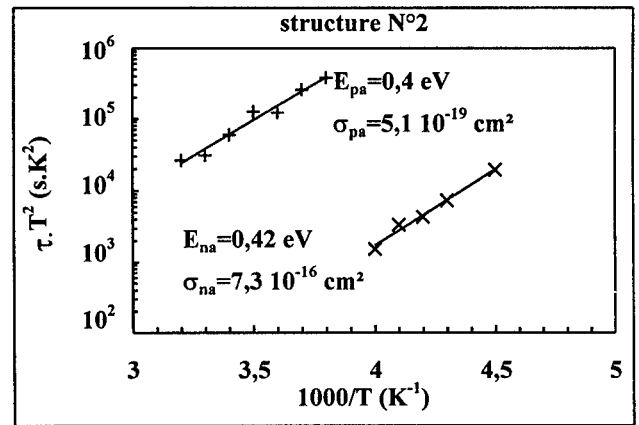
Fig. 5 : Trap signatures obtained near pinch-off conditions by means of isothermal relaxation experiment.

VI. Conclusion

An investigation of a major parasitic effect has been carried out on several MBE-grown HEMT structures regarding OEIC applications. The drain lag effect, detrimental to the laser operation, has been evidenced and characterized in terms of traps signatures related to the InAlAs buffer layers. It can be noted that the drain lag ratio is the highest for the structure the most efficient against the hole flow contributing to the gate current.

Regarding the above-mentioned results, technological improvements have been focused on the buffer layer growth conditions and design.

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INP BASED FET STRUCTURE GROWN AND PROCESSED AT EXTREMELY LOW TEMPERATURES OF 280°C

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Abstract

A technological concept for a InP-HFET structure fully grown and processed at a low temperature of 280°C is presented. It is based on low temperature grown (LTG) InP used as a auto-doped channel material and LTG-AlInAs as buffer and Schotty layer. Design and optimization, especially the transition from the P containing to the As containing compounds of the Schottky gate heterostructure contact layer is discussed. The proof of concept is demonstrated with a first FET device.

I. Introduction

In a number of optoelectronic technologies a post processing growth of electronic devices is highly desired. III/V materials grown at low temperatures have been intensively investigated in view of those applications. Due to the fact that group V overpressure adsorption and desorbtion of the group V element are not in equilibrium, as in the case of conventional growth, in consequence, a high amount of group V elementes is found in this materials, incorporated on group III-sites and interstitials. In LTG-GaAs, grown below 350°C, the As_{Ga} forms a deep level 0.6 - 0.4eV (1) below the conduction band edge, which renders the material highly resistive. Thus, it is not possible to fabricate a GaAs based active channel material at temperatures below 350°C.

Also, InP grown at such low temperature correspondingly forms a P_{In} anti-site defect, however with the first excited state located 120meV above the conduction band edge (2). In concequence this material is n-type auto-doped and is therefore a possible candidate for a low temperature grown InP channel material. The carrier density in the channel has been shown to be directly related to the growth temperature with a higher concentration at lower growth temperature (3). The channel sheet charge will

thus be determined by growth temperature and layer thickness.

However, to modulate the channel charge in a FET structure suitable interfaces, gate diode barrier layers and buffer layers have to be developed, which also need to be grown in the same temperature range. Here the focus will be on the growth of this complete heterostructure with special attention to the Schottky contact layer system and its interface to the channel, which has to prevent parallel conduction and enable capacitive channel charge modulation.

II. Layer Growth and Device Processing

The heterostructures used in this approach, are based on InP grown by GSMBE, using PH_3 as P-source. The available n-type auto-doping carrier concentration in LTG-InP in a temperature range from 350°C down to 250°C ranges from $1*10^{16} cm^{-3}$ to $5*10^{18} cm^{-3}$ with a corresponding mobility between $3200 cm^2/Vs$ and $1000 cm^2/Vs$, as descript in detail in (3).

The gate barrier layer has been systematically developed by the following procedure: Starting with AlInAs grown at 500°C, which is used as gate contact layer for conventional HFET structures, the growth temperature is reduced to the growth temperature range of the LTG-InP

channel layer centering around 280°C. Second, at this growth temperature the transition from the excess P region (LTG-InP) to the excess As region (LTG-AlInAs) has been optimised by changing the V/III ratio and incerting a spacer layers.

A. LTG barrier material on conventionally InP

The first set of samples was designed to investigate the gate barrier characteristics versus growth temperature. 25nm LTG-AlInAs barrier layers were grown on a 200nm thick AlInAs buffer layer and a Si-doped InP-channel layer grown at standart temperature (500°C), nominally having the identical channel carrier concentration as used later for the LTG-InP channel layer, thus eliminating any influence of the LTG-InP channel material. In Fig. 2 the IV-characteristics of such AlInAs-gate contact layers are shown, which were grown at temperatures of 420°C, 350°C and 280°C.

B. LTG AlInAs barrier material on LTG InP

With the second set of samples the influence of excess P at the interface to the AlInAs barrier layers due to the low channel and buffer layer growth temperatures is investigated with a thick LTG-InP layer acting as backside diode contact.
In the first part of this investigation LTG-AlInAs was directly deposited onto the LTG-InP channel using a conventional switching of the chemical components at the interface, however with an additional gradual change of the P-flux. The reason for this procedure was to prevent interfacial P segregation. Furthermore, it is not well understood how a LTG quaternary compound containing Al,In,As and P will behave electrically and whether this will be highly resistive as needed.
In detail, 30nm LTG-InP was grown using the optimised bulk materials growth conditions and a V/III ratio of 3.75, followed by a 25nm LTG-InP channel part with reduced V/III ratios of (a) 0%, (b) 20% and (c) 30%.
In the second part of experiments the insertion of diffusion barriers has been investigated. Different barrier configurations have been realized as in particular: (a.) no diffusion barrier, (b) a 5nm LTG-GaInP barrier layer and (c) a 5 nm LTG-AlInP barrier. The Ga or Al content respectively was approx. 50%. At this composition the layers are highly strained and under compressive stress. This may help to suppress P outdiffusion from the LTG-InP channel layer. The thickness of the gate diode layer system was kept constant to 25nm.

C. LTG-HFET structure

To demonstrate the feasibility of the technological approach the LTG gate diode was deposited onto a 25nm thick LTG-InP channel grown at 280°C. The temperature and thickness was choosen to result in a free carrier concentration of $8*10^{17}cm^{-3}$ and a sheet charge density of $2*10^{12}cm^{-2}$ which is a typical sheet charge concentration for a HFET structure. In detail the LTG-HFET structure consisted of a 200nm LTG-AlInAs buffer layer, a 25nm autodoped LTG-InP active channel layer and a shared 5nm/20nm LTG-GaInP/AlInAs Gate contact layer as shown in Fig. 1. However, due to the gradual change of the P flux towards the interfaces the effective sheet charge density may be significantly reduced.

D. FET Processing

Not to exceed the growth temperature the thermal processing budget was also limited to 280°C. The fabrication scheme is based on conventional InP technologies, using optical lithography and metallisation and patterning by evaporation and lift-off. The devices have been isolated by wet chemical mesa etching. Contact windows have been etched into the barrier layer structure before depositing source and drain contacts of Ge/Ni/Au, which were alloyed at 280°C. The Schottky gate contact material was Ti/Pt/Au. The gate length was 1.5µm, the gate width was 50µm.

III. Electrical Characteristics

A. LTG barrier material on conventionally InP

1µm long Schottky gate characteristics as described in section (IIA), are shown in Fig. 2.
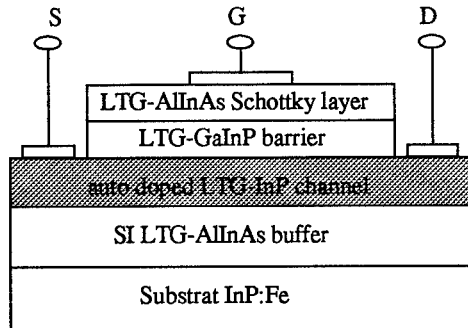
Fig. 1: LTG-HFET structure grown and processed at 280°C.
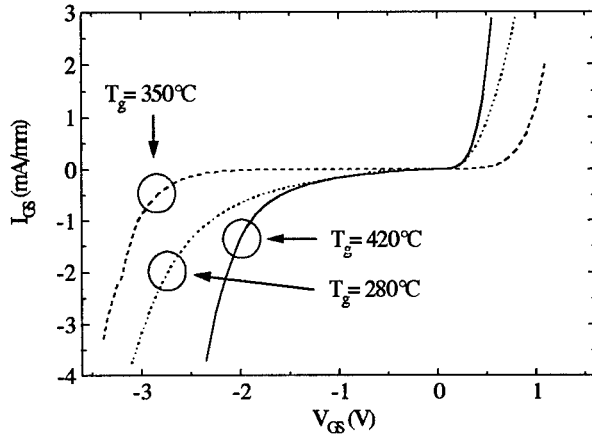
Fig. 2: Gate diode characteristics of LTG-AlInAs Gate contact layer grown at 420°C, 350°C and 280°C.

The results indicate a strong decrease of the gate leakage current with decreasing growth temperatures down to 350°C. Lowering the growth temperature further results in a small increase as seen from the sample grown at 280°C. Breakdown voltages (defined by the technical definition of 1mA/mm) vary from -2 to -3 volts. Thus this diodes will severly limit the pinch-off voltage of the FET device. The highest forward turn-on voltage is observed for the diode grown at 350°C, where also the breakdown voltage is the highest. This behaviour may be related to P accumulation or even segregation at the barrier layer interface effectively creating a highly doped Schottky barrier contact. To identify this effect in detail temperature measurements may be neccessary. Here, as a consequence the P V/III ratio at the interface was changed as described in section (IIB).

B. LTG barrier material on LTG InP

The impact of the reduction of excess P on the gate diode characteristics grown at 280°C is shown in Fig. 3 with a PH$_3$ reductions of (a) 0%, (b) 20% and (c) 30%. Indeed, the best diode characteristic is seen for case (c). At a higher reduction of PH$_3$ the morphology begins to degrade. Thus, the highest reduction of PH$_3$ results in diode characteristics with the lowest leackage current, the highest breakdown voltage (-3.2V) and the largest forward turn-on voltage.
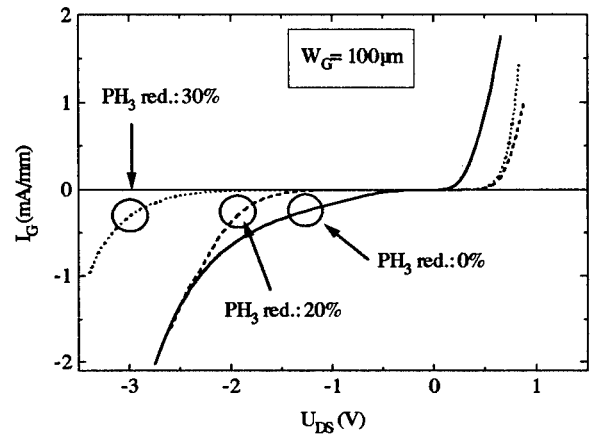
Fig. 3: Gate diode characteristics of LTG-AlInAs Gate contact layer grown on LTG-InP channel layer grown with diffrent V/III ratios.

The second concept includs GaInP or AlInP highly strained diffusion barriers at the LTG-InP channel gate contact layer interface as desribed in section (IIB). The Schottky characteristic are shown in Fig. 4.
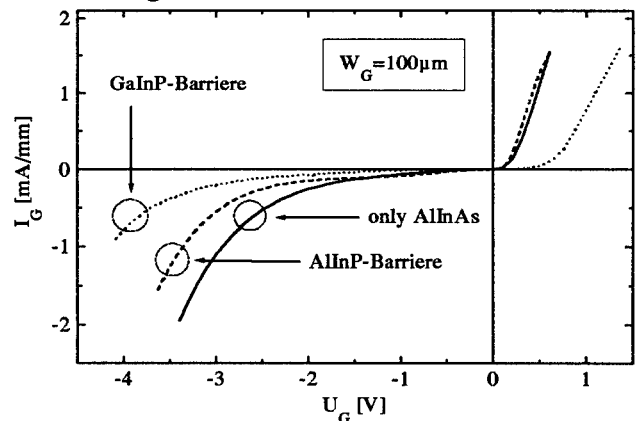
Fig. 4: Gate diode characteristcs of gate contact layers with conventional LTG-AlInAs and with a diffusion barrier of AlInP or GaInP.

167

The lowest leakage current, highest breakdown voltage of -4.2V and highest turn-on voltage is obtained for the GaInP barrier. Therefore such a spacer layer was used in the FET design.

C. LTG-HFET structure

The output characteristic of a planar device as desribed in section (IIC) is shown in Fig. 5. It is noticed that the output current density is only in the range of 2mA/mm. This means that the effective channel sheet charge density is only in the order of $10^{11}cm^{-2}$. Thus, the reduction in PH_3 at the barrier interfaces has also resulted in a reduction of the excess P concentration in a large part of the channel cross section and the sheet charge density is significantly reduced. The device can only partially pinched-off with a leackage current of 0.4mA/mm remaining. Considering the diode IV characteristics as shown above such a leackage current is already expected at low reverse bias. In FET device it is reached at approx. 0.5V.
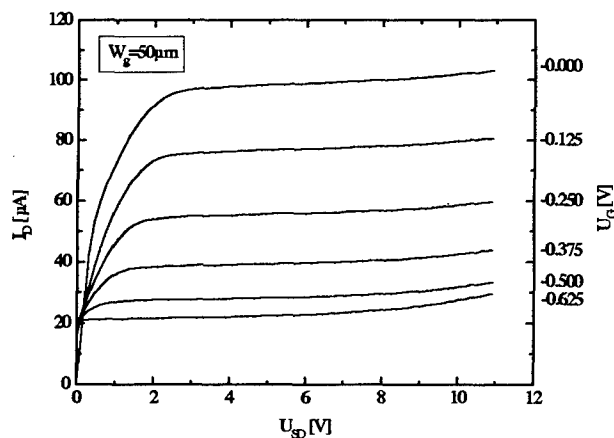
Fig. 5: Output characteristic of a LTG-HFET structure grown and processed at 280°C, shown in Fig. 1.

Thus, the device is still dominated by its paracitics. Nevertheless FET mode of operation is clearly shown. To increase the output current density and transconductance and to reduce the channel series resistencies at the same time the LTG-InP channel quantum well needs still to be optimiced further. In case the sheet charge density is increased by an order of magnitude, but the gate

leackage current not degraded further, it is expected that a current density 20mA/mm may be pinched off at approx. -3V.

Conclusion

A new concept has been presented, which allows to fully fabricate InP FET devices at a reduced termal budget below 300°C. Insulating as well as the active channel layer were grown at this low temperatures. Also the ohmic contacts have been alloyed at this low temperature. It has been shown preveously that the auto-doping is stabil up to at least 400°C, which is a temperature, where standart ohmic contact metallisation systems used in HFETs on InP may also start to show degradation. Thus this technology represents an attractive alternative to the monolitic integration of optoelectronic and electronic components, where the electronic circuitry can be grown without degrading optoelectronic properties, when overgrowing these structures. However the characteristics of the FET still have to be essentially improved. This concerns primarily the increase of output current density. The LTG-InP materials properties (especially the low field mobiliy, which is very similar to that of doped standart material (4)) may suggest that operation in the GHz regime is feasible and that eventually high drain bias operation may be achieved.

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DYNAMIC BEHAVIOUR OF THE METAL HETEROJUNCION BIPOLAR TRANSISTOR.

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Abstract

In this paper the intrinsic dynamic behavior of the Metal Heterojunction Bipolar Transistor (MHBT) is studied. First non–equilibrium electron transport in the base is characterized by electro–luminescence. Clear evidence of ballistic transport in MHBT's is shown even at room temperature. The ballistic length is found equal to 17.8 nm in p–InGaAs ($N_A = 10^{19}$ cm^{-3}). Based on these experimental results, an analytical model is developed in order to predict the transit times in both the base and the base–collector space charge layer of the MHBTs.

I. Introduction

Very fast heterojunction bipolar transistors have been demonstrated (1–4) in the InP–based system. Because the abrupt InP/InGaAs emitter–base heterojunction generates a non–equilibrium electron transport into the base with no degradation of the injection efficiency, it has been intensively used in order to reduce the base transit time (2). On the other hand, device parasitics have been drastically reduced by introducing self–aligned techniques in the device process. As a result the fastest InP–based HBTs exhibit cutoff frequencies and maximum oscillation frequencies as high as 200 GHz (2) and 236 GHz (1) respectively. These impressive performances are mainly limited by the base–collector transit time, t_{bc}, which represents up to 60% of the total emitter–to–collector transit time. A new structure, the Metal Heterojunction Bipolar Transistor (MHBT) has already been proposed (5) using a Schottky collector in order to reduce the electron transit time in the base–collector space charge layer.

MHBT demonstrators fabricated on non–optimized epitaxial structures have shown (6) at $J_C = 58$ kA/cm^2 a current cutoff frequency, f_T, of 40 GHz and a maximum oscillation frequency, f_{max}, of 156 GHz. These results demonstrate the ability of this technology to produce very high speed HBTs. In this paper we present the study of electron transport in both the base and the collector layers in order to define optimized structure for MHBT.

II. MHBT structure.

Epitaxial layers were grown by gaz–source molecular beam epitaxy (GSMBE). The group–III elements are evaporated from solid elemental sources, while the group–V elements are produced by thermally cracking AsH3 and PH3. The detailed growth conditions have been reported elsewhere (7). Epitaxial layer parameters are shown in Table 1.

Based on a fully self–aligned collector–up process, the MHBT fabrication reduces drastically device parasitics (6) and allows the emitter and collector width to be reduced below submicron dimensions. The full transistor (except pad connec-

TABLE 1 Epitaxial layer parameters of InP/InGaAs MHBT's. The n– and p–type dopants were Si and Be respectively..

Layer	Type	Material	Thickness (nm)	Doping (cm^{-3})
Collector	n–	InGaAs	450	undoped
Base	p$^+$	InGaAs	150	1×10^{19}
Spacer	n–	InGaAs	5	undoped
Emitter	n	InP	100	3×10^{17}
	n$^+$	InP	300	1×10^{19}
Sub–emitter	n$^+$	InGaAs	400	1×10^{19}
Substrate	SI	InP		

tions) was patterned with only one masking level using selective wet etching and undercut–based processing. Air–bridge technology was used to connect devices to external coplanar pads (Fig. 1).
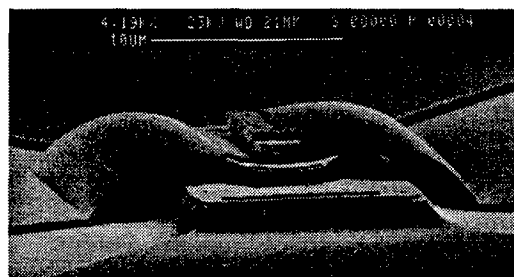
Figure 1 SEM photograph of the MHBT.

Static measurements have shown Ic–Vce characteristics with current gain of 10 and breakdown voltage $BV_{CE0} > 7$ V. Despite the thick base (150 nm) and collector (450 nm) layers f_T and f_{max} of 40 and 156 GHz were respectively achieved (Fig. 2). In the following sections the non–equilibrium electron transport into the base will be characterized in these transistors by electro–luminescence. Based on these experimental results,
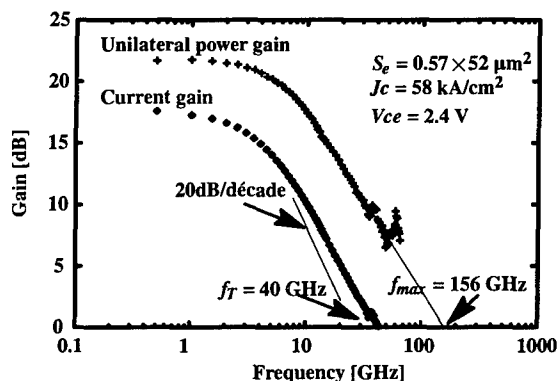
Figure 2 The current gain $|h_{21}|$ and unilateral gain as a function of frequency for device of Fig. 1.

an analytical model has been developed in order to predict transit time in both the base and base–collector layers.

III. Electro–luminescence measurements

The electro–luminescence (EL) signal originates from the electrons flowing into the base and recombining to holes of the valence band (8,9). It must be noted that the radiative recombination rate is negligible compared to other scattering mechanisms and do not participate effectively to hot electron relaxation. In a schematic picture, the photon energy is the sum of the base band gap energy and the energy of the recombining hot electron (see fig. 3). The optical signal is collected through the transparent InP substrate, the rear side of which has been mechanically polished, thus allowing real transistors to be measured without the need of a specific geometry to provide optical access. The measurements are performed for a wide range of temperature, using state of the art sensitivity for the optical detection in the photon energy range of 0.75 to 1.5 eV. Great care has been taken to correct any nonuniformity in the response of the complete optical set–up.
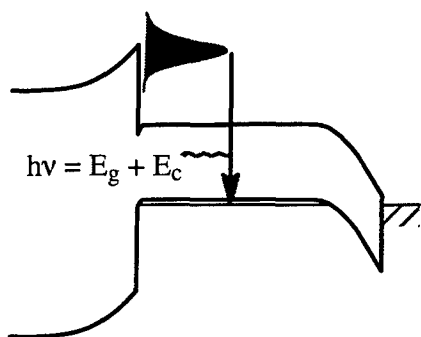
Figure 3 Band diagram of the MHBT. The hot electrons can recombine to holes in the base and emit a photon with an energy proportional to the kinetic energy Ec. The calculated injected distribution is shown.

The first result is the clear evidence that the MHBT exhibit ballistic transport in the base, as shown in figure 4. The EL spectrum at 77K consists in three distinct populations. At low

energy (0.75 to 0.85 eV) the signal originates from electrons relaxed in the bottom of the conduction band, since the peak energy of the distribution (0.78 eV) is equal to the InGaAs band gap. The high energy tail of that peak is the exponential thermal distribution:

$$n(E) = n_0 \exp\left(-\frac{E}{kT}\right) \tag{1}$$

In addition to this thermalized electron population, we observe a peak at higher energy (0.96 eV) which reflects the presence of a peaked distribution of ballistic electrons generated by the emitter–base conduction band discontinuity. These electrons have an excess kinetic energy of about 180 meV, as measured from the splitting of the two EL peaks. This high value indicates that we observe truly ballistic electrons, before they loose any energy by inelastic scattering. Finally, the flat signal in the range 0.85 to 0.92 eV is due to electrons which experienced one or several inelastic scattering but are not yet thermalized.
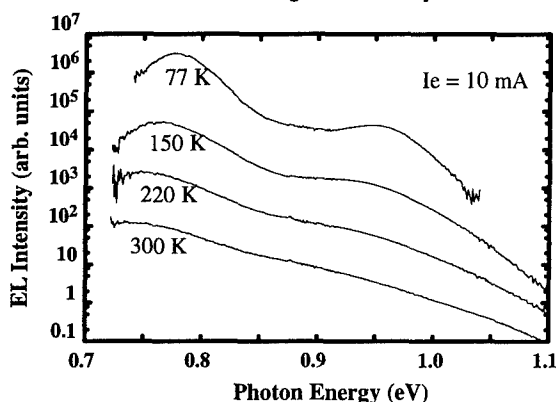
Figure 4 Electro–luminescence spectra from the MHBT for various temperatures. The emitter current density is equal to 5 kA.cm^{-2}

When the temperature is increased, the ballistic population peak broadens due to thermal activation. A non–equilibrium distribution is still visible at room temperature in the range 0.85 to 1.1 eV, demonstrating the presence of electrons with kinetic energy greater than 100 meV. The injected ballistic electron distribution at room temperature, calculated using the thermionic emission theory, including tunnelling, for the emitter–base heterojunction, is plotted in fig. 3. It is then convoluted with the degenerated hole distribution (Fermi energy of about 30 meV) and fitted to the experimental EL spectrum in fig. 5. The only adjustable parameter is the conduction band discontinuity between InP and InGaAs which is found to be of 210 ± 10 meV. For the usable range of V_{be} (0.6 to 0.8 V), no significant change in the ballistic energy distribution is observed, since the major part of the current flows above the heterojunction potential spike, the peak kinetic energy being about 190 meV.

A further analysis of the EL signal can provide direct access to the ballistic relaxation length. The idea is to measure the ballistic electron EL signal as a function of the base thickness. For that purpose, we etched off the collector layer and thinned the base to carefully controlled thickness W_b, using selective wet etching and height profile measurements. Emitter–base diodes

170
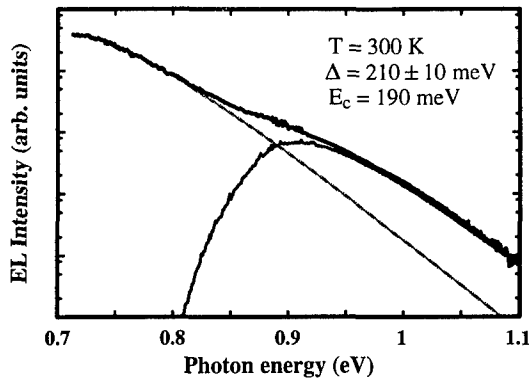
Figure 5 Electro–luminescence spectrum at room temperature. The data are compared to a convolution of the injected ballistic electron and degenerated hole distributions. From the fit, the InP/InGaAs conduction band offset Δ and ballistic electron average kinetic energy Ec are deduced.

with the same geometry as the above described transistors were then fabricated using a non–diffusive Ti/Au base contact. The lineshape analysis presented in fig. 5 allows a precise measurement of the EL intensity originating from the ballistic electrons to be done. This intensity is plotted in fig. 6 as a function of W_b for $V_{be} = 0.75$ V. Assuming a constant inelastic relaxation time the number of ballistic electrons at a distance z from the heterojunction is

$$N_b = N_o \cdot \exp\left(-\frac{z}{L_b}\right) \qquad (2)$$

where L_b is the ballistic relaxation length. The EL intensity I_{EL} is proportional to the total number of ballistic electrons present in the base of width W_b, that is :

$$I_{EL} = \int_0^{W_b} N_b(z) \, dz = I_o \cdot \left[1 - \exp\left(-\frac{W_b}{L_b}\right)\right] \qquad (3)$$
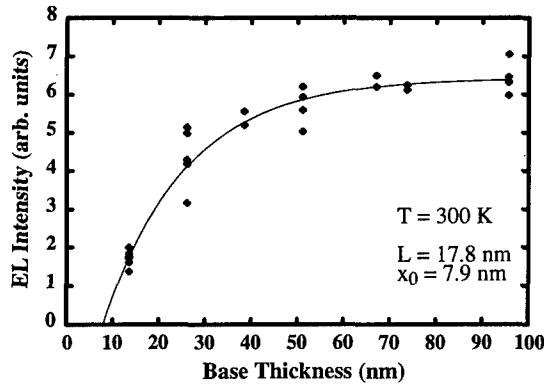
Figure 6 Dependence of electro–luminescence intensity on base thickness at room temperature. From the fit, the relaxation length is equal to 17.8 nm.

The experimental data are very well described by this simple model. The ballistic length $L_b = 17.8 \pm 2.5$ nm is deduced from the fit of equation (3) to the data of fig. 6. The offset of 7.9 nm of the fitted curve is due to the depletion layer under the base

Schottky contact which does not produce EL signal and reduces the effective base width.

IV. Electron transport modelling.
A. Into the base.

From the above results, electrons in the base are described assuming the presence of two populations. 1) the ballistic and quasi–ballistic electrons which cross the base at a constant velocity. 2) the velocity–relaxed electrons which have experienced at least one isotropic interaction and carry a diffusive current. Assuming the recombination current from ballistic electrons is negligible in front of those from the velocity–relaxed electrons, the current carried by the quasi–ballistic electrons writes :

$$J_{QB}(x) = J_E \exp\left(\frac{-x}{L_b}\right) \qquad (4)$$

where L_b is the saturation ballistic length measured at section III and J_E the emitter current density. Assuming the electric field is negligible in the base, the velocity–relaxed current writes :

$$J_{VR}(x) = qD_n \frac{\partial n_{VR}(x)}{\partial x} \qquad (5)$$

where D_n is the diffusive coefficient and n_{VR} the velocity–relaxed electron density. Introducing (4) and (5) in the continuity equation, it gives :

$$D_n \frac{\partial^2 n_{VR}(x)}{\partial x^2} - \frac{n_{VR}(x) - n_0}{\tau_n} = \frac{J_E}{qL_b} \exp\left(\frac{-x}{L_b}\right) \qquad (6)$$

where n_0 is the minority electron density and τ_n their life time. The integration of (6) requires two boundary conditions :

1) Due to the conduction band offset the velocity–relaxed electrons have no chance to diffuse from the base to the emitter. Thus the corresponding current is equal to zero at the emitter–base heterojunction.

$$\left(\frac{\partial n_{VR}(x)}{\partial x}\right)_{x=0} = 0 \qquad (7)$$

2) At $x = W_b$ the mean energy of the velocity–relaxed population is equal to :

$$\epsilon_{VR} = \epsilon_{QB} \exp\left(\frac{-W_B}{L_e}\right) \qquad (8)$$

where L_e is the energy relaxation length. Thus at the collector edge $(x = W_b)$ the mean velocity for velocity–relaxed electrons is equal to the thermal velocity, v_{th}, of this heated population. In these conditions the velocity–relaxed electron density writes :

$$n_{VR}(W_b) = \frac{J_E}{qv_{th}} \left[1 - \exp\left(\frac{-W_b}{L_b}\right)\right] \qquad (9)$$

From the integration of (6) we can write both the density and velocity of the velocity–relaxed electrons. Then the base transit time is computed using :

$$t_B = \int_0^{W_b} dx \, \frac{n_{VR}(x).v_{VR}(x) + n_{QB}(x).v_{QB}(x)}{n_{VR}(x) + n_{QB}(x)} \qquad (10)$$

Figure 7 shows, for various InP–based HBTs, comparisons of the base transit time calculated using equation (10) and using

171

Monte–Carlo simulations (10). The good agreement obtained with L_b = 10 nm and L_e = 20 nm validates our model hypothesis.
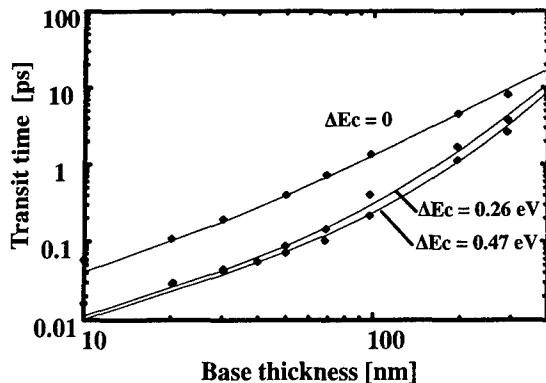
Figure 7 Calculated base transit time versus base thickness. The points are from Monte–Carlo simulations(10). The solid lines are from equation (10).

B. Into the base–collector space charge layer (SCL).

Electrons entering the base–collector SCL are strongly accelerated thus their energy and velocity are increasing till they have enough kinetic energy to transfer from the central valley (Γ) to the lateral valleys (mainly L). Once in the lateral valley their velocity is almost electric field independent and equal to the saturation velocity, v_{sat}. Assuming that both the quasi–ballistic and the velocity–relaxed electrons move into the SCL as a single particle with an initial energy ϵ_{VR} or ϵ_{QB} and an initial velocity v_{th} or v_{QB} respectively, velocity and energy of each population in the Γ–valley are calculated at any point of the SCL. The time dependance of the Γ to L transfer writes :

$$n_\Gamma(t) = n_\Gamma(0)\exp\left(\frac{-t}{\tau_{\Gamma L}}\right) \tag{11}$$

where t is the time spent since the kinetic energy is larger than the energy separation between the Γ– and L– valley, $\Delta E_{\Gamma L}$ and $\tau_{\Gamma L}$ is the reciprocal value of the Γ to L transfer probability. From the density and velocity of each population the transit time in the base–collector SCL is calculated with the equation (10).

Figure 8 shows the base and base–collector transit times as a function of the injection energy. We can notice that, as already observed by Monte–Carlo simulations (11), the base–collector transit time increases with the injection energy because the Γ–L transition probability increases.

Using the above analytical model for the MHBT structure described at section II, the base and base–collector SCL transit times have been found equal to t_b = 1 ps and t_{bc} = 2.45 ps. Thus the low cutoff frequencies measured on these transistors are only due to the thickness of both the base and the base–collector SCL. A total transit time (t_b + t_{bc} = 0.7 ps) five times smaller than the measured value has been obtained with the optimized structure of fig. 8.

V. Conclusion.

In summary, EL spectroscopy permits an evidence of ballis-
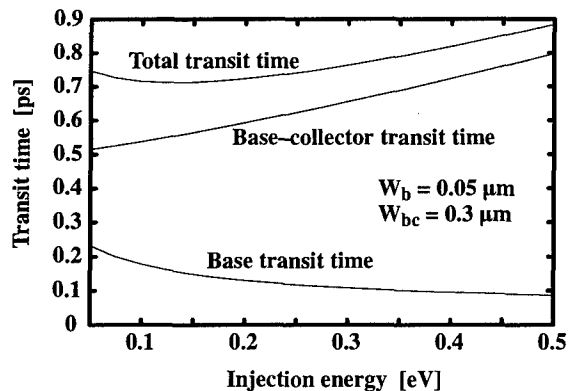
Figure 8 Calculated base and base–collector transit time versus injection energy ϵ_{QB}. Transistors parameters are from reference 11.

tic transport in MHBT's and a precise measurement of the ballistic length to be obtained. The measured L_b value is comparable to state of the art base width, thus indicating that high speed InP–based HBTs utilize the ballistic transport in order to reduce the base transit time. Based on these experimental results an analytical model has shown transit times in both the base and the base–collector SCL which are in good agreement with the literature. This model will be used to design optimized epitaxial structures for MHBTs.

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A SLOW-TRAP MODEL FOR THE KINK EFFECT ON InAlAs/InP HFET

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I. Introduction

Heterostructure Field Effect Transistors (HFET's) on InP are very interesting devices for optical communication components. These transistors can be monolithically integrated with optical emitters or modulators as well as photoreceivers. HFET's with n-doped InP channel layers and AlInAs barrier layers are suitable for low to medium frequency applications which require high breakdown voltages and a very small gate leakage current [1].

However, InP based HFET's present an important anomaly in their DC current-voltage (I-V) curves: a sharp increase in the saturated drain current with respect to drain bias that leads to high drain-source conductance (g_{ds}). It is important to understand and minimize this phenomenon, called "kink effect", in order to obtain devices with good performances for low noise and digital device applications.

Many studies have been performed to explain this kink effect [2,3]. One of the two main models presented, established a link between the kink effect and the impact ionization for the system InAlAs/InGaAs [3], while the second consider the trapping and detrapping of carriers in the InAlAs layers [2]. In our devices the impact ionization is negligible because an InP channel is used. In order to explain the kink effect in our transistors we have performed temperature and frequency analysis of the I-V characteristics.

II. Device Fabrication

The transistors were fabricated on commercially supplied epitaxial structures grown by metal organic vapor phase deposition (MOCVD) on semi-insulating Fe-doped InP substrates. Two kinds of structure have been analyzed: one with an InP buffer and another with an InAlAs buffer. The lattice matched InAlAs/InP HFET structure consists of a 30 nm undoped InP (or $In_{0.52}Al_{0.48}As$) buffer layer, a 50 nm sulfur doped InP channel ($n = 2-3 \times 10^{17}$ cm^{-3}), a 50 nm $In_{0.52}Al_{0.48}As$ Schottky barrier, and a 15 nm heavily doped $In_{0.53}Ga_{0.48}As$ contact layer (Fig. 1).
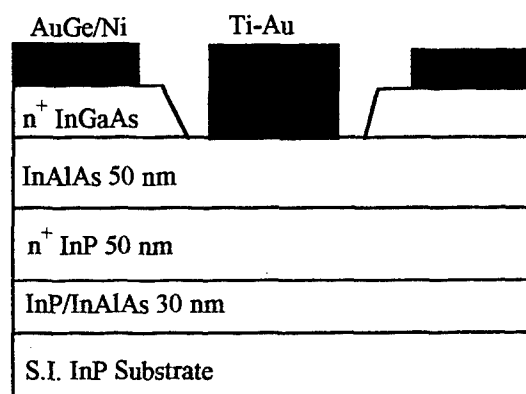
Fig. 1 HFET cross section

Fabrication consists of device isolation via mesa wet chemical etching followed by AuGe/Ni ohmic contacts deposition by e-beam evaporation and annealing at T= 360°C. A UV-CVD silicon nitride (Si_3N_4) was then deposited on the entire wafer followed by a dry etch inside the mesas, leaving the device edges and substrate regions covered with dielectric. After the gate lithography, the InGaAs cap layer was selectively etched down to the InAlAs barrier layer with a citric acid/hydrogen peroxide solution. For gate contact (1 μm length) Ti and Au was evaporated and lifted-off [4].

Typical output characteristics present high breakdown voltages, due to the high band-gap of InP (V_{BK} = 14 V), good pinch-off values (close to the expected value of -1 V) and a very low gate leakage current (4nA/mm). These performances make the transistor suitable for high sensitivity integrated photoreceiver applications.
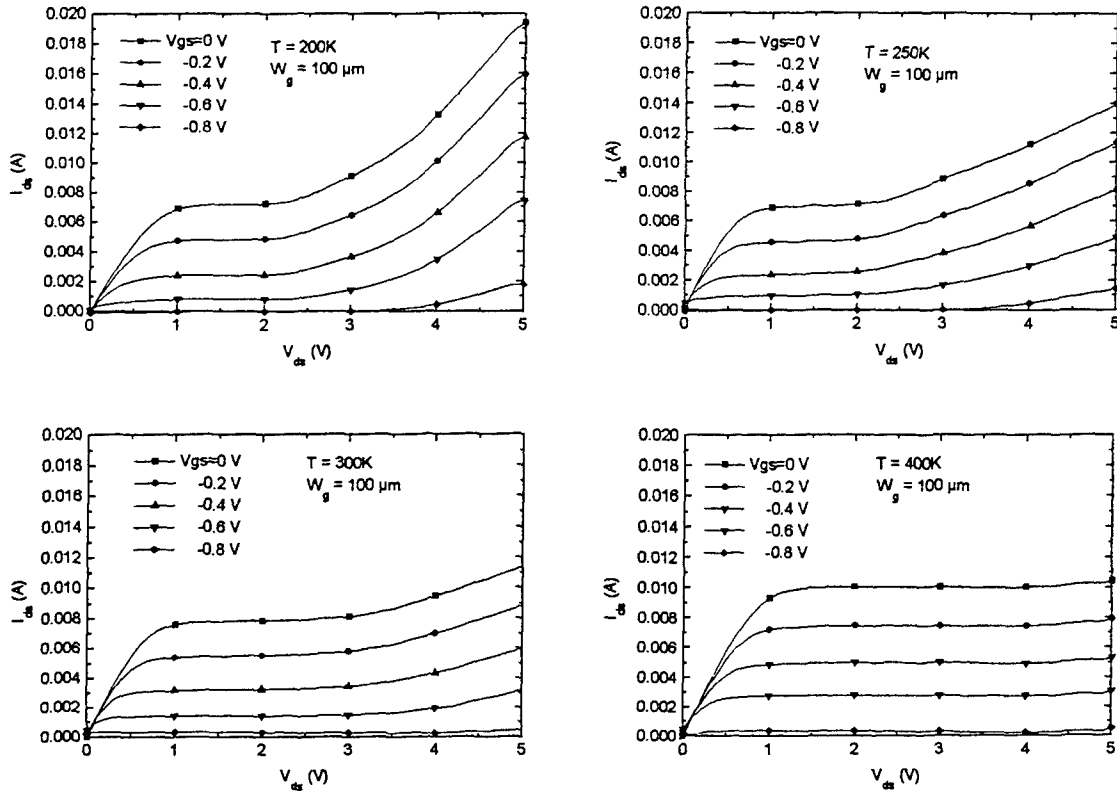
Fig. 2 I-V characteristics as a function of temperatures

III. Experimental Results

The behaviour of the kink effect is studied at different temperatures ranging from 200 K to 400 K. In Fig. 2 is presented the evolution of drain I-V characteristics with the temperature for the HFET's with InP buffer layer. At low temperatures (200 K) the kink effect is very important, while at high temperatures (400 K) it is almost suppressed. It is very important to note that the temperature dependence of I_{ds} reverses at V_{kink}. The drain current increases with the temperature for $V_{ds} < V_{kink}$ (50 % higher at 400 K than at 200 K), while for $V_{ds} > V_{kink}$, I_{ds} decreases (for the same V_{ds}). The same behaviour was observed in the case of an InAlAs buffer layer.

Previous measurements [2,5] have proved that the kink effect is a low frequency mechanism, absent at microwave frequencies (f > 1 GHz). In order to study the behaviour of I_{ds} and g_{ds} at low and very low frequencies, I-V characterization was performed in a frequency domain ranging from 1 Hz to 100kHz. Fig. 3 shows the experimental setup used in these measurements. To obtain the I_{ds} -V_{ds} dynamic curves, a triangle signal is applied at the drain. The converted drain-source current and the

drain-source voltage are recorded on a digital oscilloscope. A triangular sweep is used in order to observe a possible hysteresis. In Fig. 4 we present the curves corresponding to $V_{gs} = 0$ V bias, for different frequencies. The DC curve is plotted for comparison.
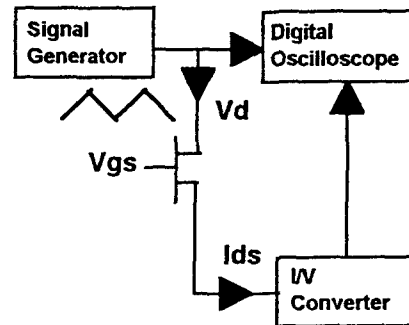
Fig.3 Diagram of the measurement circuit used to extract the dynamic I_{ds} - V_{ds} characteristics

At very low frequencies, f = 1 Hz, the kink effect is observed and the hysteresis is quite small. At frequencies one decade higher, the kink effect starts to decrease, while the hysteresis becomes important. And for f >1kHz the kink effect and the hysteresis are practically not observed at room temperature.

174
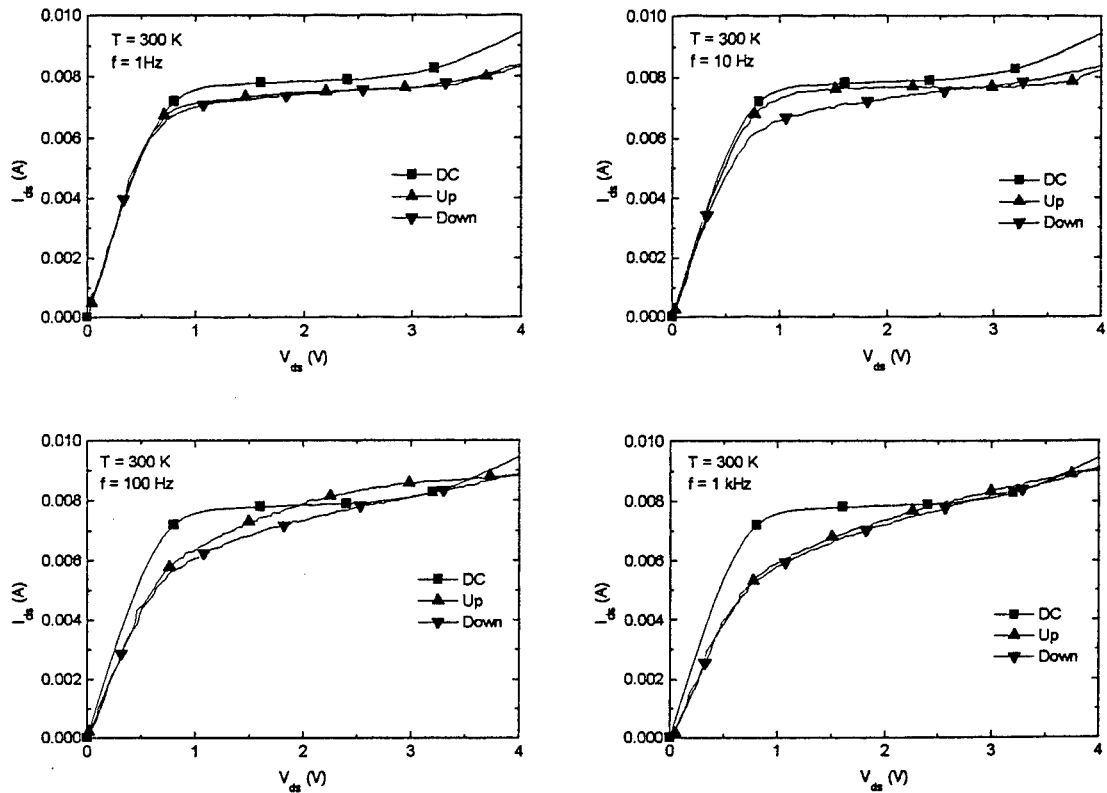
Fig. 4 I-V characteristics for $V_{gs} = 0$ as a function of frequency

IV. Discussion

This bias-sweep measurements indicate that the kink effect increases at low temperatures and could be observed only at very low frequencies. Our results suggest that the increase of the DC g_{ds} in the saturation zone, associated with the kink effect (Fig. 5) is caused by a slow state related mechanism. The same hysteresis and kink effects have been observed for the transistors with an InAlAs buffer layer, which allows us to suppose that these states are probably lying in the InAlAs barrier layer.
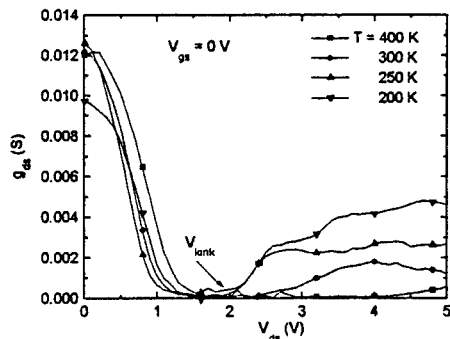
Fig. 5 The increase of g_{ds} at V_{kink} as a function of temperature, for $V_{gs} = 0$ V

At low temperatures, the slow states are filled with electrons and the charge of the trapped electrons acts as a parasitic negatively biased gate ($-\Delta V_{gs}$) which induce an early saturation of the drain current. At $V_{ds} > V_{kink}$, the electric field is high enough to produce an ionization of these states, and therefore, the effect of the parasitic gate is suppressed. This will lead to an increase of I_{ds}.

At high temperatures, the emission coefficient of the states increases, so only a little part of them are filled. In this case, $-\Delta V_{gs}$ is reduced, so the DC saturation current increases. The density of states ionized by the electric field is lower and the kink effect is reduced.

This model can also explain the frequency behaviour of the I-V dynamic characteristics. At room temperature, at very low frequencies (f = 1 Hz) the states are able to follow the drain-source excitation signal, so the kink effect is observed, while hysteresis is not present. With increasing frequency (f =10-20Hz), a hysteresis is observable. In fact, when V_{ds} increases form 0 to 4V ("up"), the states are ionised for $V_{ds} > V_{kink}$. Then, when the bias is decreased from 4 to 0V ("down"), the traps need a certain time to capture electrons, and therefore, the kink effect decreases. Also, at f = 100 Hz, the emission no longer follows the V_{ds} signal and the kink diminishes. For medium frequencies

175

(1kHz - 10kHz) the trapping and detrapping mechanisms are not able to follow the applied signal, so the kink effect and the hysterezis disappear.

In order to characterize these states, drain conductance dispersion measurements were performed. The variation of the drain conductance with the frequency for different temperatures [6] is presented in Fig 6. The associated Arrhenius plot is given in Fig. 7. This level appears to be the electron trap responsible for the kink effect. At room temperature, the corresponding variation of g_{ds} appears in the domain 10 - 60 Hz (like the maximal hysteresis in the dynamic I-V curves). This level seems to be the same as the one reported by E. Béarzi et al [7] in InAlAs MOCVD layers and is generally referred as E3 in the literature of InAlAs defects.
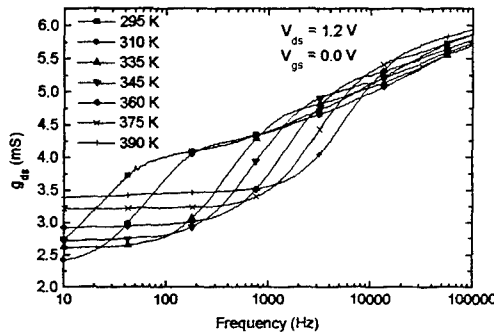
Fig. 6 Drain conductance dispersion as a function of temperature
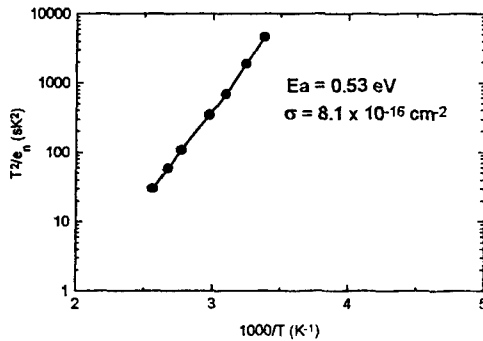
Fig. 7 Arrhenius plot of drain conductance dispersion

By calculating the emission rate at ambient temperature using (1)

$$e_n = K_n \sigma_n T^2 \exp - \left[\frac{E_C - E_T}{kT} \right] \quad (1)$$

with

$$K_n = \frac{2\sqrt{3}(2\pi)^{3/2} m_n^* k^2}{h^3} \quad (2)$$

we obtain an emission rate around 22 s^{-1}, corresponding to slow-states at T = 300 K. So, it seems very probable that this level in the InAlAs layer is involved in the kink effect.

V. Conclusion

The kink effect in InAlAs/InP HFETs was examined in temperature and frequency dependent measurements. A slow states mechanism is found to be probably responsible for the increase of the drain-source conductance related to the kink effect. A deep-level with activation energy of 0.53 eV was deduced from drain conductance dispersion measurements. This level, with a slow emission rate at room temperature, seems to be associated with the kink effect.

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A passive V-band mixer is presented which uses an InP HEMT for mixing. The measured minimum conversion loss is 10.3 dB (RF 61 GHz, LO 60 GHz) with an LO power of 6 dBm. The circuit was fabricated in coplanar technology.

I. Introduction

Commercially available wireless LANs have transmission rates of only a few Mb/s [1] which is low compared to conventional wired networks. To be able to handle higher data rates, future wireless LANs will probably have to be designed in the mm-wave frequency range where the available bandwidths are larger. Other possible applications for mm-wave systems are, for example, collision avoidance radar [2], [3] or broadband wireless TV distribution. Standards for wireless TV distribution are being developed for the 28 GHz and 42 GHz bands and prototype systems have successfully been tested in the US and Europe [4]. A key component for frontends and transmitters in these systems is the mixer. This work describes a passive, monolithically integrated HEMT mixer using an InP HEMT device. The advantages are unconditional stability, lower intermodulation and no need for a DC drain bias voltage [5].

II. Fabrication

The device used for mixing is a lattice matched InP HEMT. The structure of the MBE grown material is shown in Table 1. The measured mobility at room temperature, sheet

Table 1: Material structure of the lattice matched HEMT device.

cap	GaInAs	12 nm	$5 \cdot 10^{18}$ cm^{-3}	53% In
Schottky layer	AlInAs	20 nm	undoped	52% In
donor layer	AlInAs	10 nm	$5 \cdot 10^{18}$ cm^{-3}	52% In
spacer layer	AlInAs	3 nm	undoped	52% In
channel	GaInAs	50 nm	undoped	53% In
buffer	AlInAs	250 nm	undoped	52% In
substrate	semi-insulating InP			

carrier density and sheet resistance are $\mu_h = 10400$ cm^2/Vs, $n_s = 3.44 \cdot 10^{12}$ cm^{-2} and $R_s = 170$ Ω/sq. The seven process steps in chronological order are: ohmic contact, mesa isolation, gate definition, first metallization, dielectric isolation, thin film resistor and second metallization. Both the metal layers are evaporated Ti/Au and have a thickness of

260 nm. The dielectric isolation used for the capacitors is evaporated silicon oxide. The 100 nm thick layer yields a capacitance value of 0.5 fF/μm^2. The low value resistors are fabricated with evaporated titanium (34 nm) having a sheet resistance of 25 Ω/sq. Large resistors (> kΩ) are formed using mesas of device material. For the fabrication of the T-gate, a three layer resist system was developed in [6]. The multi-path exposure is performed with a modified scanning electron microscope (SEM). The resulting gate length is 0.2 μm and the DC-resistance 180 Ω/mm.

The transit frequency and the maximum frequency of oscillation of the standard HEMT device, with two gate fingers of a total gate width of 150 μm, are $f_t = 150$ GHz and $f_{max} \approx 200$ GHz. Coplanar technology is used to simplify the processing since it requires no wafer thinning and no via holes. To prevent any slotline mode at a coplanar waveguide (CPW) discontinuity, bonding wires were used to short the ground planes (see Fig. 5).

III. Small-Signal Equivalent Circuit Extraction

The mixer design was done with the small-signal equivalent circuit in Fig. 1 consisting of three classes of elements [7], [8], [9]: parasitic, extrinsic and intrinsic elements. The intrinsic elements originate in the active part of the channel located directly below the gate. They depend on the material structure, the layout geometry and the bias voltages. The extrinsic elements take into account the resistances between the active region and the input and output lines as well as the inductances and capacitances of the gate,
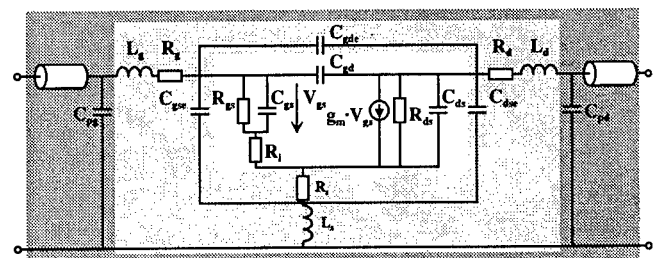
Fig. 1: Small-signal equivalent circuit of the single HEMT (white: intrinsic elements, light gray: extrinsic elements, dark gray: parasitic elements).

drain and source metallization. The extrinsic elements depend on the gate width, but not on the bias voltages. The parasitic elements result from the input and output transmission lines, which are needed for measuring the transistor. They are independent of the gate width and the bias voltages.

In the following, the extraction process of the element values is outlined. The parasitic elements were determined from the measured scattering parameters [10] of a separate test structure. The extrinsic elements were measured with DC-measurements and RF-measurements. The RF-measurements were carried out with HEMTs under reverse bias and forward bias ("hot/cold" measurements) and on a second test structure. Finally, the intrinsic elements were calculated from the measured scattering parameters after de-embedding the extrinsic and parasitic elements.

A. Parasitic Elements

To determine the parasitic elements, a test structure consisting of only the input and output line of the transistor was fabricated on semi-insulating material. The transmission line parameters were extracted from the measured scattering parameters of this test structure.

B. Extrinsic Elements

The gate resistance was measured on a test gate on semi-insulating material. The effective gate resistance used in the small-signal equivalent circuit is a third of the measured value because of the distributed gate resistance [11].

The source and drain resistances were measured with the "end" resistance method [11]. A positive current was applied at the gate. The ratio of the drain-source voltage V_{DS} and the gate current I_g defines the resistance

$$R_t = \frac{V_{DS}}{I_g} = R_s + \alpha R_{CH},\qquad(1)$$

which includes the source resistance and channel resistance multiplied with the α-factor. The α-factor depends on the gate current and becomes zero for high gate currents. Therefore, when R_t is plotted versus the inverse gate current ($1/I_g$), the intercept at the y-axis is the source resistance. The determination of the drain resistance is analogous except that the drain and the source are interchanged.

The extrinsic capacitances were determined with a second test structure, which was processed like a normal HEMT device but on a semi-insulating substrate. From the scattering parameters of the test structure the extrinsic capacitances C_{gse}, C_{gde} and C_{dse} were fitted.

The extrinsic inductances could not be extracted from this test structure because the scattering parameters are sensitive to capacitances but not to resistances or inductances.

For inductance sensitive scattering parameter measurements, the transistor has to be forward biased. The used method is called "hot/cold" measurements [12]. Two scattering parameter measurements are necessary: one under forward bias, the other under reverse bias. The drain-source voltage is zero ($V_{ds} = 0$ V) for both measurements, which simplifies the equivalent circuit considerably. From these two measurements the extrinsic inductances were determined.

C. Intrinsic Elements

The intrinsic elements can be calculated from the measured scattering parameters when the two outer shells with the parasitic and extrinsic elements are known. For more accurate values, the elements were optimized by fitting the simulated scattering parameters to the measured ones. This process was carried out for different bias voltages to obtain the bias dependent values.

Excellent agreement was obtained between the measured and the simulated scattering parameters. As an example, the comparison between measured and simulated forward transmission of a typical HEMT device is plotted in Fig. 2. A small discrepancy can be seen in the magnitude of S_{21} at low frequencies. The error is due to a dispersion of the transconductance g_m and the drain-source resistance R_{ds} [13]. Hence, the values are not correct at low frequencies (< 3 GHz). At millimeter-wave frequencies this is no limitation.

When the model is used in a circuit simulation, the parasitic elements are omitted since they model the input and output lines of the standard HEMT device, not present in the circuit. Only intrinsic and extrinsic elements are used.
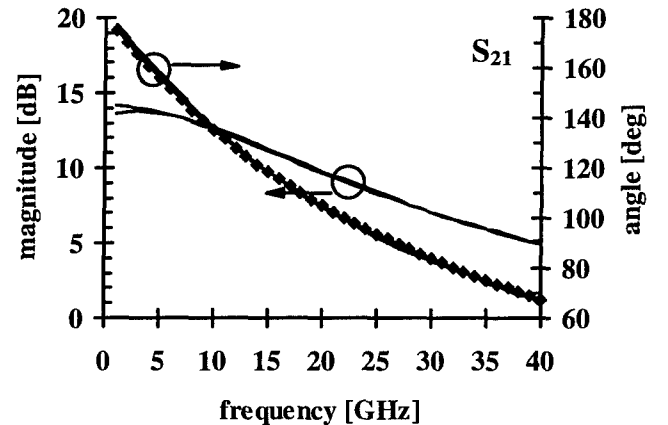
Fig. 2: Measurement and simulation of angle and magnitude of the forward transmission S_{21} ($V_{gs} = -0.4$, $V_{ds} = 1.5$ V).

IV. Mixer Design

The mixer circuit (Fig. 3) consists of a standard HEMT with matching and bias networks. The local oscillator (LO) is applied at the gate and modulates the HEMT output conductance with the LO frequency. The radio frequency (RF) is applied at the drain of the HEMT. The IF is extracted through a $\lambda/4$ stub (at RF frequency) at the drain which is RF-shorted by C_1. The filtering of the RF and IF is achieved by
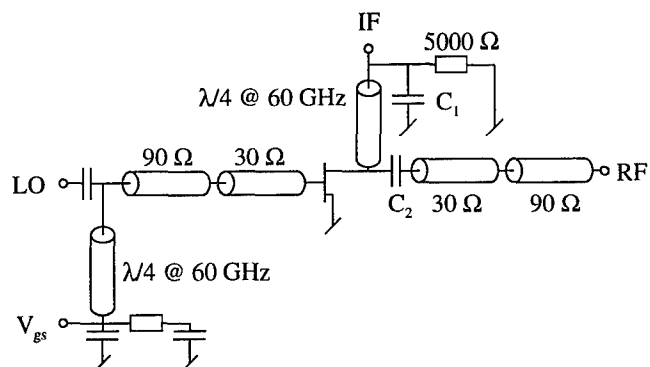
Fig. 3: Schematic of the V-band passive HEMT mixer. The transmission lines are coplanar waveguides.

the capacitors C_1 and C_2. They have to be sufficiently small so that the IF is not reflected by C_1 and does not appear at the RF port. However, if they are too small, the RF is reflected by C_2 and by the stub at the IF port. The matching of the RF- and the LO-port is achieved by coplanar waveguides connected in series.

The simulation of the CPWs was done with a conventional transmission line model whose characteristic impedance, dielectric constant, attenuation and length had to be specified. The final dimensions of the CPW for the layout were calculated by LineCalc [14]. However, when the discontinuities of the T-junctions are not taken into account, the simulation is erroneous. Therefore, the scattering parameters of the T-junctions were calculated with an electromagnetic simulator [15] and were included in the simulation as data files. The small-signal isolation between the LO and the RF port is plotted in Fig. 4 up to 70 GHz. There is a good agreement between the measured and the simulated curves over the whole measured frequency range. The measured isolation is better than 7.5 dB.
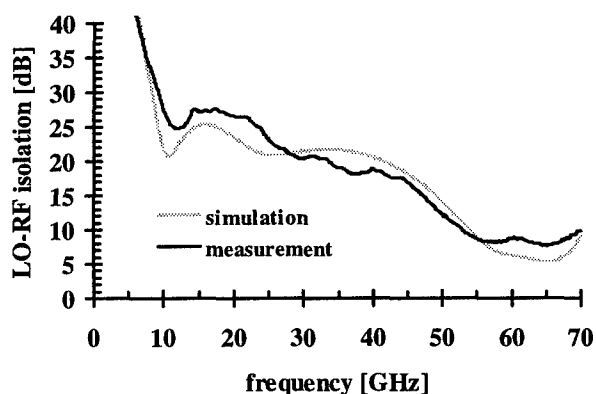
Fig. 4: Measured and simulated small-signal LO-RF isolation.

Fig. 5 shows a photograph of the fabricated passive V-band HEMT mixer, which has a size of 3.5 mm². The bonding wires, preventing any slotline mode on the CPW, clearly can be seen.
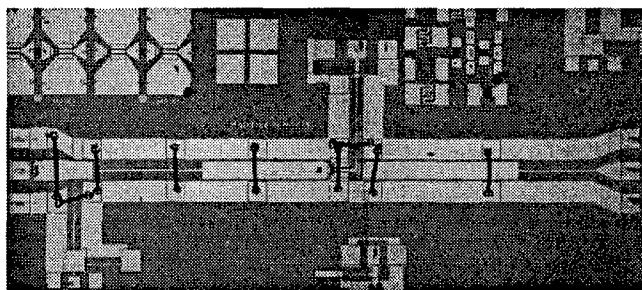
Fig. 5: Photograph of the passive HEMT mixer circuit (3010·1150 μm²). Bonding wires were used to short any parasitic slotline mode on the CPW.

V. Measurements

The mixer was measured as a down-converter. For the measurements the LO was fixed at 60 GHz. The LO was generated with a 30 GHz signal that was amplified and doubled. The RF was taken from the mm-wave extension of the network analyzer (NWA HP8510C). The conversion loss, defined as the available power at the RF-port of the circuit divided by the output power at the IF-port, is shown in Fig. 6 when the RF is swept from 61 to 71 GHz. The cable losses are
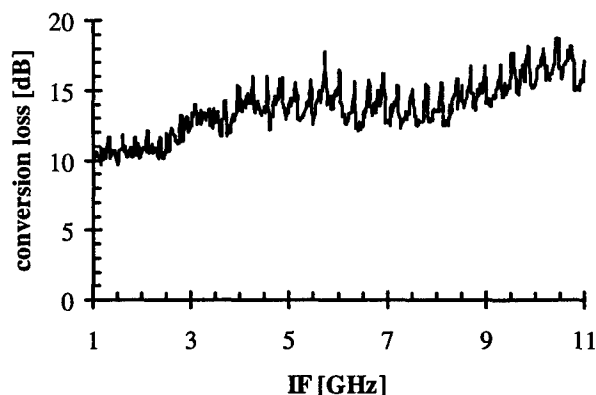
Fig. 6: Conversion loss vs. IF. The LO was fixed at 60 GHz and the RF swept from 61 to 71 GHz.

accounted for. The ripple is introduced by reflections generating standing waves on the cables. Fig. 7 shows the conversion loss and the IF output power versus LO power. Compared to active HEMT gate mixers, the conversion loss is weakly dependent on the LO power [16]. The minimum loss is 10.3 dB at an LO power of +6 dBm.

179
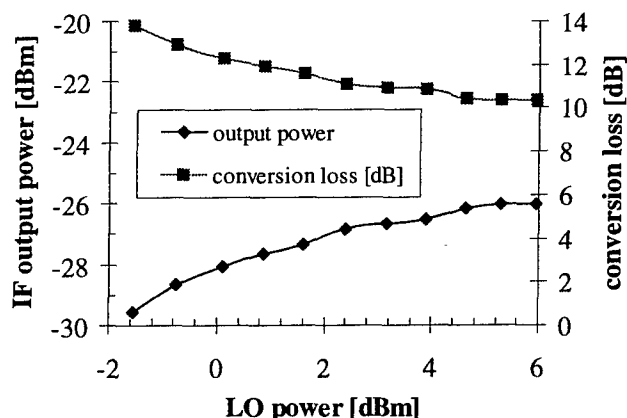
Fig. 7: Conversion loss and output power of the V-band mixer vs. LO power (LO: 60 GHz; RF 61 GHz, -16 dBm).

The conversion loss and the IF output power versus RF power are plotted in Fig. 8 for an LO power of +6 dBm. The figure shows that the 1 dB compression point is not yet reached for an RF power of -1 dBm. Active mixers, however, saturate at lower RF power levels relative to the LO power [17].
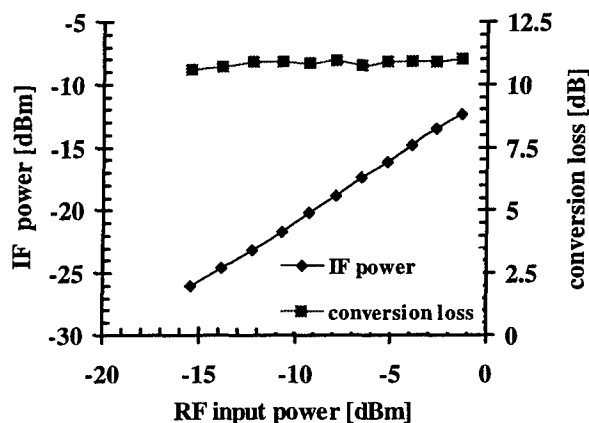
Fig. 8: IF output power and conversion loss vs. RF power (LO: 60 GHz, +6 dBm; RF 61 GHz)

VI. Conclusion

In this work a coplanar passive HEMT mixer is reported. The conversion loss for an RF of 61 GHz and an LO of 60 GHz is 10.3 dB. This is the lowest value for a coplanar passive HEMT mixer at V-band. The circuit can be an alternative to an active HEMT mixer because it is less sensitive to the LO and RF power, it has inherent RF to LO isolation and it is unconditionally stable.

Acknowledgement

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InAlAs/InGaAs/InP DUAL-GATE-HFET'S: NEW ASPECTS AND PROPERTIES

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Introduction

Dual-Gate Heterostructure Fieldeffect-Transistors (**DGHFET**) regarded a full 3-port device are typically used for mixers, oscillators and variable gain amplifiers due to the second controlling gate electrode [1,2]. Cascode configurations are of increasing interest for high frequency applications because of the reduced feedback and increased output resistance caused by the second gate. Therefore, an improved voltage gain and maximum stable gain corner frequency f_{MSG} results. Based on GaAs-substrate a 0,25 µm Dual-Gate cascode [3] has demonstrated significantly higher stable gain at the same noise figure compared to his SGHFET counterpart thus yielding a correspondingly improved SNR which can be directly transformed into an e.g., increased sensitivity of an OEIC receiver [4]. On the other hand there are obstacles like need of an additional bias for the second gate, difficult parameter extraction, and increased efforts for reliable simulation and modelling. In the InAlAs/InGaAs/InP-system, additionally, high gate leakage current originating from impact ionization in the low bandgap channel has to be considered in device fabrication and characterization [5]. In this contribution key issues of this development are adressed and new properties of DGHFET-cascodes in the InAlAs/InGaAs/InP-system are presented. Optimum bias conditions for the intrinsic voltages of the DGHFET-cascode are evaluated resulting in suppression of impact ionization in the channel underneath the rf-driven gate yielding extremely low gate leakage in the nanoampere region at conventional gate widths, high frequency capability (f_T=100GHz) and low minimum noise figure (1dB at 12GHz).

I. Device Fabrication and Performance

The DGHFET layer structures investigated in the first part of this paper (DC-analysis) are lattice matched to InP-substrate grown by solid source MBE on s.i. InP-substrate. After mesa etching and fabrication of the GeNiAu ohmic contacts both gates of the DGHFET were simultaneously processed by electron beam lithography using a three layer resist stack resulting in 0.22µm gates with a Γ-shaped cross-section. The gates were recessed in a wet chemical etching step using selective citric acid. Optimization of the gate recess results in threshold voltages of $V_{T1,2}$ = -1V leading to the best device performance at V_{G2S} = 0V in case of the DGHFET (index "1" or "2" in this paper specifies the first and the second part of the DGHFET, resp.). Hence, as far as rf-design is concerned, the second gate can be directly shorted to the source (ground), which is very advantageous for MMIC design [3], because no additional bias is required. In case of these DGHFET the investigations concentrate on two different selected bias conditions: mode A is represented by the floating second gate, whereas the condition V_{G2S} = 0V specifies mode B. In the second part of

this paper (RF-analysis) DGHFET-cascode devices with T-shaped gates (L_G=0.16µm) are analyzed. Due to a DC-blocking capacitance these devices offer to vary V_{G2S}.

II. DC-Analysis

Impact ionization is caused by the electric field in the InGaAs-channel due to the drain source voltage V_{DS} [7]. Experimental investigations of the input characteristics, represented by the gate leakage current I_{G1}, in dependence on V_{G1S} and V_{DS} as parameter, were carried out to analyze impact ionization in DGHFET's. In general, the total leakage current consists of two components [4]: 1) electron tunneling from the Schottky-gate to the channel which results in a steady increase of the gate current with increasing negative bias V_{G1S}; and 2) holes generated by impact ionization in the high field region of the InGaAs channel, tunneling through the InAlAs valence band barrier. In fig. 1 the gate leakage I_{G1} of the investigated DGHFET measured in mode A is compared to that in mode B.
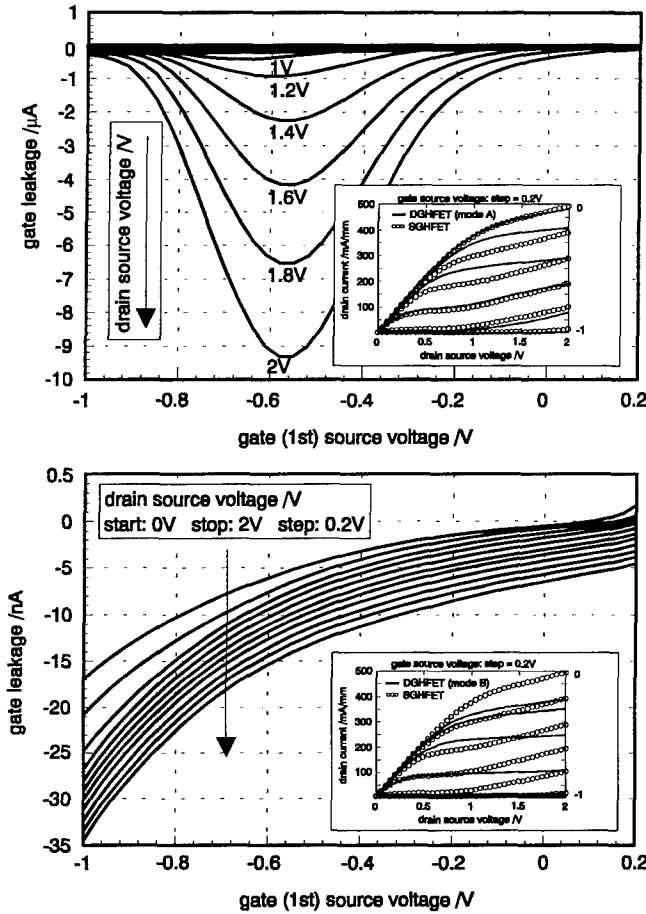
Fig. 1: Gate leakage current I_{G1} of the rf-driven gate of the DGHFET in dependence of the gate-source voltage V_{G1S} with the drain-source voltage V_{DS} as parameter measured in mode A and at $V_{G2S} = 0V$ (mode B) with corresponding output characteristics I_D (V_{G1S}, V_{GDS}) in comparison to the SGHFET

In case of mode A a peak in the input characteristics at about $V_{G1S} \approx -0.6V$ is observed, indicating impact ionization, identical to the behaviour of conventional SGHFETs. Only for $V_{DS} < 1V$ this current peak disappears. Consequently, prevention of impact ionization in case of the InAlAs/InGaAs SGHFET requires a reduction of V_{DS} to extremly low values. But for such bias conditions the device performance in terms of transconductance, output conductance and thus high frequency properties is far from optimum. In case of the DGHFET the second gate offers a local controlling of the intrinsic electric field in the channel below the first gate without the necessity to reduce the extrinsic drain source voltage of the device. The gate leakage current I_{G1} is now measured in mode B for the same range of V_{G1S} (fig. 1). The missing bump indicates, that impact ionization is completely suppressed below the first gate. Consequently, the gate leakage current is drastically reduced -by more than a factor of 250-, and only the electron tunneling component of I_{G1} is present. This behaviour was analyzed by the evaluation according to a nomogram after C. Tsironis et al. [8] (fig. 2): The DGHFET

is described as a cascode configuration of two separate SGHFETs. At $V_{DS} = 3.6V$ both intrinsic FETs are measured separately, and characteristics are plotted in the diagram using the equations in fig. 2.
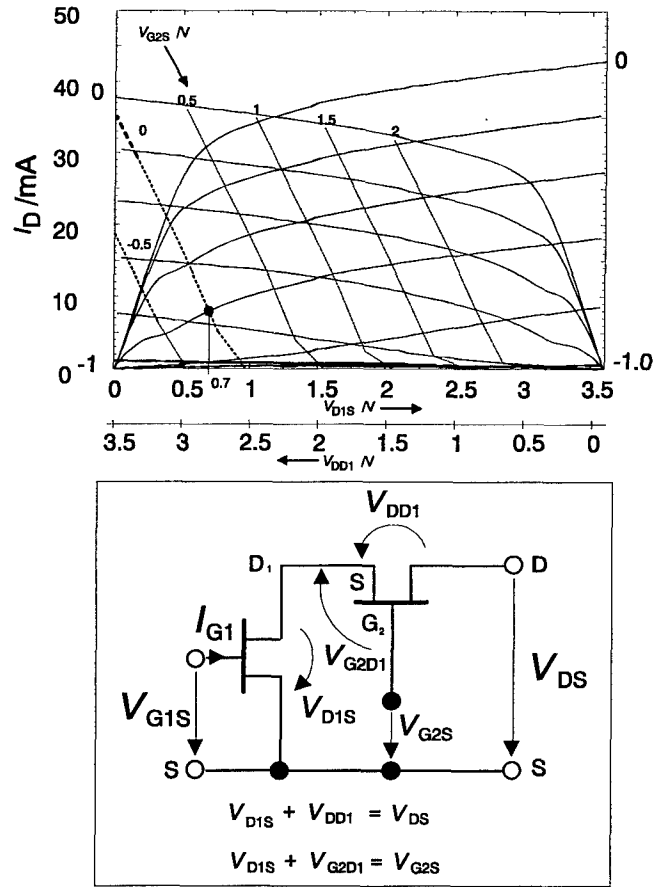
Fig. 2: Nomogram measured at $V_{DS} = 3.6V$ evaluating the output characteristics of the first and the second intrinsic FET I_D (V_{G1S}, V_{D1S}), and I_D (V_{G2D1}, V_{DD1}) including the equivalent circuit with corresponding equations of the DGHFET cascode ($W_{G, DGHFET} = 100\mu m$)

From the nomogram the intrinsic drain source voltages V_{D1S} and V_{DD1} of the DGHFET at $V_{G1S} = -0.6V$ and $V_{G2S} = 0V$ can be extracted: $V_{D1S} < 1V$, insufficient to generate impact ionization, and $V_{DD1} > 2V$, leading to both, high saturation current I_D and high transconductance g_m. In addition the controlling mechanism of the second gate in term of V_{G2S} on the saturation of I_D can be seen.

Using a quasi-2dimensional, non-stationary, numerical model [6], both, the electric field and the potential distribution in the channel between source and drain of the investigated DGHFET were simulated at $V_{DS} = 3.6V$ and $V_{G2S} = 0V$, verifying, that the electric field underneath the rf-driven first gate is significantly reduced. The simulated intrinsic drain source potential V_{D1S} corresponds exactly to that extracted from the nomogram.

II. RF-Analysis

Bias dependent s-parameter measurements from 45MHz to 40GHz at room temperature of both, dual- and single gate HFET ($L_G = 0.16\mu m$) were carried out: Due to its physical nature, the DGHFET shows the expected loss of f_T in comparison to its SGHFET counterpart ($f_{T,SG}$=154GHz, $f_{T,DG}$=115GHz). But because of the drastic reduction of both, output conductance and feedback as demonstrated in fig. 3, the measured DGHFET offer a 8dB higher maximum stable gain and consequently a f_{max} as high as 300GHz in spite of 220GHz in case of th SGHFET. In addition to these conventional advantages in this section the DC-results of the DGHFET-cascodes described above will be reflected by additional rf-measurements and small-signal analysis in dependence of V_{G2S}. Three different bias conditions (mode I, II, III) were choosen to analyze impact ionization in the device (table 1).

Table 1 Extrinsic and intrinsic bias conditions of the DGHFET driven in different modes and transconductances related to impact ionization

	mode I	mode II	mode III
V_{DS} /V	3	3	3
V_{G1S} /V	0.1	0.1	0.1
V_{G2S} /V	0.6	1.45	2.3
V_{D1S} /V	<1	1.5	>2
V_{DD1} /V	>2	1.5	<1
$g_{m,im1}$ /mS	0.22	1.31	2.11
$g_{m,im2}$ /mS	5.02	3.02	0.23

For meaningful comparison of the s-parameters all modes exhibit nearly the same drain currents ($I_D \approx$ 20mA) and cut-off frequencies ($f_T \approx$ 80GHz). The different bias conditions represent different saturation conditions for both of the intrinsic FET of the DGHFET-casode. Mode I represents a intrinsic drain source voltage of the first FET at the very beginning of the saturation region, which is too low to generate impact ionization underneath the rf-driven gate whereas the second FET is fully saturated; mode II represents equal intrinsic drain source voltages V_{D1S} and V_{DD1}, corresponding to full saturation of both intrinsic FET; mode III is inversed to mode I. The corresponding measured and modelled s-parameters are illustrated in fig. 3. For characterization of the impact ionization effect both, the output-reflectance $\underline{S}_{22}$ and the transmission $\underline{S}_{21}$ has to be fundamentally discussed [9]: When impact ionization occurs in the device, $\underline{S}_{22}$ shows an inductive behaviour at low frequencies which can be described by an additional tranconductance $g_{m,im}$ controlled by the electrical field between gate and drain combined with a low pass filter. Simultaneously, a deterioration of the power gain represented by a decrease of $|\underline{S}_{21}|$ can be observed in the same frequency range. A detailed description of the rf-model of the impact ionization effect for SGHFET is given

in [9]. Fig. 3 shows nearly equal measured s-parameters in mode II and III, resp. According to the intrinsic drain source voltages of the first and the second FET (V_{D1S}, V_{DD1} > 1V), the presence of impact ionization becomes obvious in terms of $\underline{S}_{22}$ and $\underline{S}_{21}$, as described before. In contrast, for mode I the behaviour of $\underline{S}_{22}$ and $\underline{S}_{21}$ completely differ from that shown in mode II and III because the intrinsic drain source voltage (V_{D1S} < 1V) and consequently the intrinsic electric field between gate and the drain of the rf-driven first FET is too low to generate impact ionization in the channel.
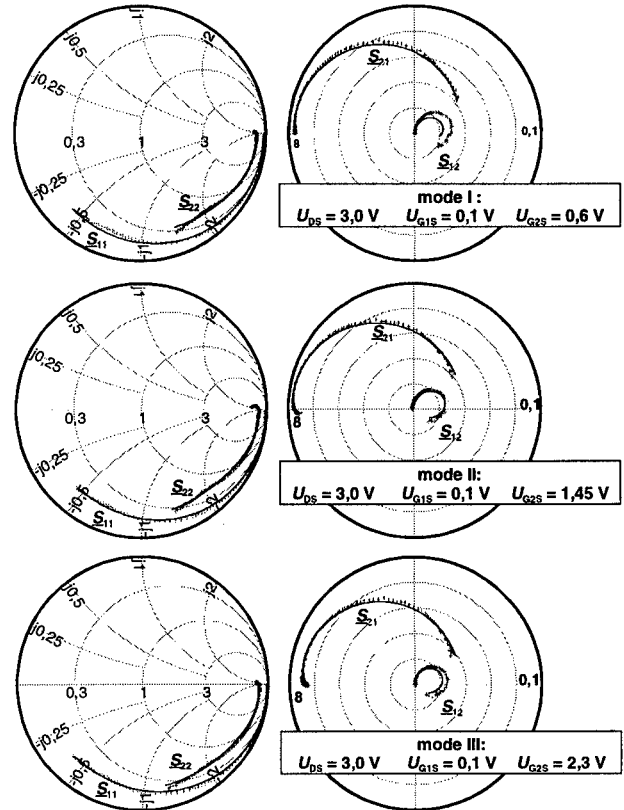
Fig. 3. Measured (+) and modelled (-) s-parameters of the DGHFET driven in mode I, II and mode III

These results were verified by calculation of the small-signal elements using an extended equivalent circuit of the DGHFET-cascode including the extension of impact ionization in case of both, the first and the second FET. As far as impact ionization is concerned table 1 shows the related transconductance $g_{m,impact1,2}$. According to an increase of the intrinsic drain source voltage of the first FET (V_{D1S}) which simultaneously is correlated to a decrease of that of the second FET (V_{DD1}) an increase in the value of the corresponding transconductance $g_{m,im1}$ combined with a decrease of its counterpart $g_{m,im2}$ can be observed. Consequently, an increased $g_{m,im2}$, indicating the presence of impact ionization in the second part of the device, does not affect the high frequency performance of the rf-driven first FET of the cascode. Consequently, from the first point of view, the rf-measurements correlate with the DC-results.

III. Noise Measurements

Over the last years research in DGHFET based on GaAs-substrate exhibit good results as far as noise behaviour up to 18GHz is concerned. Excellent minimum noise figures at 10GHz in terms of F_{min} <1dB have been reported recently [10]. In the InAlAs/InGaAs/InP system it is shown that impact ionization in the channel combined with high gate leakage current significantly disturbed the noise behaviour in this frequency range [9]. After R. Reuter [9] a high equivalent noise resistances R_{aq} combined with an increase of F_{min} at frequencies below 10GHz is highly significant for the presence of impact ionization in the device. Consequently, with regard to the results of the DGHFET's described above an improvement of the noise behaviour is expected when controlling the impact ionization in the channel underneath the rf-driven gate. For verification room temperature noise measurements were carried out in the range of 2-18GHz refering to mode I and III in case of the DGHFET-cascode. The minimum noise figures F_{min} and the corresponding equivalent noise resistance R_{eq} are shown in fig. 4.
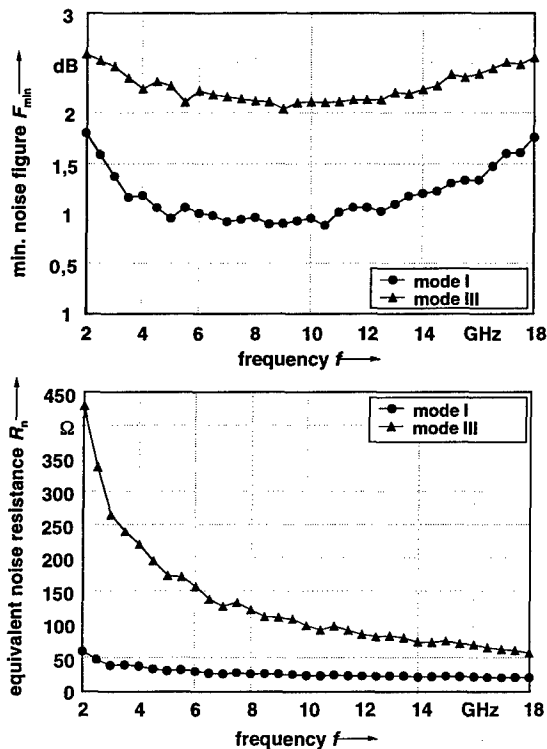
Fig. 4. *Minimum noise figure F_{min} and equivalent noise restistance R_n measured in mode I (•) and III (▲)*

In mode I -representing a bias condition with suppressed impact ionization in the channel underneath th rf-driven gate- excellent data ($F_{min}\leq$1dB, R_n=50Ohm) at 10GHz were achieved. In contrast in mode III -representing a bias condtion significantly suffered from impact ionization- an impressive increase of both, F_{min} and R_n, is observed. Consequently, these results verifies the predicted behaviour.

IV. Summary

Regardless the conventional advantages (higher MSG, higher f_{max}) of dual-gate HFET-cascodes in comparison to its single-gate counterpart new properties of the threeport device in the InAlAs/InGaAs/InP-system have been presented by extended dc- and rf-analysis. The influence of the second gate via V_{G2S} on the impact ionization effect has been clearly demonstrated. Optimum extrinsic bias conditions offer the possibility to shift impact ionization from the first intrinsic, rf-driven FET$_1$ to the second FET$_2$. S-parameter measurements underline that at this bias condition impact ionization does not affect the high frequency behaviour of the whole device. Thus a drastic improvement of the noise behaviour has been demonstrated. In conclusion, the DGHFET-cascode on InP -under the bias condition V_{G2S}=0V- instead of its SGHFET-counterpart will be a promising candidate for low noise amplifiers, e.g. in optoelectronic receivers.

V. Acknowledgements

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Novel InAlAs/InGaAs Heterojunction FETs with Modulated Indium Composition Channel and AlAs/InAs Superlattice Barrier Layer

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Abstract

Novel InAlAs/InGaAs heterojunction FETs (HJFETs) with modulated indium composition channels, named CCMTs (Channel Composition Modulated Transistors), have been successfully fabricated, in which an InAs channel is sandwiched by $In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As$ sub-channels. The channel structure is designed to improve electron transport and electron confinement by increase effective indium content in consideration of channel electron distribution. The fabricated devices also employ an AlAs/InAs superlattice as a barrier layer against impurity contamination for high thermal stability. A 0.2μm T-shaped gate device exhibits gm of 1370mS/mm, and Ft of 180GHz at a low drain bias of 1.0V. In high temperature and DC life test conducted at more than 230°C, the devices exhibited less than 3% degradation after 100hrs, which shows the developed CCMTs with AlAs/InAs superlattice insertion technology can offer high-performance and highly-reliable InP-based HJFETs for various microwave and millimeter-wave applications.

I. Introduction

Several papers reporting the excellent potential of InAs channel HEMTs on InP substrates as high frequency devices have been published with the intention to utilize its superior electron transport property[1-2]. However, in the channel structure designs, consideration of effective electron distribution in the strained channel has not been applied sufficiently. Taking into account of critical thickness of indium-rich strain channels on an InP substrate, simply inserting a thin InAs layer into an $In_{0.53}Ga_{0.47}As$ channel is insufficient to obtain a large sheet carrier density and good carrier confinement. In this paper, a novel device, the channel composition modulated transistor (CCMT) is presented, which is designed for a high sheet carrier density and for a majority of the transport in high indium content layers over a rather wide gate bias operation range by inserting an InAs main channel with thin sub-channel InGaAs layers having step indium composition.

In addition, the fabricated CCMT also employs AlAs/InAs superlattice insertion technology [3] in order to secure high device reliability. The superlattice inserted structure is designed to improve the thermal stability of InP-based HJFETs, which is closely related to Si donor inactivation caused by fluorine contamination in an n-type InAlAs layer [4]. By employing an AlAs/InAs superlattice

as a barrier layer under the gate, thermal stability of InAlAs/InGaAs HJFETs has been dramatically improved because the superlattice is an effective barrier against thermal diffusion of fluorine [3]. The AlAs/InAs superlattice is the most simple way to realize the same composition as ternary alloy InAlAs with a binary material system.

As the result of introducing the channel indium composition modulation technology and AlAs/InAs superlattice insertion technology, the CCMT is expected to demonstrate great device performance along with excellent device stability comparing to conventional InAlAs/InGaAs HJFETs in high temperature DC life tests.

II. Device Design

Using one-dimensional simulation solving Schrödinger's equation with Poisson's equation self-consistently, the InAs main channel layer is designed to be sandwiched by $In_{0.8}Ga_{0.2}As$ and $In_{0.53}Ga_{0.47}As$ sub-channel layers for large sheet carrier density, high carrier confinement and high electron transport. In Fig.1, an example of the calculation of a conduction band and the ground, first and second excited states of the CCMT structure are shown with a conventional lattice-matched channel structure having the same thickness

Fig.1 Conduction band energy and electron levels of (a)conventional device and (b)CCMT. ϕ_B -Vth is 0.5V in both figures. Ground state in conventional device is -0.13eV, and it in CCMT is -0.19eV.

channel. For simplicity, the AlAs/InAs superlattice layer is not taken into consideration in this simulation, however, it has been confirmed that the superlattice does not effect the results. In the calculated CCMT, the channel consists of 1nm-In$_{0.53}$Ga$_{0.47}$As, 2nm-In$_{0.8}$Ga$_{0.2}$As, 4nm-InAs, 4nm-In$_{0.8}$Ga$_{0.2}$As and 4nm-In$_{0.53}$Ga$_{0.47}$As. A planar doping concentration of 5×10^{12}cm^{-2} is adopted in both of the devices. The ground state in the conventional device is observed at -0.13eV; whereas in the CCMT it is at -0.19eV, which is lower than the conventional by 0.06eV. As the result of the ground state lowering, a larger sheet carrier density can be obtained in the CCMT structure. Figures 2(a) and (b) show the calculated electron distributions in the conventional channel and our modulated composition channel at various gate voltage. The peak position of the electron distribution on the conventional channel shifts gradually deeper by more than 5nm in the channel with a gate bias of 0V to -1.4V. On the other hand, with the same gate bias range, the center of the distribution on the CCMT shifts less than 1nm in the InAs well of the channel. Furthermore, more than 60% of channel electrons accumulate in the InAs main channel over this wide Vg range. The contribution of this excellent electron confinement property and the large sheet carrier density enable an improvement of the aspect ratio between the gate length and the gate-to-channel distance. Therefor the CCMT is also expected to be an effective device in a view of suppressing short channel effect even in fine gate devices.

III. Device Fabrication and Characteristics

The device structure is shown in Fig.3. The channel structure is the same as the CCMT structure discussed in Section II. The processed wafer was grown by MBE.

Fig.2 Channel Electron Distribution calculated in (a) Conventional FET and (b) CCMT. More than 60% of electrons accumulate in the InAs layer in CCMT. While the shift of the electron distribution peak with gate voltage is 5nm in the conventional FET, the shift in CCMT is less than 1nm.
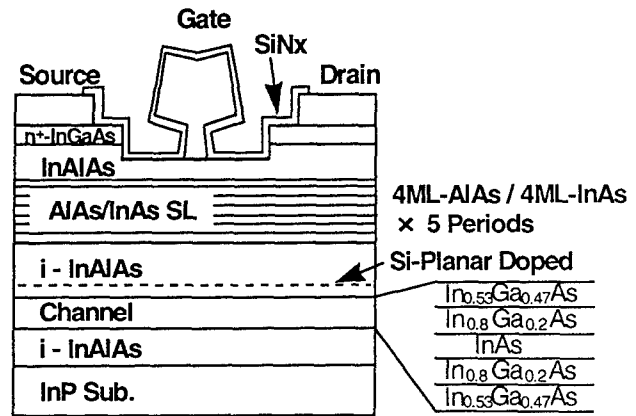
Fig.3 Schematic view of fabricated CCMT. The channel consists of 1nm-In$_{0.53}$Ga$_{0.47}$As, 2nm-In$_{0.8}$Ga$_{0.2}$As, 4nm-InAs, 4nm-In$_{0.8}$Ga$_{0.2}$As and 4nm-In$_{0.53}$Ga$_{0.47}$As. 5 periods of 4ML-AlAs/4ML-InAs superlattice layer are inserted as impurity barrier layer. The gate and the ohmics are composed of Mo/Ti/Pt/Au.

186
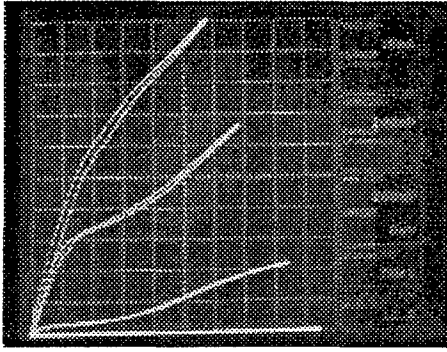
Fig.4 DC characteristics of 0.2µm T-shaped gate CCMT. Vd : 200mV/div, Id ; 10mA/div. The top curve corresponds to Vg=0V and Vg step is -0.2V. The source resistance is 0.38 Ω mm. The gate-to-drain breakdown voltage is more than 5V.
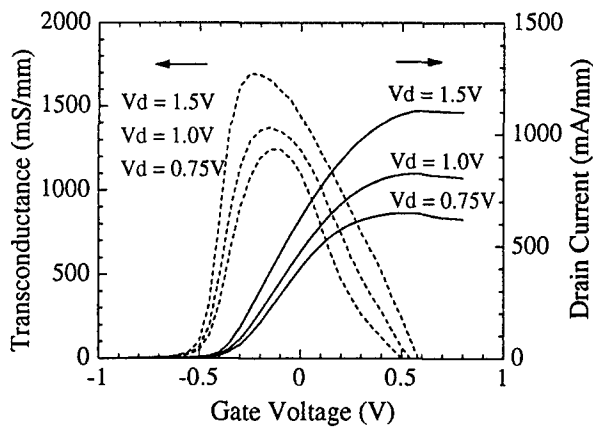
Fig.5 Bias dependence of drain current and gm. gm of 1370mS/mm at Vd=1.0V and 1690mS/mm at Vd=1.5V are measured.
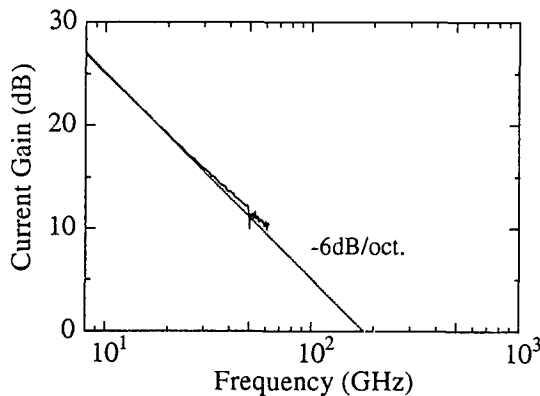
Fig.6 Frequency dependence of current gain calculated from S-parameters between 0.5-62.5GHz. Ft of 180GHz at Vd=1.0V is obtained with 0.2µm T-shaped gate CCMT.

The wafer also includes of an superlattice layer composed of 5 period superlattice of 4ML-AlAs/4ML-InAs inserted between the undoped InAlAs Schottky layer and the InAlAs donor layer in order to obtain high thermal stability. Due to the superior electron transport property in the indium composition modulated channel, an electron mobility of 18,300cm^2/Vs has been measured at room temperature [5]. In the device fabrication process, for the purpose of suppressing interdiffusion between the electrode metals and the semiconductors, Mo/Ti/Pt/Au was employed for both gate and non-alloyed ohmic metallization [6]. The gates were defined by electron beam lithography and lift-off techniques. All the devices have been passivated by plasma-CVD-SiN film for surface stabilization and as a guard film for the n-InAlAs donor layer against fluorine contamination [7].

The DC characteristics and bias dependence of transconductance of the fabricated device are shown in Figs.4 and 5, which shows no degradation of device performance due to inserting the AlAs/InAs superlattice. The 0.2µm T-shaped gate CCMT exhibited gm of 1370mS/mm at a low drain bias of 1.0V and 1690mS/mm at 1.5V. The threshold voltage is -0.45V, and the gate-to-drain breakdown voltage is more than 5V. The S-parameters of the device were measured from 0.5 to 62.5GHz. The current gain h_{21} as a function of frequency was extracted from the S-parameters and -6dB/octave gain roll-off was obtained. Extrapolating the data, as shown in Fig.6, a unity current gain cut-off frequency of 180GHz was obtained. This is a highest value reported to date with greater than 0.2µm gate length.

IV. Device Reliability

The device stability of the CCMTs has been examined through high temperature life test at 250°C, and high temperature DC life test at the set condition of 230°C, Vd=0.75V and Id=200mA/mm. The changes of saturation drain current and maximum transconductance as a function of duration of each stress condition are shown in Figs.7(a) and (b). The parameters are measured at a drain bias of 1.0V. No drastic changes were observed in both of the life tests. The degradation of Idss and gm are restricted to less than 3% and 8% in high temperature test and to less than 1% and 3% in high temperature DC life test, after 100hrs. This excellent reliability is due to the high stability of molybdenum based electrode technology, which restricted interdiffusion between electrode metals and semiconductors, and AlAs/InAs superlattice technology to protect the InAlAs donor layer from fluorine contamination, which inactivates Si donors in an n-InAlAs layer.
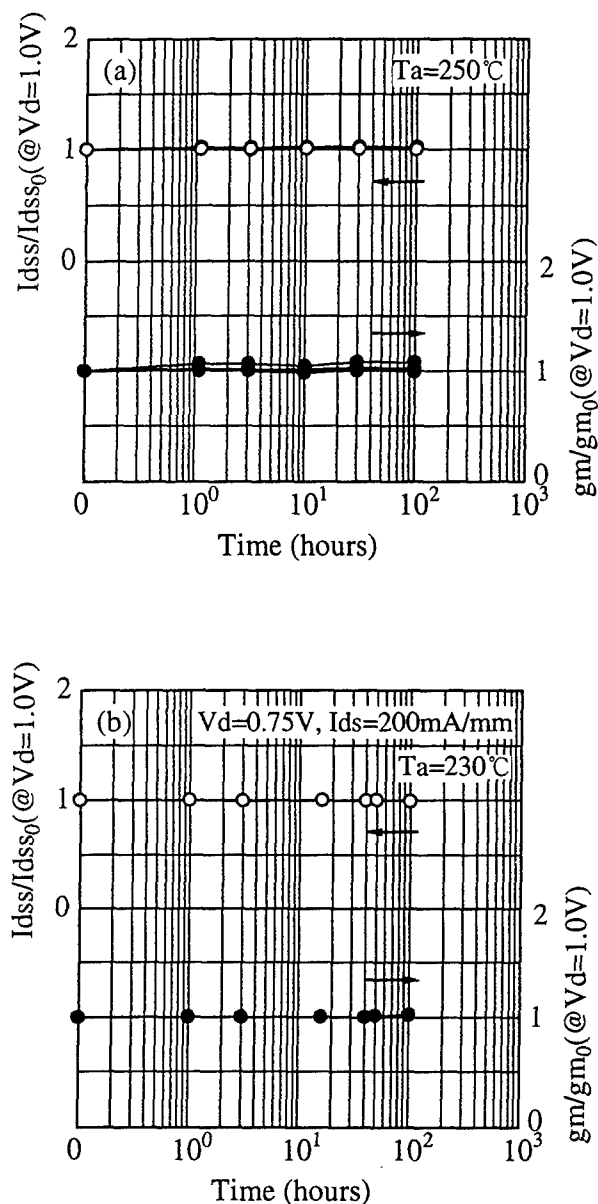
Fig.7 Results of (a)high temperature test and (b)high temperature DC life test. Open circles correspond to drain current and closed circles correspond to transconductance.

V. Conclusion

In conclusion, high performance and high reliability InAlAs/InGaAs HJFETs, CCMTs, which comprise a modulated indium composition channel including an InAs layer and an AlAs/InAs superlattice layer inserted between Schottky and donor layers, have been successfully fabricated. The $0.2\mu m$ T-shaped gate CCMT showed gm of 1370mS/mm and Ft of 180GHz at a 1.0V drain bias. Its great thermal stability has been confirmed through high temperature tests and high temperature DC life tests. Its excellent device performance and high reliability are attributed to the introduction of channel composition modulation technology realizing a high effective indium channel and AlAs/InAs superlattice technology as an effective barrier against impurity contamination. The developed CCMT with AlAs/InAs superlattice insertion technology is promising as a key device for a number of millimeter-wave applications.

Acknowledgment

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FIRST DEMONSTRATION OF AlInAs/GaInAs HEMTs ON AlAsSb AND OXIDIZED AlAsSb BUFFERS

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Introduction

We report for the first time two new AlInAs/GaInAs HEMT device structures, one fabricated on thin AlAsSb buffer and the other on oxidized AlAsSb buffer. $AlAs_{0.56}Sb_{0.44}$ which is lattice matched to InP has a bandgap of 1.9 eV compared to 1.45 eV for AlInAs. This increases the barrier between the channel and the substrate reducing parasitic conduction through the buffer and improves the charge control properties. Also AlAsSb can be converted to Al_2O_3 by lateral oxidation in steam to obtain a truly insulating buffer. An AlInAs/GaInAs HEMT with AlAsSb buffer with Lg=1.5 μm has Ids=500 mA/mm and gm=810 mS/mm. AlInAs/GaInAs HEMTs with oxidized AlAsSb buffer has gm=190 mS/mm for Ids=130 mA/mm.

I. Oxide Based Electronics in AlInAs/GaInAs/InP material system

Oxidation of Al containing compounds like AlAs and AlGaAs has been extensively investigated for applications in GaAs based electronic and opto-electronic devices. GaAs on Insulator MESFETs and pHEMTs have been recently demonstrated [1,2]. An insulating buffer is desirable in III-V FET technology as it enables excellent charge control for sub-micron gate length devices and reduces the substrate leakage. This approach can be extended to the InP based material system by using oxidized AlAsSb. Steam oxidation of AlAsSb lattice matched to InP at 350 °C has been reported previously [3]. The differentiating aspect in this case from AlAs is the segregation of Sb into a semimetallic layer at the top oxide-semiconductor interface. This is undesirable as it prevents the oxide from being used as a insulating buffer. However we have observed that oxidation at higher temperatures (400 °C, 450 °C) reduces the amount of Sb in the oxide. This oxidation temperature is still low enough to prevent the oxidation of the AlInAs. Hence oxidized AlAsSb layer can be used as insulating buffers AlInAs/GaInAs HEMT structures. An insulating buffer for AlInAs/GaInAs HEMT enables the fabrication of low power, high speed transistors.

II. Device Structure

The layer structure is grown by solid source MBE and is shown in Fig.. 1. Compared to the conventional thick AlInAs buffers used for AlInAs/GaInAs HEMTs, a thin 500 Å AlAsSb buffer grown on a thin 200 Å AlInAs (T_{growth} =530 °C) layer is used here. The AlAsSb is growth temperature is 480 °C and the As_2 flux is 1×10^{-6} torr and the Sb_4 flux is 2×10^{-6} torr. The remaining layers are grown at 510 °C. To protect the GaInAs channel during a 100 Å AlInAs oxidation spacer layer is used between

Layer
150 Å n+ GaInAs n=1.2x10^{19} cap
150 Å n+ AlInAs n=1.2x10^{19} cap
175 Å i-AlInAs barrier
40 Å n+ AlInAs n=1.2x10^{19} donor layer
30 Å i-AlInAs spacer
400 Å i-InGaAs channel
100 Å i-AlInAs oxidation spacer
500 Å AlAsSb buffer
200 Å i-AlInAs buffer
S.I. InP substrate

Fig.1 Layer structure of AlInAs/GaInAs HEMT with AlAsSb buffer

the AlAsSb buffer and the GaInAs channel. A heavily doped n+InGaAs/n+ AlInAs cap is used to obtain a non-alloyed contact [4]. The sheet charge density of is

2.3 $\times 10^{12}$ /cm^2 and the mobility 12000 cm^2/Vs as obtained from Hall measurement. (The heavily doped cap layers are etched before the Hall measurement). Thus the introduction of the AlAsSb buffer does not degrade the material quality of the GaInAs channel in any manner.

III. Device Fabrication

Device fabrication begins with deposition of a protective SiO$_2$ cap layer over the entire wafer. Next Cl$_2$ based reactive ion etching is used to define the device mesa and expose the AlAsSb buffer layer for lateral oxidation. The SiO$_2$ acts a mask during reactive ion etching and also protects the underlying layers during the oxidation. The AlAsSb layer is laterally oxidized at different temperatures ranging from 350 °C to 450 °C for 30 minutes. The oxidation is done in a three zone furnace, the steam is introduced in the furnace by nitrogen bubbling through water kept at 90 °C. After the oxidation process the protective SiO$_2$ cap layer is removed and AuGe/Ni/Au metallization is deposited to form non-alloyed contact to the source and drain. The gate (Lg=1.5 μm) is defined by optical lithography, the n+ GaInAs/n+ AlInAs layers are etched using citric acid based etchant and Ti/Au gate metallization is deposited. Also HEMTs were fabricated with above process with as grown (unoxidized) AlAsSb buffers. The main advantage of using oxides as buffers in FETs is that no additional mask levels are required.

IV. AlInAs/GaInAs HEMT with AlAsSb Buffer

Figures 2 and 3 show the three terminal I-V characteristics and the transfer characteristics of the **AlAsSb buffer HEMT**. The I-V characteristics show a kink which is probably due to traps in the AlAsSb
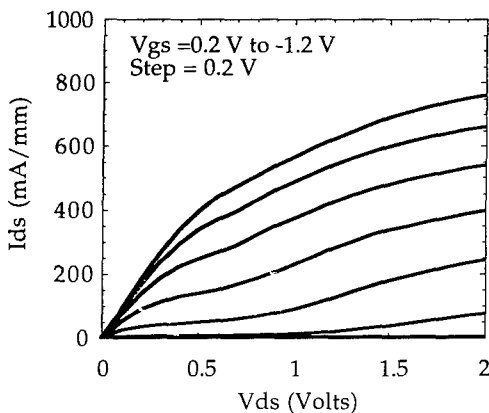
Fig. 2 Three terminal I-V characteristics of AlAsSb buffer HEMT.

buffer layer. The drain current is 500 mA/mm and the peak transconductance is 811 mS/mm at Vds=1.5 V,

Vgs= - 0.6 V. The high value of the transconductance indicates that the AlAsSb buffer improves the charge control and reduces the parasitic conduction through the buffer. The two terminal gate-drain breakdown voltage of the device is 6.5 Volts.
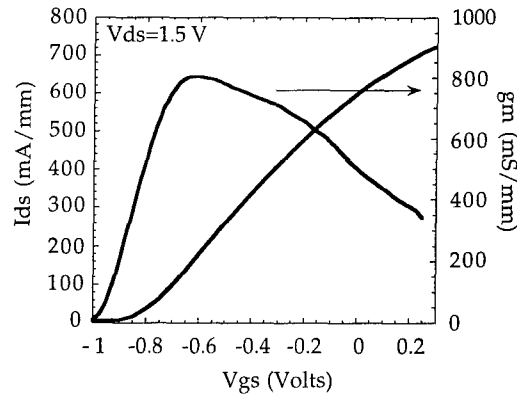
Fig. 3 Transfer Characteristics of AlAsSb Buffer HEMT

A short circuit current gain cutoff frequency f$_t$ of 22 GHz and a maximum frequency of oscillation f$_{max}$ of 60 GHz is obtained from S-parameter measurements as shown in Figure 4. These values are comparable to 1 μm AlInAs/GaInAs HEMTs.
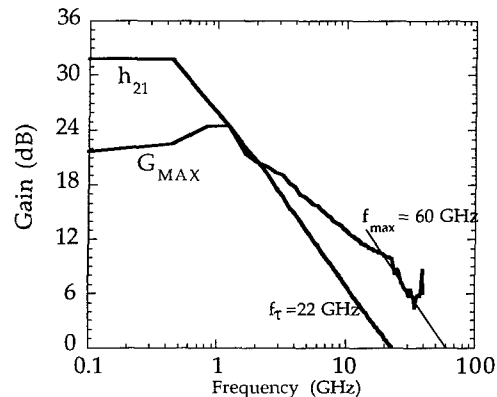
Fig. 4 High frequency performance of AlAsSb Buffer HEMT

V. AlInAs/GaInAs HEMT with oxidized AlAsSb buffer

As described before AlInAs/GaInAs HEMTs were fabricated with buffers oxidized at different temperatures ranging from 350 °C to 450 °C. There is a tradeoff involved in the selection of oxidation temperatures, lower oxidation temperatures minimize the electronic and structural damage to layers adjacent to the

oxidizing layers. However at lower temperatures Antimony accumulation occurs at the top oxide semiconductor interface. Devices with AlAsSb buffer oxidized at 350 °C show no saturation in drain current indicating that a low resistance leakage path from the source to the drain is created by the semimetallic Antimony layer at the GaInAs channel /AlAsSb oxide interface.

On the other hand when the AlAsSb buffer is oxidized at 450 °C the parasitic leakage path is seliminated enabling normal FET operation. A 1.5 μm gate length device has a peak gm of 176 mS/mm, however the current level in this device is 50 mA/mm. The reason for the low current level is depletion of charge in the channel due to two mechanisms. The first is structural degradation of the channel during the process of oxidation, the other is the depletion of channel charge by interface traps at the oxide semiconductor interface [5].

The degradation in current level is reduced if the oxidation temperature is reduced. When the AlAsSb buffer is oxidized at 400 °C, it is observed at the current level is increases to 130 mA/mm. Figures 5 and 6 show the three terminal I-V characteristics and the transfer characteristics of the **oxidized AlAsSb buffer** HEMT with the AlAsSb buffer oxidized at 400 °C. No kink effect is observed in the I-V characteristics.
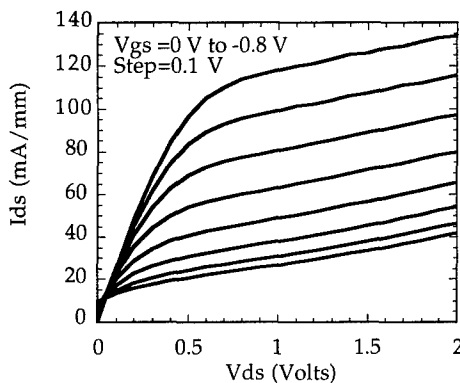
Fig. 5 Three terminal I-V characteristics of Al₂O₃ (oxidized AlAsSb) buffer HEMT

The peak transconductance is 190 mS/mm at Vds=1.5 V, Vgs= -0.2 V. The output conductance is 15 mS/mm. This particular device could not be pinch-off due to excessive gate leakage. The leakage current through oxidized AlAsSb is 2 pA/μm^2 (from measurements on MIS capacitors with ozidized AlAsSb dielectric) [6]. Though the substrate current is not directly measured, it is expected to be similar as above. Thus the possibility of leakage through the oxide buffer is eliminated here.

A short circuit current gain cutoff frequency f_τ of 6 GHz and a maximum frequency of oscillation f_{max} of 13 GHz was obtained S-parameter measurements as shown in Figure 7. The charge depletion due to oxidation

results in a high input resistance R_i. Thus the channel charging delay R_iC_{gs} is high and this reduces the f_τ of the device. This phenomenon has also been observed for GaAs on Insulator pHEMTs.
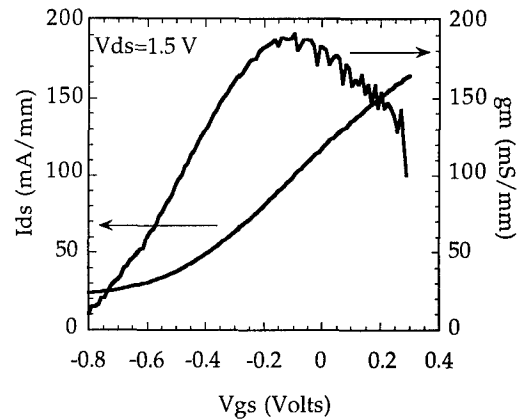
Fig. 6 Transfer characteristics of Al₂O₃ (oxidized AlAsSb) bufferHEMT
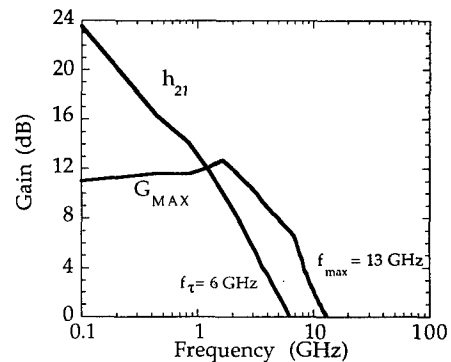
Fig. 7 High frequency performance of Al₂O₃ (oxidized AlAsSb) buffer HEMT

Since this is the first attempt to fabricate a device in the InP based material system using oxidized AlAsSb there is room for improvement. Further optimization of the device structure and the AlAsSb oxidation process will help in improving the device performance.

V. Conclusion

To summarize AlInAs/GaInAs HEMTs with an a thin AlAsSb buffer and oxidized AlAsSb buffer have been demonstrated for the first time. This technology enables the formation of an insulating buffers and interlayer dielectrics for the AlInAs/GaInAs/InP material system and has applications in low power complementary HFET technology.

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DC, SMALL-SIGNAL, AND NOISE CHARACTERISTICS OF 0.1 μm AlSb/InAs HEMTs

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Abstract

We report on the dc and small-signal characteristics of 0.1 μm AlSb/InAs HEMTs. These recessed-gate devices have an $In_{0.4}Al_{0.6}As$/AlSb composite barrier above the InAs quantum well and a p^+ GaSb layer within the AlSb buffer layer. The devices exhibit a transconductance of 600 mS/mm and an f_T of 120 GHz at $V_{DS} = 0.6$ V. An intrinsic f_T of 150 GHz is obtained after removal of the gate bonding pad capacitance. 0.5 μm HEMTs on the same wafer exhibit a transconductance of 1 S/mm and an intrinsic $f_T L_g$ product of 50 GHz-μm. At 4 GHz, the 0.1 μm HEMTs have a minimum noise figure of 1 dB with 14 dB associated gain at $V_{DS} = 0.4$ V.

I. Introduction

AlSb/InAs-based HEMTs have potential for low-voltage, high-speed applications due to attractive material properties of this heterojunction system. Compared to $In_xGa_{1-x}As$ channel HEMTs, the smaller electron effective mass in the InAs channel results in higher electron mobilities. Due to the larger Γ-L valley separation, InAs also has the advantage of a higher electron peak velocity(4×10^7 cm/sec)[1]. The considerably larger conduction band discontinuity (1.35 eV) of the AlSb/InAs heterojunction enables the formation of a deeper quantum well and the associated benefits of a larger 2-DEG sheet charge density, superior carrier confinement, and improved modulation efficiency. The higher electron mobility and velocity, lower threshold field, and reduced access resistance also enable the attainment of higher effective velocity at a lower drain voltage. However, impact ionization in the InAs channel is higher than in InGaAs due to its narrow bandgap of 0.36 eV at room temperature. The extent to which the higher impact ionization deleteriously affects performance is currently under study.

Although significant progress has been reported since the devices were first proposed[2], further improvements in the material growth, design, and fabrication technology are necessary to understand and fully realize their performance potential. In this paper, we report on the improved mm-wave performance obtained from the first AlSb/InAs-based HEMTs fabricated with a 0.1 μm gate length. It is also the first report on the microwave noise performance for a HEMT in this material system.

II. Material Growth

The AlSb/InAs HEMT material was grown by solid-source MBE on a semi-insulating (100) GaAs substrate. A 0.5 μm buffer layer of GaAs was grown first, followed by 2.4 μm of AlSb. A 200Å Si-doped GaSb layer ($p \sim 6 \times 10^{17} cm^{-3}$) was grown next, followed by a 500Å undoped AlSb layer, a 100Å undoped InAs channel layer, a 125Å undoped AlSb layer, a 40Å undoped $In_{0.4}Al_{0.6}As$ layer, and finally a 15Å undoped InAs cap layer. The 2.4 μm AlSb buffer layer was used to accommodate the 7% lattice mismatch between HEMT material and the GaAs substrate. Modulation doping of the InAs quantum well was obtained through the use of an As soak technique which was performed between the growth of the AlSb and InAlAs barrier layers. The sheet carrier density and mobility of the starting material, determined by Hall measurements at 300K, were 1.5×10^{12} cm^{-2} and 16,600 cm^2/V-s, respectively.

III. HEMT Design and Fabrication

Two key features of the HEMT design are the use of an $In_{0.4}Al_{0.6}As$/AlSb composite barrier above the InAs quantum well and a 200Å p^+ GaSb layer located within the AlSb buffer layer. The addition of the InAlAs layer enhances the insulating property of the barrier, improves

chemical stability, and enables a gate recess process to be employed. The p^+ GaSb layer in the buffer is intended to drain a portion of the impact-ionization-generated holes back to the source contact rather then allowing them to remain in the AlSb buffer layer where they are likely to cause deleterious trapping effects[3].

A Pd/Pt/Au ohmic contact metalization scheme was used which was developed to achieve low access resistance in AlSb/InAs-based HEMTs[4]. After definition and heat treatment of the source and drain ohmic contacts, a Cr/Au Schottky-gate metalization was formed using a PMMA-based tri-level resist e-beam lithography and lift-off procedure. A citric acid-based recess etch through the cap layer was performed prior to gate metal deposition. Device isolation was then achieved by wet chemical etching. As a result of this etch, a gate air bridge was formed which extends from the channel to the gate bonding pad.

IV. DC Characterization

The dc characteristics of HEMTs with gate lengths from 0.1 to 0.5 μm were evaluated. The drain characteristics of a 0.1 μm HEMT are shown in Fig. 1. The transconductance at $V_{DS} = 0.6$ V and $V_{GS} = -0.3$ V is 600 mS/mm. The HEMTs exhibit an increase in the output conductance at a drain voltage above 0.5 V due to the effects of impact ionization in the channel.

The drain characteristics of a HEMT with a 0.5 μm gate length are shown in Fig. 2. The low- field source-drain resistance is 0.9 Ω-mm at $V_{GS} = 0.1$ V. The HEMTs display negligible kink effect and a maximum transconductance of 1 S/mm at $V_{DS} = 1$ V. The 0.5 μm HEMTs
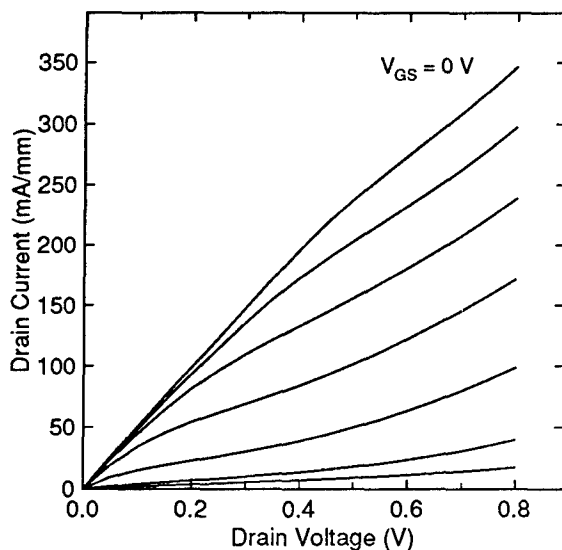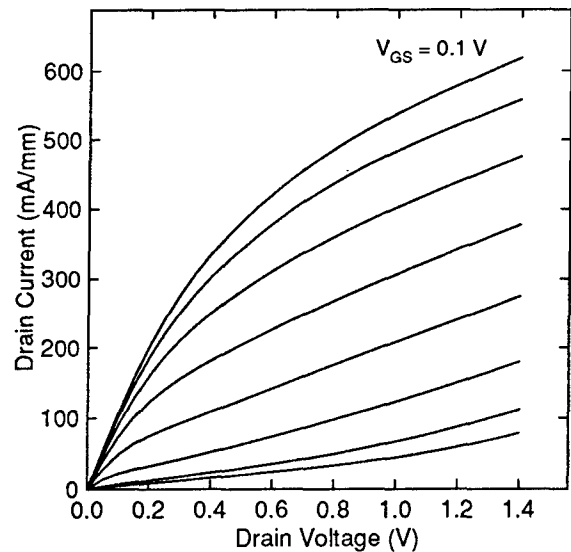
Fig. 2. 0.5 μm HEMT drain characteristics.
$L_{SD} = 1.3$ μm, $W_G = 25$ μm, $V_{GS} = 0.1$ V/step.

exhibit more saturation in the drain current presumably due to the larger gate length/gate-channel separation aspect ratio and the lower electric field strength under the gate which reduces the effects of impact ionization. The lack of drain current pinchoff in the HEMTs is apparently due to hole current in the p^+ GaSb layer in the buffer. HEMTs fabricated using a similar design but without the p^+ GaSb layer exhibited more complete pinchoff.

AlSb/InAs HEMTs are susceptible to high gate leakage current due to the staggered type-II heterojunction band lineup. Despite the large electron barrier height (> 1 eV) between the gate metal and the channel, relatively high gate leakage currents are typically observed due to the substantial hole transport which can occur across the small valence band barrier between the gate and the channel. The problem is exacerbated by the increased number of holes which are present in the channel due to impact ionization. With the addition of the InAlAs/AlSb barrier layer, the gate current was found to be reduced by an order of magnitude compared to our previous results[5]. When biased for maximum f_T, a gate leakage current of 14 μA was measured for a 0.1 μm x 150 μm gate.

Most AlSb/InAs-based HEMTs reported thus far suffer from an anomalous increase in the dc output conductance of the drain characteristics as the drain voltage is increased. This "kink effect" causes degraded performance at nominal bias values and precludes the use of the devices at fields where optimum performance could be expected. Based on measurements made on a variety of different HEMT designs at our laboratory and elsewhere, the kink in the drain characteristics is

Fig. 1. 0.1 μm HEMT drain characteristics.
$L_{SD} = 2.3$ μm, $W_G = 28$ μm, $V_{GS} = 0.1$ V/step.

believed to be caused by the trapping of holes generated by impact ionization in the channel[6,7]. Despite the high field present under the gate, the drain characteristics of the 0.1 μm HEMTs do not display the kink which was previously observed in our HEMTs with gate lengths below 0.2 μm[7]. This may be explained by the reduction of hole trapping near the gate metal-semiconductor interface region due to the use of a gate recess etch in these devices. HEMTs on this wafer which did not receive a gate recess etch prior to gate metal deposition exhibited a kink in the drain characteristics.

V. Microwave Characterization

The S-parameters of the HEMTs were measured from 1 to 40 GHz. The 0.1 μm devices exhibit an f_T of 120 GHz and an f_{max} of 80 GHz at a drain voltage of 0.6 V. A plot of $|h_{21}|$ as a function of frequency is shown in Fig. 3. Equivalent circuit models of the devices were developed by fitting the S-parameters over the measured frequencies. S-parameter measurements on gate-less HEMTs of the same geometry were utilized to model the external parasitics.

In order to examine the inherent device speed, the bonding pad capacitance of the gate was subtracted in the equivalent circuit. The results indicated an intrinsic f_T of 150 GHz for the 0.1 μm device. The 0.5 μm HEMTs exhibited an intrinsic $f_T L_g$ product of 50 GHz-μm, which is comparable to the highest previously reported for a FET in this gate length region. Improvement of the $f_T L_g$ product in the deep submicron regime should be achievable with improved HEMT channel designs and higher sheet charge density.
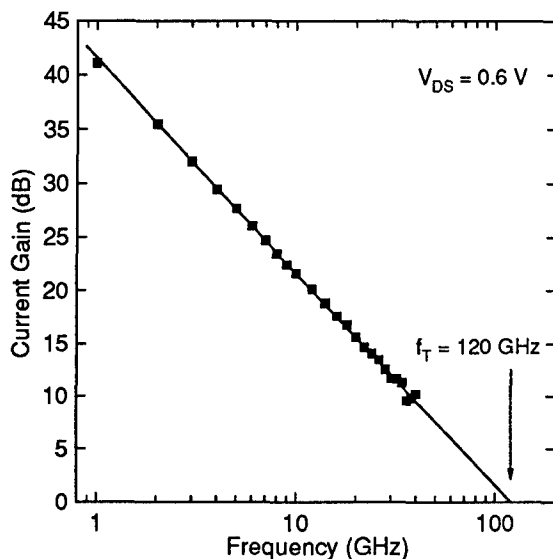
Fig. 3. Extrinsic current gain, $|h_{21}|$, versus frequency.
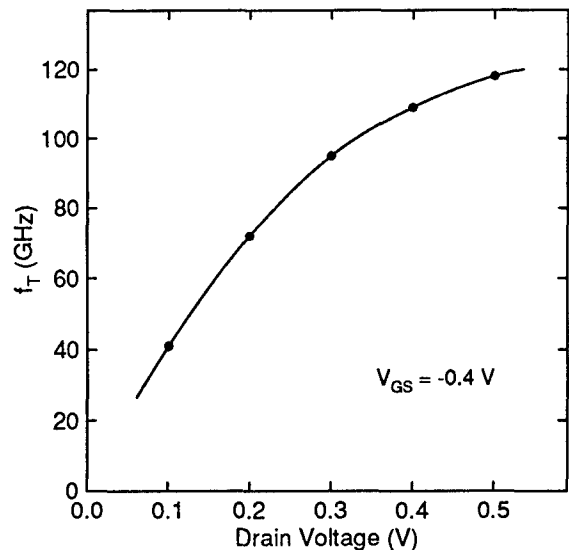
Fig. 4. Extrinsic current gain cutoff frequency, f_T, versus drain voltage.

The f_{max} of the 0.1 μm HEMTs is primarily limited by the relatively high output conductance of 150 mS/mm. The removal of the p$^+$ GaSb layer from the model increased the f_{max} to 90 GHz. Future design iterations will determine how the dc and mm-wave performance are affected by a reduction in the p$^+$ GaSb layer thickness and carrier density. Below the region of impact ionization, only minimal g_m and g_{ds} dispersion are observed between dc and 1 GHz. The devices typically exhibited a maximum g_m/g_{ds} ratio of 4.

Additional study is needed to determine to what extent the output conductance can be decreased and the f_{max}/f_T ratio improved using advanced channel designs which reduce short channel effects and impact ionization in the channel. The highest f_{max} observed was 110 GHz which was measured on a 0.4 μm gate length HEMT which exhibited an output conductance of 100 mS/mm and a g_m/g_{ds} ratio of 7.

The potential for low voltage operation is shown in Fig. 4, which shows the extrinsic f_T as a function of drain voltage for the 0.1 μm HEMT described above. At a drain voltage of 0.2 V, an f_T of 72 GHz was obtained. Additional measurements on 0.15 μm HEMTs with lower access resistance have exhibited extrinsic f_T's of 100 GHz and 130 GHz at a drain voltage of 0.2 V and 0.3 V, respectively.

VI. Microwave Noise Measurements

The AlSb/InAs HEMT has potential advantages compared to GaAs- and InP-based HEMTs for achieving lower noise figure and higher associated gain due to better material properties. Moreover, a low noise figure should be obtainable at a drain voltage of 0.5 V or lower.

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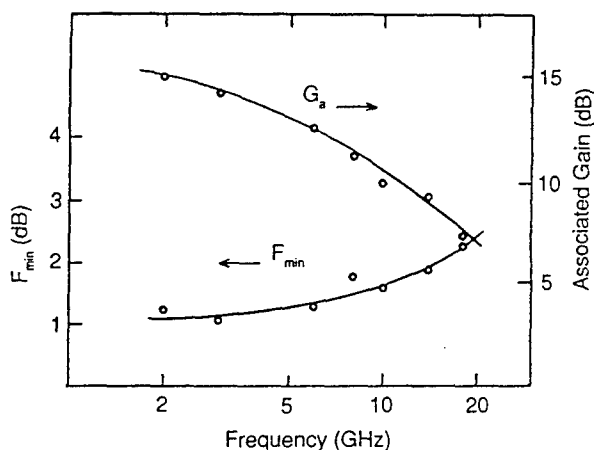
Fig. 5. F_{min} and associated gain as a function of frequency. $V_{GS}= -0.4$ V, $L_G= 0.1$ μm, $W_G= 150$ μm.

The minimum noise figure, F_{min}, and the associated gain, G_a, for a 0.1 μm AlSb/InAs HEMT are shown as a function of frequency in Fig. 5. These measurements were made on-wafer with mechanical tuners. The value of V_{DS} applied to get the performance shown was adjusted from 0.35 V at 2 GHz to 0.55 V at 18 GHz. V_{GS} was picked for the best value of F_{min} and remained constant over the frequency range.

It should be noted that the F_{min} and G_a values are achieved at low drain voltages. This is a direct result of the high mobility and velocity in this material system. To examine this property more closely, the values of F_{min} and G_a are shown in Fig. 6 as functions of V_{DS} at 4 GHz. This figure clearly shows the potential for low-voltage operation of the AlSb/InAs HEMTs.

It is important to realize that these devices were not designed specifically for low-noise performance. Consequently, considerable improvements are expected from a more optimal design involving higher sheet charge density, more suitable horizontal dimensions, es-

pecially smaller bonding pads, and further improved barrier layer design resulting in lower gate current. To obtain a quantitative measure of expected improvements, a noise equivalent circuit was used to examine the performance potential of AlSb/InAs HEMTs. The results indicate that noise figures of 0.3 and 0.6 dB are feasible at 4 and 10 GHz, respectively, at $V_{DS}=0.5$ V. These values are obtained without assuming any increase in the basic speed of the device. Although the effect of impact ionization on the noise performance needs to be further examined, these results indicate that AlSb/InAs-based HEMTs have significant potential for low-voltage, low-noise operation.
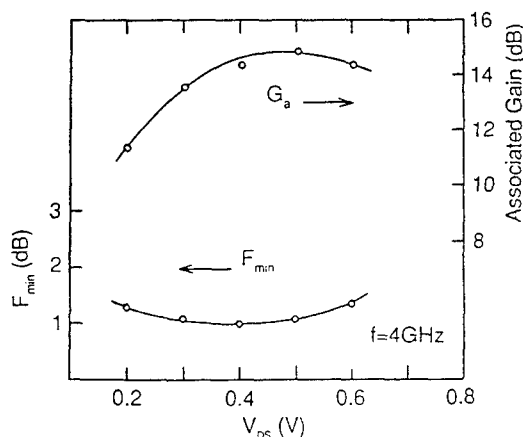
VII. Acknowledgment

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Fig. 6. F_{min} and G_a as a function of V_{DS} at 4 GHz.

Temperature Dependence of Breakdown Voltage in InAlAs/InGaAs HEMTs: Theory and Experiments

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Abstract

We present results of an experimental and theoretical study of the temperature dependence of the off-state breakdown voltage of InAlAs/InGaAs high electron mobility transistors (HEMTs). We find that the breakdown voltage (BV) has a negative temperature coefficient that is more prominent for lower values of the extrinsic sheet carrier concentration (n_s). Structural parameters such as the insulator thickness and top-to-bottom delta doping ratio have little effect on BV if n_s is held constant. These results are consistent with an extension of a new tunneling model for breakdown in HEMTs to include thermionic-field emission.

I. Introduction

InAlAs/InGaAs high electron mobility transistors (HEMTs) show promise for millimeter wave power applications. Recent years have seen significant improvements in the off-state breakdown voltage (BV), a key parameter for power (1-6). However, this work has been mainly empirical due to the lack of a predictive model. This has hindered first-pass design success.

Conventional understanding has held impact ionization or a combination of tunneling and impact ionization as the dominant mechanism for HEMT breakdown (7,8). Recently however, based on mounting experimental evidence suggesting that breakdown in HEMTs is largely determined by tunneling and/or thermionic-field emission, a 0 K predictive model for tunneling-limited breakdown was presented (9). The model, however, is incomplete without including a mechanism describing the temperature dependence of breakdown. An understanding of the temperature dependence of breakdown is important in itself since power HEMTs must operate at a wide range of temperatures. To address this, we have carried out careful temperature-dependent BV measurements on several state-of-the-art InAlAs/InGaAs HEMTs with well controlled values of sheet carrier concentration in the channel. Our work shows that an extension of the tunneling-limited breakdown model to finite temperatures successfully predicts all the experimental results.

II. Experimental

The devices used in this work are 0.1 µm T-gate double heterostructure InP HEMTs with a thin undoped cap fabricated by Lockheed Martin (Fig. 1). Several heterostructures with different insulator thicknesses, total doping levels and top to bottom delta doping ratios were grown. These design variations yielded wafers with sheet carrier concentrations from 2.82×10^{12} cm^{-2} to 3.66×10^{12} cm^{-2}. The fabrication process features a selective gate recess (10), allowing precise control of V_T and the value of the sheet carrier concentration in the extrinsic regions, $n_{s(extrinsic)}$.
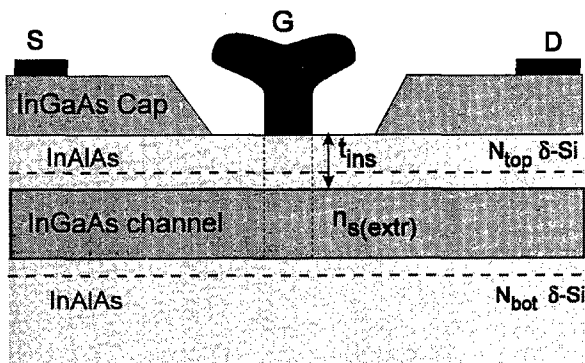
Figure 1: Cross section of the HEMTs under study.
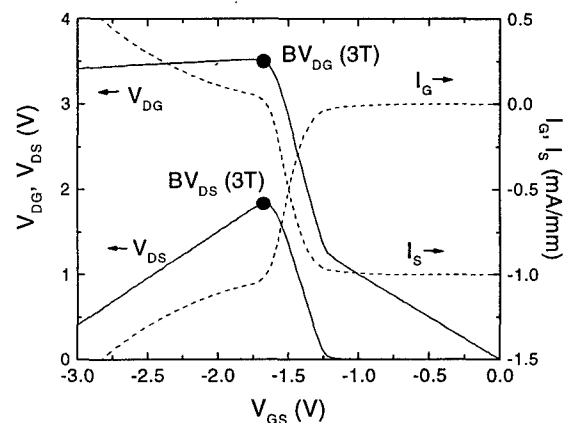
Figure 2: The drain current injection (3-terminal) breakdown voltage measurement for one of the devices under study. 1 mA/mm is injected into the drain and V_{GS} is swept from on-state to off-state.
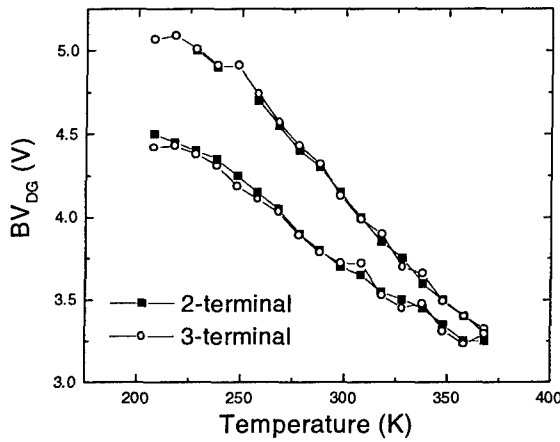
Figure 3: Temperature dependent breakdown voltage measurements for two representative devices using both a two-terminal and a three-terminal technique. Both techniques yield the same BV indicating breakdown is a gate-drain phenomenon.

Figure 4: Plot of BV_{DG} vs. $n_{s(extrinsic)}$ for all wafers under study. Each data point and error bar represent data from several devices on each wafer.

To establish the breakdown path, we began our analysis by looking at 2- and 3-terminal measurements of the breakdown voltage (7). The 2-terminal technique involves only the standard reverse gate diode characteristics. BV_{DG} is extracted where the gate current reaches 1 mA/mm with the source left floating.

For a more complete investigation of the breakdown of the device, we used the 3-terminal drain current injection technique (7). In this measurement, a 1 mA/mm current is injected into to the drain with the source grounded and the gate voltage is swept from the on-state through threshold into the off-state. The results of this technique on a typical device at room temperature are plotted in Fig. 2. BV_{DG} is extracted at the point where I_S goes to 0, and BV_{DS} is defined as the peak in the V_{DS} curve. V_{DG} remains fairly constant once it reaches BV_{DG}. This is an indication that the breakdown we are observing takes place in the drain-gate diode and channel breakdown is not coming into play. This hypothesis is further supported by the comparison of 2-terminal and 3-terminal measurements in Fig. 3. BV(2T) tracks BV(3T) almost exactly for the entire temperature range studied. Armed with this evidence and the fact that the currents are very well behaved, we conclude that the breakdown path is in fact between the gate and the drain and that the 2-terminal measurement is sufficient to evaluate it.

Fig. 4 shows 2-terminal measurements of BV_{DG} for a large number of room temperature measurements on each of the wafers under study. Each point represents the average of the measurements and the error bars indicate the standard deviation. BV exhibits a clear dependence on $n_{s(extrinsic)}$: higher values of $n_{s(extrinsic)}$ result in lower breakdown voltages. It does not, however, show significant correlation with most parameters, such as the insulator thickness and the delta doping ratio.
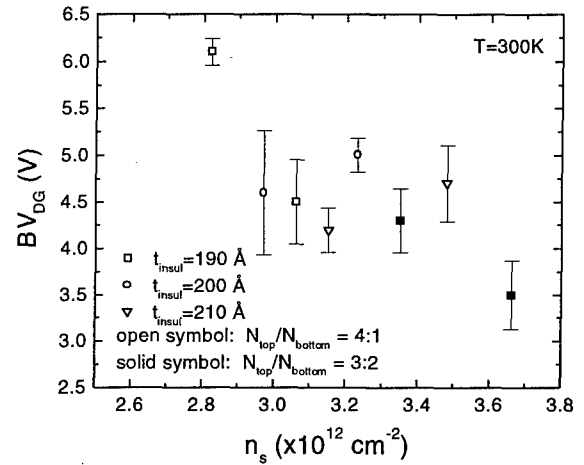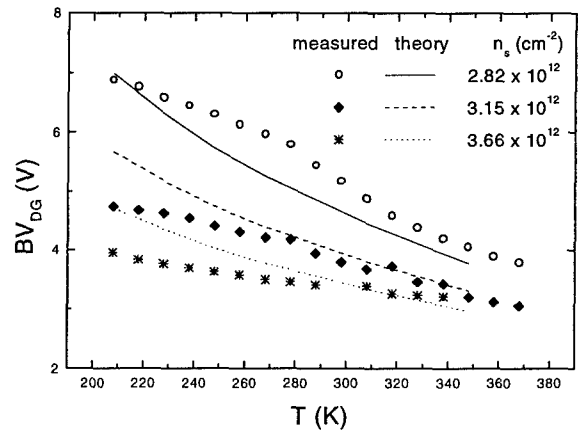
Figure 5: Experimental and theoretical temperature dependence of breakdown voltage for different values of $n_{s(extrinsic)}$. Theory lines correspond to $\phi_B = 0.63\text{eV}$ and the measured $n_{s(extrinsic)}$.

In Fig. 5 we see BV results for three of the wafers in the sample set as a function of temperature. We observe that BV is a well-behaved function of temperature. It has a negative temperature dependence, and the temperature coefficient decreases for higher values of $n_{s(extrinsic)}$.

To complete our study, we have measured the temperature dependent characteristics of the gate current. We have found that I_G is thermally activated. This is evident in an Arrhenius plot of I_G/T^2 for one of the samples shown in Fig. 6. The activation energy depends on bias. This is consistent with a thermionic-field emission model for the gate current. The evolution of the activation energy with V_{DG} is shown in Fig. 7 for several samples. Comparison with a simple model (discussed below) allows for the extraction of

198
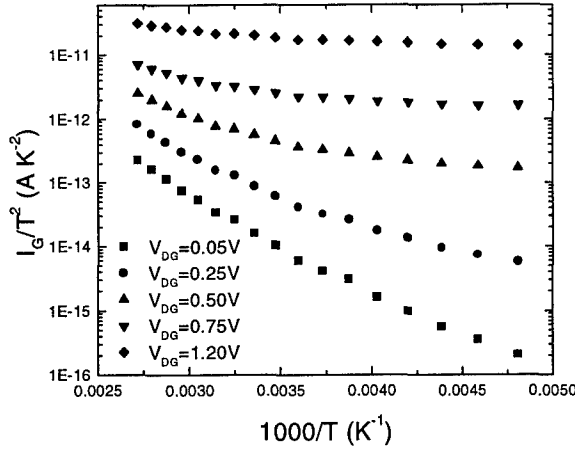
Figure 6: Arrhenius plot of the gate current. The activation energy decreases as V_{DG} increases and approaches V_T.
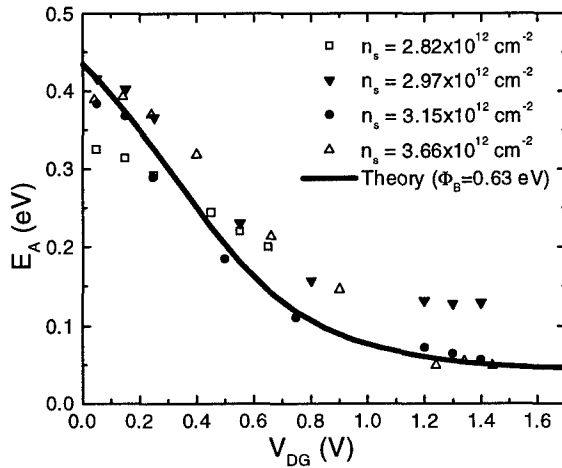
Figure 7: Activation energy of I_G at various bias values for different samples.

the Schottky barrier height of the gate which is found to be 0.63eV.

III. New Model for BV

In our experiments, we have observed that breakdown is a purely drain-gate phenomenon, $n_{s(extrinsic)}$ is the only structural parameter that significantly affects BV, the reverse-biased gate current is a well-behaved function showing temperature activation throughout, and BV has a negative temperature dependence that is more prominent for lower $n_{s(extrinsic)}$.

The new tunneling-limited model for BV (9) concludes that there should be a nearly inverse relationship between BV and $n_{s(extrinsic)}$ and that BV should be rather insensitive to other structural parameters. Fig. 8 presents BV vs. $n_{s(extrinsic)}$ results for leading devices in the literature and theory lines based on
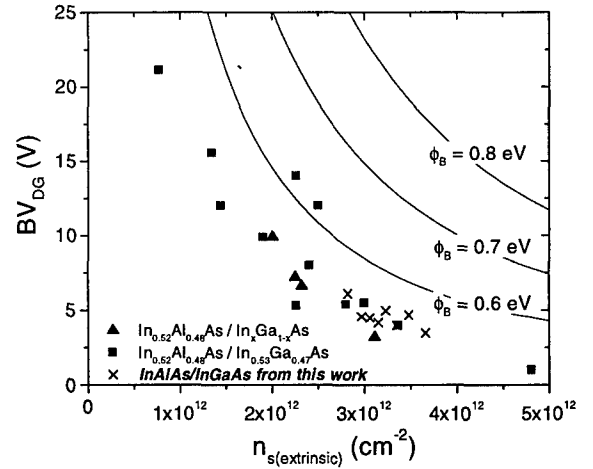
Figure 8: BV_{DG} vs. $n_{s(extrinsic)}$ for InAlAs/InGaAs HEMTs from the literaure and this work. The lines represent theoretical limits of BV on devices with the indicated Schottky barrier height.

the tunneling-limited model for the Schottky barrier heights indicated. The results from our sample set correspond very well to the theoretical and experimental trends offered in the literature, leading us to conclude to the first order that the tunneling-limited model is appropriate for these devices. According to the model, calculations for the off-state breakdown current are dominated by a peak in the electric field under the gate at its drain end. This peak results from a depletion region extending into the extrinsic channel at the drain end of the gate. This model suggests that $n_{s(extrinsic)}$ is the only structural parameter that has a significant impact on the magnitude of the peak in the electric field and, therefore, BV.

The tunneling model alone, however, does not include any temperature dependence and therefore does not help in explaining our experimental observations on the temperature dependence. In incorporating temperature dependence effects, it is important to recognize that the electrostatics of the problem near breakdown are unlikely to be much affected by T. This is because of the high aspect ratio of the depletion region in the drain of the device. Therefore, we can still use 0 K electrostatics in our revised model. On the other hand, for a given field distribution underneath the gate, the gate current is strongly affected by temperature. The tunneling model needs to be extended to include thermionic-field emission as well as thermionic emission over the gate Schottky barrier (11). This does not complicate the model in a significant way since these current components depend only on ϕ_B, the Schottky barrier height of the gate, and the electric field.

If the gate current is determined primarily by tunneling and thermionic-field emission in the gate Schottky diode, currents from different samples should match if the field configuration under the gate is the same and they have the same ϕ_B. In fact, we have found that if we match the gate

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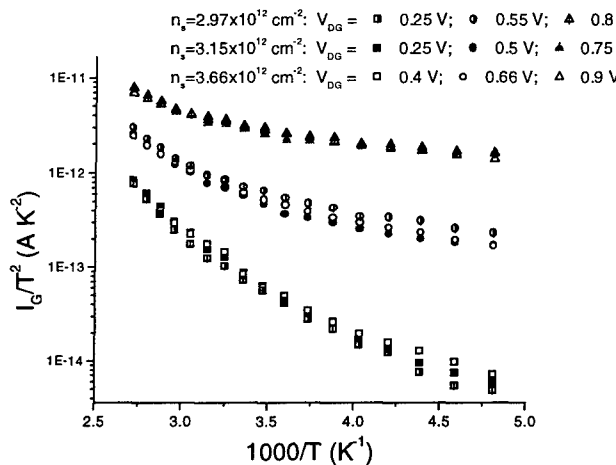
Figure 9: "Universal behavior" of I_G across samples. I_G vs. T dependence is identical for different samples if proper value of V_{DG} is selected.

Figure 10: Experimental and theoretical bias dependence of I_G at the temperature extremes for a sample with $n_{s(extrinsic)}= 3.15 \times 10^{12}$ cm^{-2}.

currents on different samples at any given temperature, the evolution of those gate currents with temperature is identical if V_{DG} is held constant and above threshold. This "universal" behavior is shown in Fig. 9.

Fig. 5 shows calculations of BV_{DG} based on the extracted Schottky barrier height and the known value of $n_{s(extrinsic)}$ for the three measured samples shown. The qualitative agreement is fairly good especially given that the model does not take into consideration non-idealities such as the presence of a cap recess. As before, once ϕ_B and $n_{s(extrinsic)}$ are independently determined, there are no adjustable parameters in this theory. The reason for the reduced temperature coefficient for increased $n_{s(extrinsic)}$ is now obvious. For higher $n_{s(extrinsic)}$, tunneling plays a more significant role in the current and thus the effect of temperature (thermionic-field emission) is smaller.

As a further confirmation of the theory, we investigate the bias dependence of the gate current at various temperatures. In Fig. 10 we see the reverse bias current for the drain-gate Schottky diode near each extreme of the temperature range studied. The current grows strongly as a function of bias when the channel is on ($V_{GD} < -1.3$ V) but grows more slowly past threshold. Only at currents above 1 mA/mm and high temperatures does the current begin to grow significantly again. The theory, which has no adjustable parameters, provides an excellent prediction of the bias dependence of the current at both temperature extremes. Above threshold ($V_{DG} < 1.3$ V), the field under the gate is directly controlled by V_{DG}, hence I_G shows a strong dependence on V_{DG}. Below threshold ($V_{DG} > 1.3$ V), the current grows more slowly since a fraction of V_{DG} is consumed opening the depletion region towards the drain (9). I_G only begins to deviate for currents well above 1 mA/mm. This may be due to the onset of impact ionization in the
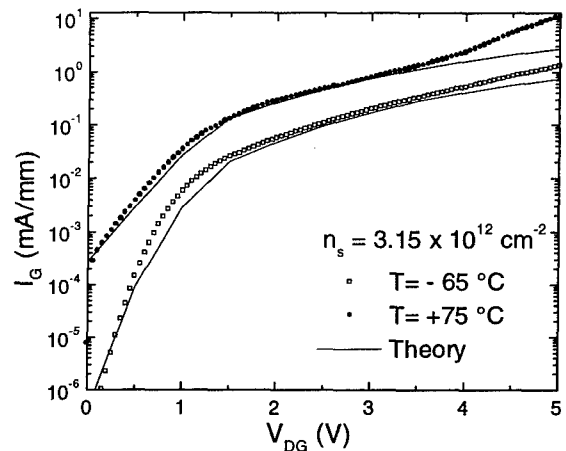
channel. Considering this might be important to describe the on-state breakdown voltage.

IV. Conclusions

In summary, we have investigated the temperature dependence of off-state breakdown in InAlAs/InGaAs power HEMTs and found that the results are in good agreement with a tunneling/thermionic-field emission theory. BV has a negative temperature coefficient that is more prominent for a lower $n_{s(extrinsic)}$. The theory predicts well the bias dependence of the reverse diode current and the temperature dependence of BV_{DG} as well as the actual values of BV_{DG}.

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Fluorine Limited Reliability of AlInAs/InGaAs High Electron Mobility Transistors with Molybdenum Gates

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Abstract

A highly reliable AlInAs/InGaAs high electron mobility transistor with the projected life time of 10^6 hours at 125°C is developed. The gate electrode sinking is eliminated by adopting molybdenum gate contact metal, and the carrier passivation is controlled by eliminating the extrinsic fluorine containing processes. The experimental results and theoretical calculation indicate the present reliability is limited by the intrinsic fluorine contamination from the air.

I. Introduction

There has been a common view that AlInAs/InGaAs high electron mobility transistors (HEMTs) have poorer reliability than GaAs-based HEMTs, while those have better performance especially at millimeter-wave frequencies. Recently several approaches have been reported to improve the reliability of AlInAs/InGaAs HEMT [1]-[4]. In addition, four different degradation mechanisms have been suggested, such as gate electrode sinking [5], penetration of ohmic metals [1][5], surface degradation of AlInAs layer [2] and fluorine (F) contamination [6]. In our previous work, it has been found that the changes of the zero-gate bias saturation drain current (I_{dss}) and the pinch off voltage (V_p) of AlInAs/InGaAs HEMTs during the reliability tests are due to either titanium (Ti) gate electrode sinking or F diffusion [5], and that the thermally diffused F passivates donors in the n-AlInAs layer [7]. In this paper, we show a successfully improved reliability of AlInAs/InGaAs HEMT by eliminating those two deterioration factors.

II. Experimental

Figure 1 shows a schematic cross-sectional view of the HEMT used in this study. The Si planar doping layer is used as an electron supplying layer. The sample is
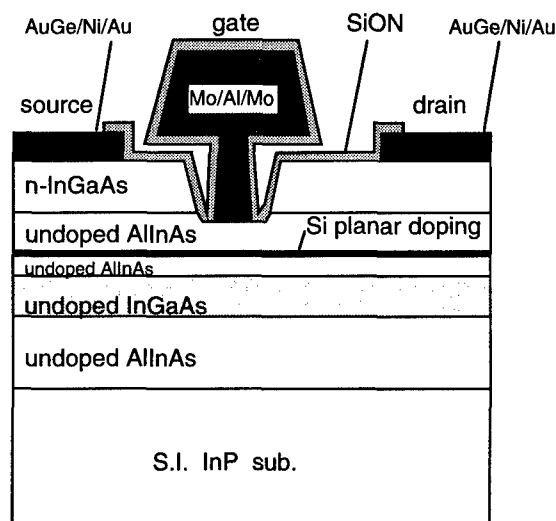
Figure 1 Schematic cross-sectional view of AlInAs/InGaAs HEMT with Mo gate.

passivated with a silicon oxynitride (SiON) layer. The conventional AuGe/Ni/Au is used as the ohmic contact metal and Mo/Al/Mo is newly applied as the gate contact metal. The conventional Ti/Al/Mo gate HEMTs are also fabricated as the reference. The gate length (L_g) and gate width (W_g) are 0.15 μm and 120 μm, respectively. For the device fabrication, the extrinsic F contamination is controlled by eliminating F containing etching processes (such as HF solution treatment). DC accelerated life tests
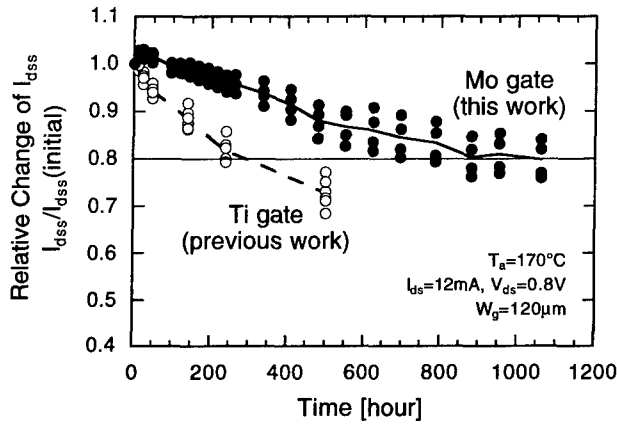
Figure 2 Relative changes of I_{dss} during the DC accelerated life tests at 170°C for Mo gate HEMTs in this work and Ti gate HEMTs in the previous work [5].

Figure 3 V_p shift versus time for life tests. Open circle and closed circle are for HEMTs with Ti gates measured in the previous work [5] and HEMTs with Mo gates in this work, respectively.

are performed at temperatures from T_a=170°C to 240°C under our typical DC biasing parameters of I_{ds}=12mA and V_{ds}=0.8V.

III. Results and Discussion

Figure 2 shows the relative change of I_{dss} during the life tests at 170°C for the devices in this work and the previous work [5]. Mo gate HEMTs fabricated by the F eliminating process show longer life time than Ti gate HEMTs fabricated by the F containing process.

First, to examine the effect of gate electrode sinking as a failure mechanism, we compare the V_p shifts of Mo gate HEMTs during the life tests with those of Ti gate HEMTs, in which Ti was found in the AlInAs layer after the life tests by X-ray spectroscopy analysis [5]. **Figure 3** shows the results of the life tests at 170°C. V_p of Mo gate HEMTs keeps almost constant, while those of Ti gate HEMTs gradually decrease. This result suggests that the gate electrode sinking is negligible for the Mo gate HEMTs. **Figure 4** shows the relative change of I_{dss} during the life tests at 240°C for Mo and Ti gate HEMTs, both of which are fabricated by the F eliminating process in this work. This result also suggests that Mo is superior to Ti as gate electrode in terms of the reliability.

Next, to investigate the F contamination, we compare

the median-time-to-failure (MTTF) of the Ti gate HEMTs fabricated by the F eliminating process with those by the F containing process. The failure criterion is defined as I_{dss}/I_{dss}(initial)=0.8. The former reveals the MTTF of about 5 hours at 240°C, while the latter does only 5 minutes. This result indicates that F contamination is a dominant factor in terms of reliability.

Then, to examine the effect of F contamination quantitatively, we investigate the relative I_{dss} shift during the life tests theoretically.

The thermal degradation of electrical properties of the AlInAs should be determined by the electrochemical reaction as described as follows [6] :

$$F_{in\ air} \rightarrow F_{diffused}. \text{-----(1)}$$

$$F_{diffused} + e \rightarrow F^-. \text{-----(2)}$$

$$F^- + Si^+ \rightarrow F\text{-}Si. \text{-----(3)}$$
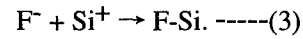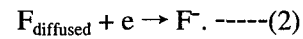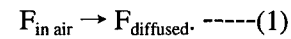
At first, fluorine atoms thermally diffuse into the AlInAs layer (Eq.(1)). Then the diffused fluorine atoms capture free electrons (Eq.(2)). Consequently the ionized fluorine atoms react with donor atoms (Si) to passivate the donors (Eq.(3)). The electrochemical kinetics theory leads to the Eq.(4) expressing the decrease of carrier concentration (n) in n-AlInAs material due to the thermal annealing :

202
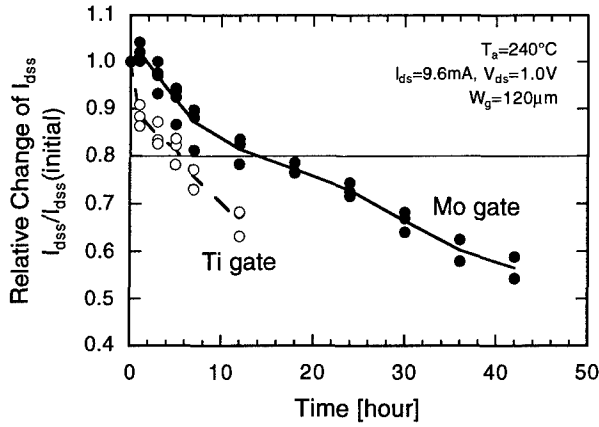
Figure 4 Relative changes of I_{dss} during life tests at 240°C for Mo gate and Ti gate HEMTs fabricated by the F eliminating process.

Figure 5 Relative changes of I_{dss} during life tests at various temperatures for Mo gate HEMTs fabricated by the F eliminating process with the theoretical curves obtained from Eq.(6).

$$n = n_0 exp[-k_0 t \exp(-E_a/k_B T)], \text{-----}(4)$$

where k_0=9180 sec^{-1} and E_a=1.0 eV are experimentally obtained [6]. The drain current (I_{ds}) of HEMTs is also expressed with sheet carrier concentration in the channel layer (n_s) through the gradual channel approximation as follows :

$$I_{ds} \approx q\mu(L_g/d_{sd})V_{ds}[n_s-\varepsilon \ V_{ds}/2q(d_{gc}+\Delta d)], \text{-----}(5)$$

where L_g, d_{sd}, ε, d_{gc} and Δd are gate length, distance between source and drain electrode, permitivity of electron supplying layer, distance between gate electrode and channel layer, and the effective thickness of 2DEG, respectively. Assuming that V_{ds} is constant, we now obtain the Eq.(6) by combining Eqs.(4) and (5) to express the relative Idss shift of HEMTs during the life tests :

$$I_{dss}/I_{dss}(initial) \approx \exp[-9180t \exp(-1.0/k_B T)]. \text{-----}(6)$$

Figure 5 shows the relative changes of the I_{dss} during life tests at various temperatures for Mo gate HEMTs fabricated by the F eliminating process with the theoretical curves obtained from Eq.(6). The theoretical curve well expresses the experimental data, which indicates that the primary degradation is determined by the carrier passivation even for the HEMTs fabricated by the F eliminating process.

Figure 6 shows the relative changes of the source and drain parasitic resistances (R_s and R_d) during the life tests for Mo gate HEMTs fabricated by the F eliminating process. R_d increases much faster than R_s, which is well consistent with the reference [4][6]. This result suggests that the ionized F atoms easily migrate through the AlInAs layer under the electric field, from the region beneath the gate electrode to the drain electrode region resulting in the dominant carrier passivation in the drain electrode region. F is considered to be incorporated from the air [8] because F is eliminated from the materials used for the device fabrication process. In addition, sub-atomic percent (10^{12} - 10^{13} cm^{-2}) F is detected on the surface of n-AlInAs layer exposed to the air by X-ray photoelectron spectroscopy measurement.

Finally, **Figure 7** shows the Arrhenius plot for the MTTF of the HEMTs fabricated by the F elimination process. The projected MTTF at 125°C is 10^6 hours, which is one of the highest values for AlInAs/InGaAs HEMTs and rivals well-established GaAs-based HEMTs. The activation energy (E_a) is 1.7 eV, which is comparable with the reference [1][2][3][4].

203
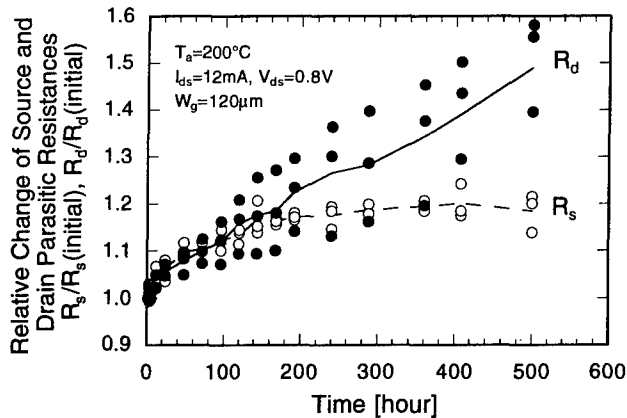
Figure 6 Relative changes of the source and drain parasitic resistances (R_s and R_d) during life tests for Mo gate HEMTs fabricated by the F eliminating process.

Figure 7 Arrhenius plot for MTTF of HEMTs with Mo gates fabricated by the F eliminating process.

IV. Summary

Highly reliable AlInAs/InGaAs HEMTs are obtained by adopting Mo gate electrode and eliminating the F containing processes. The reliability of those HEMTs is limited by F incorporation from the air.

V. Acknowledgement

The authors would like to thank Mr. Kojima and Mr. Totsuka for supporting the device fabrication processes. They also thank Dr. Yoshida for fruitful discussion and encouragement through this work.

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BULK TERNARY INDIUM PHOSPHIDE ARSENIDE, InP$_{1-x}$As$_x$: GROWTH AND CHARACTERIZATION

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Introduction

The growth of bulk single crystal ternary III-V's has been demonstrated employing conventional semiconductor growth technologies. Materials so prepared include; gallium-indium arsenide, Ga$_{1-x}$In$_x$As[1-4], gallium-indium antimonide, Ga$_{1-x}$In$_x$Sb[5], and indium phosphide-arsenide, InP$_{1-x}$As$_x$[6]. The InP$_{1-x}$As$_x$ system addresses the compelling device interest in the 2-3μm spectral regime for low cost, ultra-sensitive gas detection and monitoring. DFB lasers based on InP$_{1-x}$As$_x$ substrates, x $\cong$ 0.40 are predicted to have particular promise in this area. To date, InP$_{1-x}$As$_x$, 0 < x < 0.10, single crystals have been grown using LEC and initial device structures fabricated using these ternary materials attest to the quality and potential applications[7].

I. Generic Bulk Ternary III-V Relevance and Issues

Generically, bulk ternary III-V single crystal alloys provide access to the vast lattice parameter, bandgap and spectral regimes outside the discrete intrinsic limits imposed by binary III-V materials. Thereby, availability of III-V bulk ternary crystals affords an additional degree of freedom to device concept and design through the opportunity to composition and lattice-tune substrates to appropriately match epitaxial layers. As a first-order benefit, this can avoid the necessity for deposition of costly and often only moderately effective compositionally graded epitaxial layers on binary substrates to compensate for small degrees of lattice mismatch. In this regard alone, increased yield, and improved epilayer quality is anticipated to result in significant cost reduction for devices traditionally fabricated on binary substrates. The more far-reaching impact, includes the potential for developing bulk devices, thereby avoiding costly epilayer deposition altogether and providing avenues to novel epitaxial devices in spectral/bandgap regimes heretofore not attainable utilizing simple binary substrates. The range of physical parameters for the ternary III-V materials systems are given in Table I.

Single crystal growth of bulk ternary indium phosphide-arsenide has been accomplished using the liquid encapsulated Czochralski (LEC) technique. The important technological key to the growth of this and other ternary III-V materials by Czochralski and LEC is the utilization of compositionally compliant, lattice matched and melting point compatible seeds. Seeds are generated by a series of iterative growth runs, "bootstrapping" whereby the alloy composition is monotomically increased from the appropriate binary compound[1,2]. For obvious reasons ternary growth must be initiated from the higher melting end-member. Bootstrapping is an extremely time intensive process, however, once a seed base is established there exists the potential for compositional tuning of substrates to any discrete composition desired.

Table 1. Ternary III-V Physical Parameters

Ternary System	Melting Point Range(°C)	Lattice Constant Range (Å)	Bandgap (μm)
InAs-GaAs	943-1238	5.654-6.058	0.356-1.40
InP-GaP	1062-1467	5.447-5.869	1.35-2.24
InAs-InP	943-1062	5.869-6.058	0.356-1.35
GaAs-GaP	1238-1467	5.447-5.654	1.40-2.24
InSb-GaSb	525-706	6.095-6.497	0.18-0.69
InSb-InAs	525-943	6.058-6.497	0.18-0.356

The fundamental difficulties in producing bulk ternary single crystals by solidification from the melt can be appreciated by examination of the respective pseudobinary phase diagrams. Phase relations for the InP-InAs system[8] are shown in Figure 1. Note initially, the major variation between different sets of data points representing different investigators. The high degree of uncertainty, in the position of published liquidus and solidus curves dictates that the melt composition, as a function of the first-to-freeze(FTF) crystal composition, must be obtained empirically. This is not unique to the In(P,As) system, as similar degrees of uncertainty exists for all of the published pseudobinary III-V composition data.

Additional complexity arises from the solid solution characteristics of the III-V pseudobinary systems which results in non-unity segregation between the respective end-members. Not considering absolute values or uncertainty in

absolute position of the solidus, for any given melt composition the FTF material will contain a specific concentration of arsenic. As solidification continues, the remaining liquid will become increasingly rich in arsenic. For a finite melt, the composition of a growing single crystal exhibits a corresponding increase in arsenic. Ultimately an excessive accumulation of arsenic can occur at the solid/liquid interface leading to constitutional supercooling, interface breakdown and the onset of polycrystallinity. The degree to which the crystal perfection deteriorates as a function of ternary composition is dependent on the pseudobinary system and can be somewhat controlled by growth speed, thermal gradient and other related growth parameters.
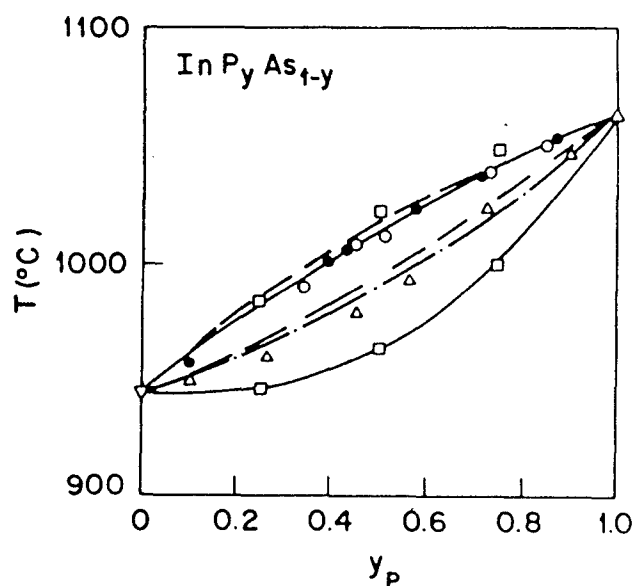
Figure 1. InP-InAs pseudobinary phase relations[8]

Accompanying growth problems which contribute to interface breakdown are the effects of strain due to the changing lattice parameter. Figure 2 depicts graphically the lattice parameter change between the binary components for several III-V ternary compositions. The magnitude of the difference is reflected by the slope of the join for each respective pair of binary materials. As example, the difference in lattice parameter between GaAs-InAs and InP-InAs is 0.404Å and 0.189Å respectively, more than a factor of 2 less for the phosphide system. Thus if we compare (Ga,In)As and In(P,As), for similar size In(P,As) crystals grown from similar volume melts, the lattice parameter change will be proportionately less for corresponding composition changes. This suggests less strain and a larger fraction of the melt may be grown as single crystal. Reported observations, for the (Ga,In)As system are that interface breakdown can occur abruptly and the growing crystal converts from single to fine grain poly within a few tenths of a millimeter[1-4]. In this regard, it is anticipated that composition change along the growth direction of In(P,As) and Ga(P,As)

crystals will not have as dramatic effect as that observed for (Ga,In)As or expected for (Ga,In)P.
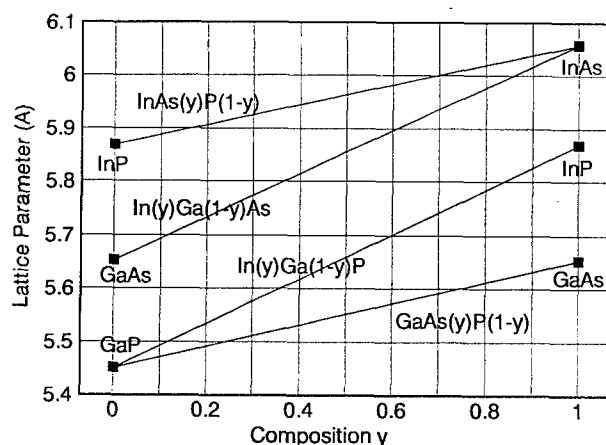
Figure 2. Lattice parameter as a function of composition for several III-V ternary material systems

II. Experimental

Crystals for these studies were grown using the LEC technique and conditions similar to those required for InP given the close proximity compositionally. Research size r-f heated, high pressure crystal growth systems[6] were employed. Nominally 150-200gm melts prepared from precompounded InP and InAs were contained in 5cm. diameter hemispherical bottom pBN or fused silica crucibles. Dry boric oxide, <200ppm H_2O, was employed as the encapsulant. Growth in both the <111> and <100> directions was investigated. Initial studies were conducted using InP seeds while subsequent growth was accomplished on In(P,As) seeds.

III. Results and Discussion

In general, the ability to grow single crystal $InP_{1-x}As_x$ and the percentage of the melt that could be obtained as single crystal was observed to be a function of the growth parameters, and the magnitude of the composition/lattice mismatch between the seed and FTF crystal. Obviously, the closer the FTF composition was to the seed composition the more easily good growth was established and proceeded as single crystal. Unfortunately, in the extreme case, for melts containing very low concentrations of arsenic, (<1%) little is incorporated into the growing crystal, defeating the concept of bootstrapping. Using InP seeds, for similar growth parameters, completely single crystals could be grown for melt compositions containing <5 mole% InAs. Conversely, melts containing >15 mole % InAs yielded no single crystal growth and resulted in polycrystalline freeze-on. Typical crystals were 2-3cm diameter, 4-8cm long and weighed nominally 150gms.

Single crystal yield and melt composition for several In(P,As) crystals grown on InP seeds are summarized in Table 2. For consistency, yield of single crystal was recorded based on 150gms of melt grown. Composition was determined on FTF and last-to-freeze(LTF) single crystal material only using energy dispersive x-ray spectroscopy (EDS), wavelength dispersive x-ray spectroscopy (WDS) and photoluminescence (PL). The data presented in Table 2 represents a combination of EDS and WDS values averaging several data points on the same wafer. FTF samples were cut as close to the seed as possible and therefore were small diameter by comparison to the LTF. Composition was determined only on single crystal material due to the ambiguity in data for polycrystalline material. Composition change along the length of the single crystal region is represented by the FTF and LTF compositions and is a function of the estimated mass fraction of the melt solidified prior to the onset of polycrystallinity.

Table 2. *Composition and Volume of Single Crystal In(P,As) as a function of Melt Composition for Growth on InP <111> Seeds.*

Melt Composition InP/InAs	$InP_{1-x}As_x$ Single Crystal		% Single Crystal
	x @ FTF	x @ LTF	
0.97 / 0.03	0.02	0.06	100%
0.96 / 0.04	0.025	0.08	100%
0.95 / 0.05	0.025	0.057	40%
0.90 / 0.10	0.07	~0.095*	15-20%
0.85 / 0.15	Poly	Poly	0

* Value questionable due to cracking and proximity to a polycrystalline region

Radial composition uniformity was determined on circular (111) wafers cut normal to the crystal growth axis with four data points at the outer circumference and one at the center of the wafer. Table 3 is a tabulation of data for a LTF single crystal wafer from a crystal grown on a 5% arsenic ternary In(P,As) seed. It is interesting to note that the PL intensity for the nominal 8% arsenic ternary material was higher than the InP reference substrate used to calibrate the wavelength. Compositional variations in both cases are very small, +/- 0.05%, across the wafers and may be related to interface characteristics.

Typically, ternary single crystal grown by LEC exhibits a high degree of radial composition uniformity. However, the composition changes moderately along the length due to significant separation between the liquidus and solidus phases. The amount of change in composition is obviously then dependent on the pseudobinary system, the volume of the melt and the fraction of solid crystallized therefrom. Thus, individual wafers cut normal to the growth direction of a given crystal will be of uniform composition, whereas some composition variation, wafer-to-wafer, is to be expected. In practice, the situation represents a "catch 22"; i.e. changing

composition is beneficial and that element of the technology which permits "bootstrapping", while detrimental to providing the high degree of wafer-to-wafer uniformity necessary for device manufacture and commercial acceptance. Note also, that seeds generated by bootstrapping exhibit nonuniform composition along the length corresponding to the crystal from which they were cut. This presents an issue with regard to determination of a melt composition to provide appropriate lattice match between the seed and FTF crystal composition.

Table 3. *PL Results for a (111) In(P,As) Substrate, Maximum 10% Arsenic, Grown on a Ternary, 5% arsenic, In(P,As) Seed.*

Wafer	Position	Peak Wavelength (Å)	PL Intensity	% As
InP		9250	50	0
In(P,As)	center	9800	100	8.0
"	1-edge	9830	50	8.2
"	2-edge	9830	50	8.2
"	3-edge	9840	55	8.3
"	4-edge	9830	55	8.2

An additional benefit derived from the nonuniform composition is the fact that, to date, device researchers have not had the luxury of ternary substrate availability. Small compositional differences wafer-to-wafer, at this stage of the technology, permit investigation of the effects of subtle compositional differences in epitaxial growth and device design without the need to grow large numbers of crystals with small composition changes.

In contrast to observations reported for other ternary III-V systems, the transition from single to polycrystalline growth in In(P,As) crystals begins on the exterior of the growing ingot as multiple twins which progress to complete polycrystallinity as growth continues. This is significantly different when compared to an abrupt transition from completely single to fine grained polycrystalline growth, due to interface breakdown reported in the (Ga,In)As system[1-4]. In addition the twin formation observed in the In(P,As) system is different from that observed for InP. Twins, typical of InP, i.e. laminar <111> twins, have not been observed, whereas, In(P,As) twinning initially appears dendritic, nucleating on the crystal surface and growing inward. Figure 3 depicts the traditional InP laminar twin formation observed on a <111> slice cut normal to the growth axis (left) and the twin structure observed in In(P,As) parallel (center) and normal (right) to the growth direction.

The most serious problem encountered in the ternary material was that of cracking. We postulate that this is the combined result of too great a lattice/composition mismatch between seed and FTF crystal, the constantly changing composition along the length and induced stress due to growth in a steep thermal gradient. The degree of cracking follows a trend similar to that observed with regard to the onset of

polycrystalline growth and related to the composition difference between seed and FTF crystal composition. It was observed that, for growth under similar conditions, the closer the lattice match to the seed the less severe the cracking. Minimum to no cracking was observed for growth on seeds from melts containing ~3 mole% InAs. Ternary seeds with a maximum arsenic concentration of x = 0.05 were fabricated from such crystals and utilized for growth of In(P,As) with "x" values approaching 0.10.
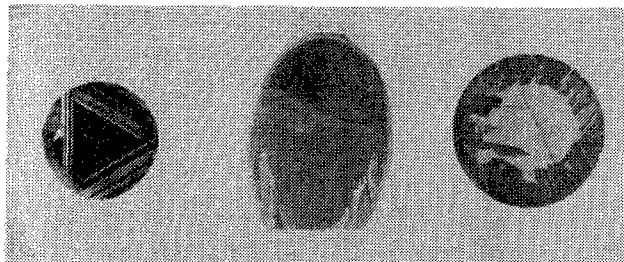
Figure 3. Twin structure in InP and In(P,As) crystals.

Electrical characteristics were determined using standard Hall effect techniques. Carrier concentration and mobility are shown in Table 4 for FTF and LTF single crystal sections only at room temperature and 77K. The equivalent values for the binary source materials employed are included for comparison and are consistent with anticipated values. In(P,As) has been successfully doped with sulfur to produce material with N_D-$N_A \approx 10^{18}$ cm^{-3}. Semi-insulating material has not yet been prepared.

Table 4. Electrical Characteristics of Undoped In(P,As) Single Crystals as a Function of Composition. Values for Binary Source Materials are Included for Comparison

Crystal	N_D - N_A (cm^{-3})		Mobility (cm^{2}V^{-1}s^{-1})	
	300 K	77K	300 K	77K
InP	5×10^{15}	2×10^{15}	4,000	25,000
InP$_{0.975}$As$_{0.025}$	8.1×10^{15}	6.4×10^{15}	4,226	27,367
InP$_{0.943}$As$_{0.057}$	5.4×10^{15}	4.6×10^{15}	4,688	24,498
InP$_{0.920}$As$_{0.080}$	5.7×10^{15}	4.8×10^{15}	4,504	24,034
InP$_{0.903}$As$_{0.097}$	5.9×10^{15}	4.9×10^{15}	4,330	22,041
InAs	3×10^{16}	2×10^{16}	>17,000	>20,000

IV. Summary

In(P,As) bulk ternary single crystal growth has been demonstrated using both InP and ternary In(P,As) seeds. Arsenic concentrations to nominally 10% have been achieved. While problems related to cracking and compositional uniformity exist single crystals are capable of producing

wafers and bulk material for characterization and preliminary device studies.

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RESIDUAL STRAIN AS A MEASURE OF WAFER QUALITY IN INDIUM PHOSPHIDE CRYSTALS

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Introduction

The quantitative photoelastic technique was utilized to characterize residual strain as a measure of InP wafer quality. A series of standard wafers (Sn-doped, 2-inches, LEC-grown InP) received commercially from four different wafer suppliers were characterized and compared to demonstrate a feasibility of residual strain as the quality measure. In order to understand the residual strain well, the generation mechanism was modeled and explained in conjunction with plastic deformation originating dislocation generation due to thermal stress caused during various processes in crystal growth and device fabrication.

I. Background

Many investigators have made much effort to improve the quality of indium phosphide crystals, in which etch pit (dislocation) density is essentially used as a measure of crystal quality. From aspect of crystal growth, temperature or thermal stress profiles during crystal growth and cooling processes are the most important problem, because a part of thermal stress is relaxed generating dislocation and then, as the result, residual strain or stress is frozen into crystalline ingot. Therefore, the residual strain may be used as another measure of crystal quality. It may be, furthermore, used for process control in fabricating various devices, because thermal stresses induced during various device processes modify the residual strain originating in crystal growth, wafer slicing and polishing processes.

For measurement of strain in crystals, several methods can be considered; that is, X-ray diffraction, Raman scattering, photoelastic technique, and so on. X-ray diffraction is a direct method to measure strain (change in lattice parameters). Raman scattering is an indirect method to measure change in optical phonon frequencies. Photoelastic technique is another indirect method, in which strain-induced birefringence is measured and connected to strain by photoelastic effect. From viewpoint of sensitivity, it is superior to X-ray diffraction and Raman scattering.

Völkl and Müller[1] employed the photoelastic technique using conventional linear and circular polariscopes, for the first time in InP crystals. Müller[2] and Hirano et.al.[3] also used them to see microscopic strain field patterns of precipitates as well as whole-wafer strain patterns. However, their photoelastic technique was not quantitative but qualitative. In order to characterize residual strain quantitatively, Yamada[4] developed a high-sensitivity computer-controlled infrared polariscope. Although it was used for quantitative characterization of InP wafers, it was poor ($\approx$2mm) in spatial resolution[5, 6]. We recently developed a scanning infrared polariscope[7] as a whole-wafer inspection tool with reasonably high spatial resolution ($\approx$ 200μm), which was used in characterizing fine

structures such as slip-like deffects originating from crystallographic glide during crystal growth process, inclusions or voids inside the wafer, and scratches on the surface[8, 9].

In this paper, we present the photoelastic characterization results, which were measured in various indium phosphide wafers by using a scanning infrared polariscope with high sensitivity and high spatial resolution, to demonstrate that the residual strain may be used as a good measure of wafer quality.

II. Quantitative Photoelastic Characterization of Commercial Standard Wafers

The photoelastic characterization is based on the measurement of birefringence induced by residual strain, in which some combinations of strain components in wafer plane: that is, $|S_{yy} - S_{zz}|$, $|S_{yz}|$, and $|S_r - S_t|$ for (100) wafer can be evaluated from the refractive ellipse of birefringence measured[4, 5]. The strain component of $|S_r - S_t|$ is the absolute value of the difference between the radial and tangential strain components in a cylindrical coordinate system, which is the most useful value as a quality measure.

In the present photoelastic characterization, we used an improved version of scanning infrared polariscopes[7, 8, 9], whose performances were summarized in Table 1. In order to eliminate unwanted surface effects in light transmission and polarization effect of light source, a sophisticated technique was developed in the scanning infrared polariscope[7].

Tabel 1. Typical performances of scanning infrared polariscope used in the present photoelastic characterization.

Wafers	GaAs, InP, GaP, etc.
	double-side polished,
	upto 8-inches in diameter
Sensitivity (typical)	10^{-7} in the term of strain
Spatial Resolution	50μm in min.
Measurement Time	3 hours for 3-inch diam.
	@200μm resolution
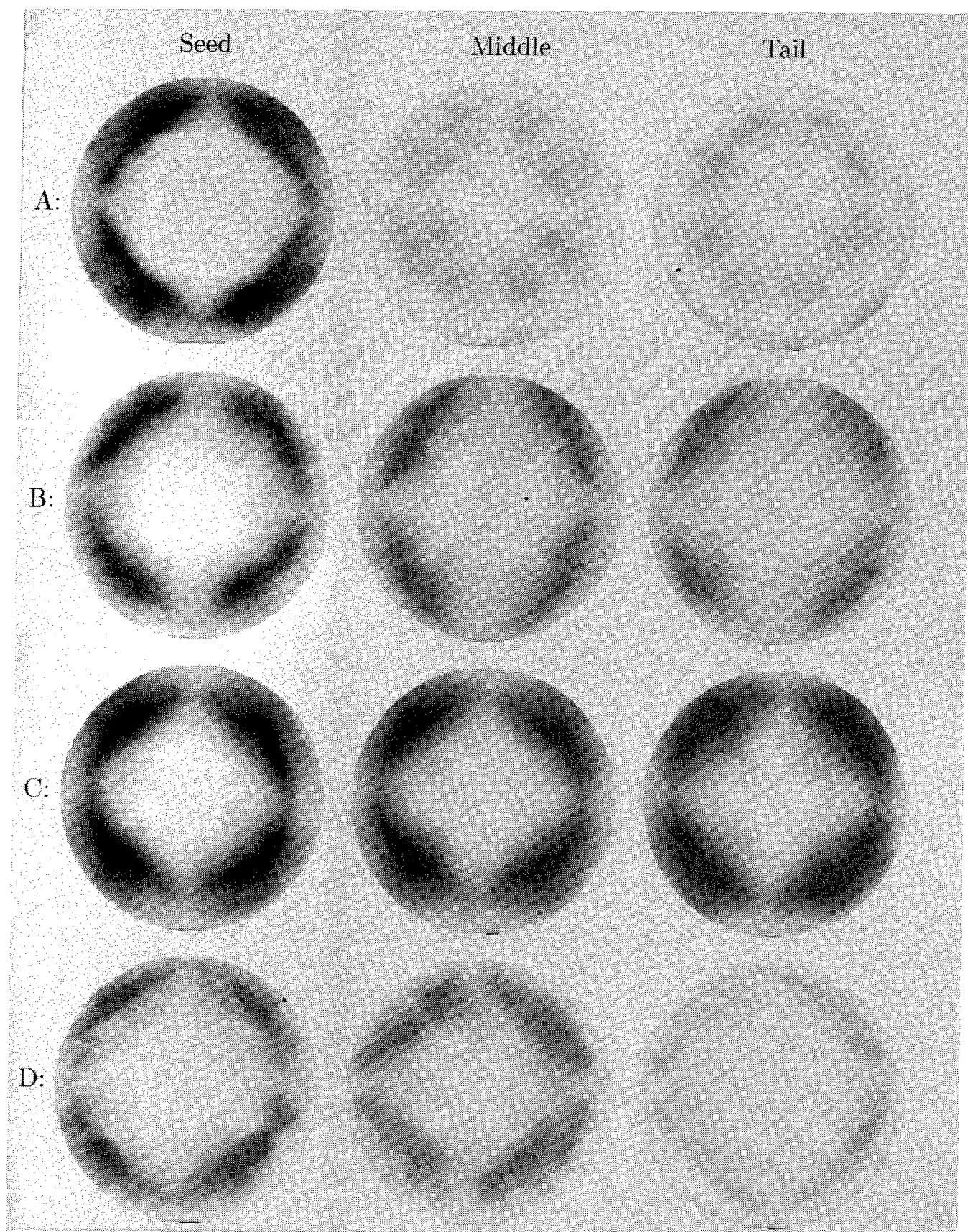
Fig. 1. Two-dimensional maps of $|S_r - S_t|$ measured in a series of wafers sliced from the seed, middle, and tail portions of ingots grown by four different wafer suppliers (A-D).

A series of standard wafers received commercially from four different wafer suppliers were characterized and compared to demonstrate a feasibility of residual strain as the quality measure. The specifications of the wafers characterized here are listed in Table 2.

The two-dimensional maps of $|S_r - S_t|$ are shown in Fig. 1, corresponding to the wafer suppliers (A-D) and the sliced portions (Seed, Middle, Tail). The gray scale used in Fig. 1 is the same in all wafers and the darker indicates the higher strain. All seed-portion wafers of the A-D suppliers exhibit almost the same fourfold pattern, although there are differences in fine structures. The middle- and tail-potion wafers of the A supplier show eightfold pattern and are flat in comparison with the seed-portion wafer. The middle- and tail-potion wafers of the B and C suppliers show the same fourfold pattern as the seed portion. The wafers of the D supplier show a fylfot pattern or a distorted fourfold pattern indicating that the crystal rotating speed would be fast compared with the crystal pulling speed. It is clearly seen that there is a big difference in the wafers received from the four diffrent wafer suppliers. The fourfold pattern observed here is seemed to be causing from the elastic and plastic properties of InP crystals.
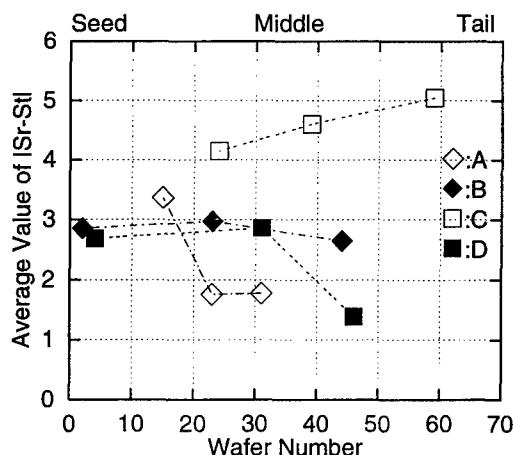
Fig. 2. Average value of $|S_r - S_t|$ plotted as a function of wafer number.

The average value of residual strain over the whole wafer region is plotted in Fig. 2, as a function of wafer number. Except for the C, there is found a tendency that the average value is decreased as the wafer number is increased. The average strain value ranges from 1.5×10^{-5} to 5.1×10^{-5}. According to the elastic equation of $T_{ij} = c_{ijkl}S_{kl}$, the corresponding stress value

may be estimated to be from 6.9×10^5N/m^2 and 23.5×10^5N/m^2. The maximum value observed here is about 5×10^{-4} in the term of strain and 23×10^6N/m^2 in the term of stress, which attains to the upper yield stress of undoped InP at the temperature of about 600°C measured by Yonenaga and Sumino[10].

Here, we may understand from Figs.1 and 2 that there are many variations in the two-dimensional profile and average value of residual strain, reflecting the crystal growth conditions. It is noted here that the residual strain can be decreased by decreasing the temperature gradient during crystal growth processes, from the fact that the residual strain of VCZ-wafers (the axial temperature gradient is 30-50°C/cm) is much lower than that of conventional LEC wafers (100-130°C/cm)[9].

III. Model of Residual Strain Generation due to Thermal Stress

It is very important to understand how the residual strain is generated during crystal growth and device fabrication processes.
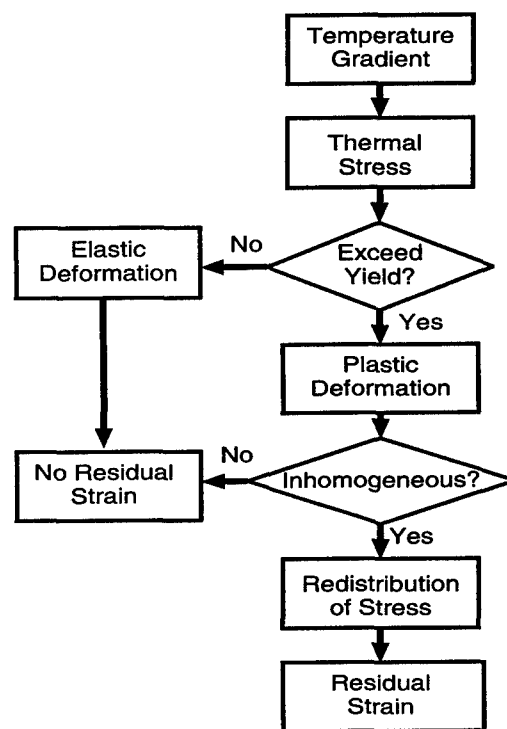
Fig. 3. Flow chart of residual strain generation.

Figure 3 shows a flow chart interpreting the mechanism of residual strain generation. The temperature gradient during crystal growth and device fabrication processesbegins by causing thermal stress. If the thermal stress does not exceed the yield strength, then no residual strain is generated. This means the deformation is elastic. If the thermal stress exceed the yield strength, then the plastic deformation originating dislocation generation occurs. Even if the lastic deformation would occur, the residual strain would not be always generated in a macroscopic sence. The residual strain is generated when the plastic

211

deformation occurs inhomogeneously in wafer or crystal. If the plastic deformation occurs once in a certain local region, a local internal force is generated and deforms the local region by itself while deforming the surrounding region. The internal force causing deformation still exists even if the thermal stress is removed. In the one-dimensional case, the residual strain is the deformation for the unit length. It should be reminded that deformation is generally three-dimensional and furthermore stress and strain are treated as tensor.
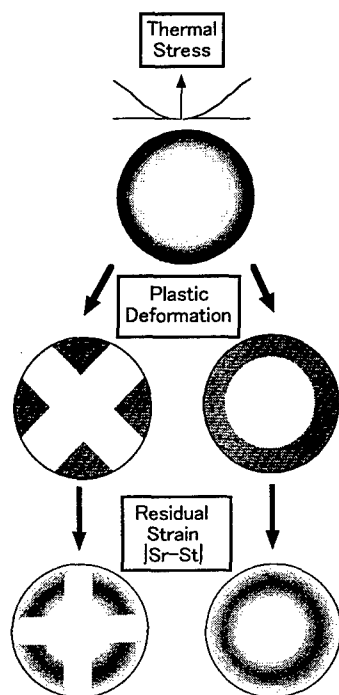
Fig. 4. Two-dimensional distibutions of residual strain modeled with a parabolic thermal stress and two different plastic deformations.

Examples of residual strain generation in the two-dimensional case are shown in Fig. 4. The thermal stress along the radial direction is assumed to be parabolic. For the plastic deformation, the two different cases are taken into account; one is the case that the plastic deformation is isotropically caused by the excess thermal stress near the wafer periphery, and the other is the case that it is anisotropically caused due to the crystallographic anisotropy. The residual strain of $|S_r - S_t|$ is only presented in the figure.

IV. Concluding Remarks

The residual strain can be nondestructively characterized by using the scanning infrared polariscope, as shown in the present work. The origin of residual strain comes from an inhomogeneous plastic deformation; that is, an inhomogeneous distribution of crystal deffects in a macroscopic sense. Therefore, the residual strain may be used as a good measure of wafer quality. Furthermore, it is very useful to find an optimum condition of crystal growth and also to improve various heating processes in fablicating devices.

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Crystal Quality of InGaAs Epitaxial Layer on 3-inch Diameter VCZ/LEC InP(Fe) Substrates

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Abstract

Crystal quality of InGaAs epitaxial layers grown by MOCVD on 3-inch diameter Fe-doped VCZ/LEC InP substrates have been studied by double crystal X-ray diffraction measurements. The crystallographic property of the InP substrates reflected on the InGaAs layers. The average full width at half maximum (FWHM) of X-ray rocking curves of the InGaAs layer on the VCZ-grown InP substrate was narrower than that on the LEC-grown InP substrate. X-ray topographies of the InGaAs layer on the VCZ-grown InP substrate showed less lattice orientation variation than that on the LEC-grown InP substrate. Dark currents of p-i-n photodiodes fabricated on the epitaxial wafers were also studied. The average dark current on the VCZ-grown InP substrate was lower than that on the LEC-grown InP substrate. The standard deviation of dark currents on the VCZ-grown InP substrate was also smaller than that on the LEC-grown InP substrate. Therefore, InGaAs epitaxial layers on 3-inch diameter VCZ-grown InP substrates have superior quality from crystallographic and device characteristics point of view.

Introduction

InP crystals are used for long-wavelength optoelectronic devices such as PDs, LDs, and OEICs. Commercially available InP is generally 2 inches in diameter, so the device fabrication has been done by using a 2-inch diameter wafer or a cleaved rectangle wafer. Recently a 3-inch diameter InP with long ingot length and good crystal quality has been grown [1]. Developments of wafer processing with 3-inch diameter InP will make it possible to lower the device cost drastically. To succeed in 3-inch wafer processing with high device yield, it is important to clarify the relationship between device characteristics and crystal quality of epitaxial wafers. Yabuhara et al. reported that 3-inch diameter Fe-doped InP grown by the VCZ method has lower etch pit density (EPD), lower residual strain, and less lattice orientation variation than that grown by the conventional LEC method [1]. Furthermore, recent studies have shown that dark currents of InGaAs PIN-PDs are very sensitive to crystal quality of 2-inch diameter S-doped InP substrates [2]. Therefore, it is important to investigate the difference of device performance between VCZ and LEC crystals with 3-inch diameter Fe-doped InP.

In this study, we report crystal quality of InGaAs epitaxial layers grown on 3-inch diameter Fe-doped InP substrates which were grown by the VCZ method and the LEC method. We also report dark current distribution of InGaAs PIN-PDs fabricated on these epitaxial wafers.

Experimental

InGaAs epitaxial layers which have a p-i-n structure were grown by MOCVD on 3-inch diameter Fe-doped (001) InP substrates. The growth temperature was 650 ℃. The total thickness of the InGaAs layer was 2.75 μ m. The average EPDs of InP substrates were ~7 $\times 10^3$cm^{-2} for the VCZ crystal and ~3$\times 10^4$cm^{-2} for the LEC crystal.

Crystal quality of InP substrates and InGaAs epitaxial layers were evaluated by double crystal X-ray diffraction measurements. The first crystal was a 4-inch diameter (001) Si wafer, and (004) symmetric reflection was used. A (004) symmetric reflection of epitaxial wafers
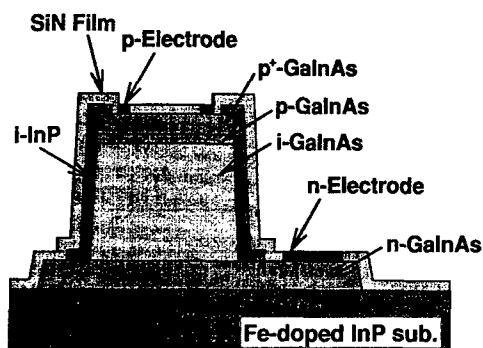
Fig. 1 Schematic cross section of a photo diode chip
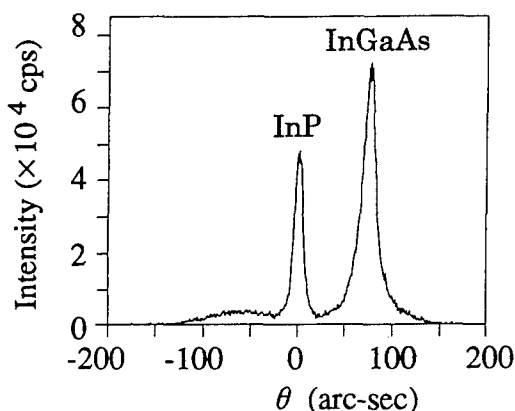
Fig. 2 (004) double crystal X-ray rocking curve of the epitaxial wafer on the LEC substrate

Fig. 3 Diametric distribution of FWHMs of rocking curves of InP substrates and InGaAs layers. Comparison between VCZ and LEC.

was also used for the measurements of rocking curves and topographies. Details of the apparatus have been presented in another report [2].

After the evaluation of crystal quality, photo diode chips which have mesa type structures as shown in Fig. 1 were fabricated. Details of the device structure and characteristics will be reported elsewhere. The lattice mismatch ($\Delta a / a$) between InGaAs and InP is about $- 0.06\,\%$, which is selected to lower dark currents of PDs. The diameter of photosensitive area was 100 μ m. Dark current - reverse voltage characteristics of each chip in a wafer were measured at room temperature by a semi-automatic prober. The number of chips were about 16,000 per wafer.

Results and Discussion

An X-ray rocking curve measured at the center of the epitaxial wafer on the LEC substrate is shown in Fig. 2. The peak separation between the InGaAs layer and the InP substrate is about 80 arc-sec and its value is constant except for the peripheral region of the wafer. Figure 3 shows the diametric distribution of FWHMs of the InP substrate and the InGaAs layer. The average FWHM of the VCZ substrate is narrower than that of the LEC substrate, which is related to the fact that the average EPD of the VCZ substrate is lower than that of the LEC substrate. The average FWHM of the InGaAs layer on the VCZ substrate is also narrower than that on the LEC substrate. These results indicate that crystal quality of the InGaAs epitaxial layer reflects crystal quality of the InP substrate.

The peak separation between the InGaAs layer and the InP substrate (~80 arc-sec) is larger than the sum of FWHMs of the InGaAs
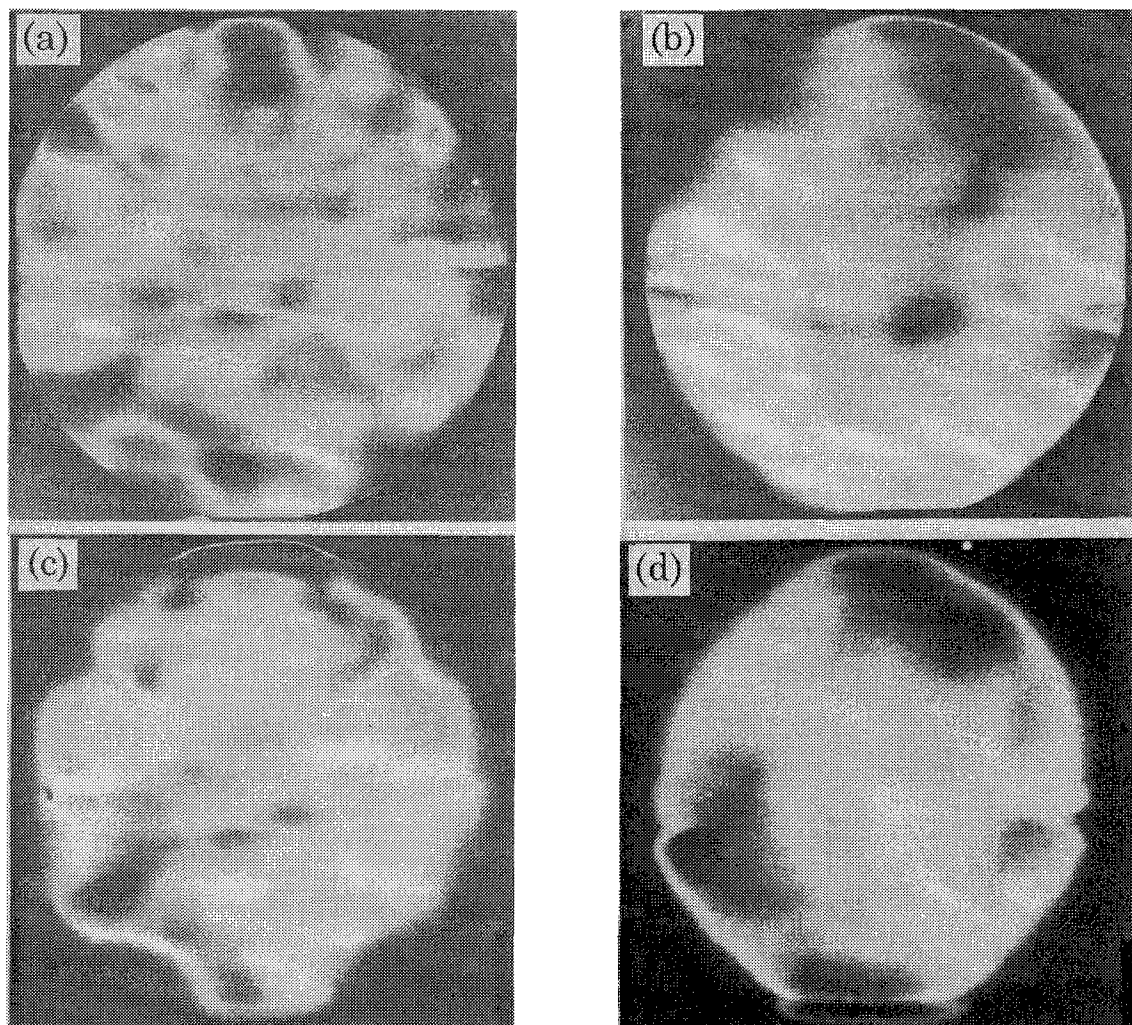
Fig. 4 Double crystal X-ray topographies of InP substrates and InGaAs layers.
(a) LEC-grown InP substrate, (b) VCZ-grown InP substrate, (c) InGaAs layer on
the LEC substrate, (d) InGaAs layer on the VCZ substrate

layer (~16 arc-sec) and the InP substrate (~11 arc-sec). Therefore, it is possible to obtain two topographies of the InGaAs epitaxial layer and the InP substrate from one epitaxial wafer. However, peak angles of rocking curves drift due to the curvature of the wafer, so it is difficult to obtain topographic images of the whole wafer with the asymmetric reflection such as (224) reflection. We adopted (004) symmetric reflection and measured topographies by automatically correcting the incident angle of X-rays according to the wafer curvature. Figure 4 shows the topographies of the InP substrates and the InGaAs epitaxial layers. Whole images of 3-inch wafers were successfully recorded. In both cases of VCZ and LEC, the contrast of the InGaAs topographies

corresponds very well to that of the InP topographies. The contrast of the InGaAs topography on the LEC substrate is much more inhomogeneous. This shows that the InGaAs layer on the LEC substrate has considerable lattice orientation variation. On the other hand, the InGaAs topography on the VCZ substrate has a homogeneous contrast. Therefore, VCZ crystals are preferable as substrates to obtain an InGaAs epitaxial layer with less lattice orientation variation.

The distribution of dark currents at $V_R=3V$ are shown in Fig. 5. Dark currents on the LEC substrate have a circular distribution. On the other hand, the distribution of dark currents on the VCZ substrate is homogeneous over the whole of the wafer except for the dot-like high
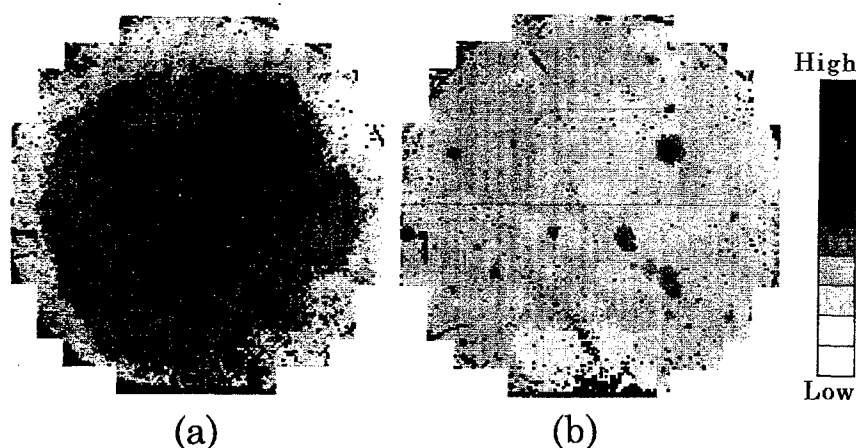
Fig.5 Dark current map of InGaAs PIN-PDs at V_R=3V
(a) on the LEC substrate, (b) on the VCZ substrate
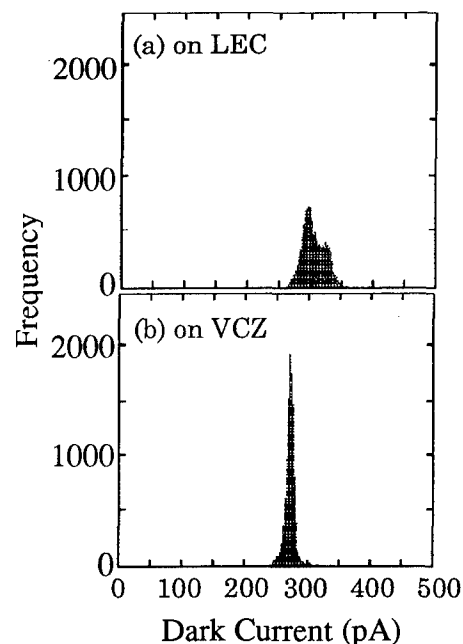
Fig. 6 Histograms of dark currents at V_R=3V

dark current region caused by anomaly during the wafer processing. The histograms of dark currents are shown in Fig. 6. The average of dark currents on the VCZ substrate is lower than that on the LEC substrate. Furthermore, the standard deviation of dark currents on the VCZ substrate is about half of that on the LEC substrate. We have already confirmed that dark currents at V_R=3V are dominated by the leak currents generated in the InGaAs layer. Therefore, lower average value and smaller standard deviation of dark currents on the VCZ substrate suggest that crystal quality of the InGaAs layer on the VCZ substrate is supe-rior to that on the LEC substrate.

Conclusion

3-inch diameter Fe-doped InP crystals grown by the VCZ method and the LEC method were compared from the viewpoint of long-wavelength optoelectronic device applications. First, crystal quality of InGaAs epitaxial layers grown by MOCVD on these substrates were studied by double crystal X-ray diffraction measurements. The average FWHM of rocking curves of the InGaAs layer on the VCZ substrate was narrower than that on the LEC substrate. Lattice orientation variation of the

InGaAs layer on the VCZ substrate was less than that on the LEC substrate.

Dark currents of InGaAs PIN-PDs fabricated on the VCZ substrate have smaller standard deviation than those fabricated on the LEC substrate. The average of dark currents on the VCZ substrate was also lower than that on the LEC substrate.

3-inch diameter Fe-doped InP crystals grown by the VCZ method is more favorable to the substrates for InGaAs PIN-PDs than those grown by the LEC method.

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High-Speed InAlAs/InGaAs HBTs on 4-inch S.I. GaAs Substrates

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Abstract

In this paper, we describe high-speed InAlAs/InGaAs HBTs on 4-inch S.I. GaAs substrates, which were made with constitutionally graded lattice-buffer layers and optimization of the epitaxial growth temperature. The use of these structures leads to excellent RF characteristics in spite of the thick base (200nm) and collector (600nm) of the HBTs. The maximum frequency (fmax) and the current gain cut-off frequency (ft) are 53GHz and 37GHz, respectively.

We achieved a delay time of 26ps for an ECL gate , which consists of 130 transistors, 150 resistors, and 10 capacitors on a 4-inch GaAs substrate.

I . Introduction

InAlAs/InGaAs HBTs, which are lattice-matched to the InP substrate, are better than AlGaAs/GaAs HBTs for ultra high-speed applications[1]. However, it is very difficult to obtain an InP substrate greater than 4inches, and the hetero band alignment is fixed only at the lattice-matched point.

The lattice-mismatched growth technology has been developed for forming the In(GaAl)As HEMTs structure on the S.I. GaAs substrate in the case of a thin epitaxial film[2],[3]. The RF and DC characteristics of InAlAs/InGaAs HBTs are closely related to the dislocation density which makes it difficult to fabricate InAlAs/InGaAs HBTs on S.I. GaAs substrates.

II. Crystal growth

We have fabricated InAlAs/InGaAs HBTs on 4-inch S.I. GaAs substrates by optimizing the epitaxial growth temperature.

Table 1   **Layer Structure**

Emitter Cap	n-InGaAs	$4\times10^{19}/cm^3$	120nm
	n-InAlAs	$1\times10^{19}/cm^3$	10nm
Emitter	n-InAlAs	$5\times10^{17}/cm^3$	75nm
Base	p-InGaAs	$1\times10^{19}/cm^3$	200nm
Collector	n-InGaAs	$5\times10^{16}/cm^3$	600nm
Subcollector	n-InGaAs	$1\times10^{19}/cm^3$	500nm
Buffer	$Al_{1-x}In_xAs$	undoped	$1\,\mu$ m
Substrate	GaAs	insulator	$600\,\mu$ m

Table 1 shows the layer structure of our InAlAs/InGaAs

HBT. All layers were grown by MBE at 400-430°C.

Si and Mg were used as n- and p-type dopants, respectively. For the base layer, in particular, the epitaxial
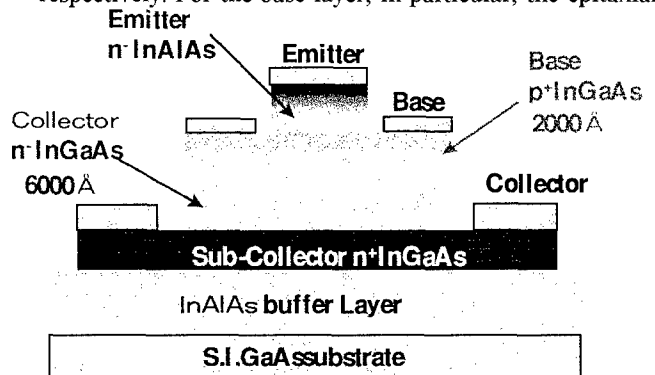
Figure 1   Cross sectional image of our HBT

growth was reduced to a rate of 2000Å to 3000Å/hour[4]. For the constitutionally graded lattice-buffer layers, we could obtain the optimal temperature of 400-430°C for the epitaxial growth experiment. At these temperatures, we obtained miller-like surface morphologies on top of the wafer surface, which had complete HBT epilayers.

Figure 1 shows the cross sectional image of our InAlAs/InGaAs HBT.

To fabricate our InAlAs/InGaAs HBTs, mesa etching was used for device isolation, and spin-on-glass for planarization. For the ohmic contacts, we employed a non alloy ohmic contact using a Pt/Ti/Pt/Au metal system and a highly doped InGaAs emitter cap layer.

III. DC characteristics

Figure 2 shows the common emitter I-V curves of our InAlAs/InGaAs HBT. The emitter area of the HBT, which was used in this measurement of the I-V curves, is 2.1x5.0 μ m^2. Figure 2 shows that we obtained 10~20 times of the DC current gain(hfe) on the 4-inch S. I. GaAs substrate. This value is the same as the value for a conventional high speed InAlAs/InGaAs HBT on the S. I. InP substrate. These current gain data show that we were able to exclude the influence of the dislocation by using constitutionally graded lattice-buffer layers.

On the other hand, we estimated the band gap discontinuity to be about 0.8 volts from the turn on voltages of the I-V curves. In conventional InAlAs/InGaAsHBT,
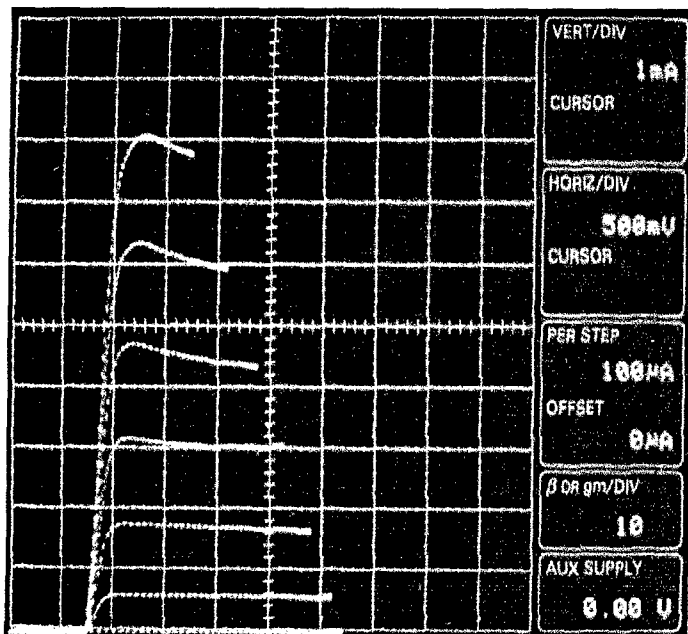
Figure2   Typical common emitter I-V characteristics of our InAlAs/InGaAs HBT on GaAs substrate (emitter area=2.1x5.0 μ m^2)

which are lattice-matched to the InP substrate, this value becomes 0.6 volts from 0.5 volts. For this result, our crystal mixing ratio for the epitaxial growth was shifted away from the point of lattice-matching with the InP substrate.

Moreover, this result shows that it is released from the lattice-matched point through the use of the constitutionally graded lattice-buffer layers process and that it is possible to do a band design freely.

IV. RF characteristics
The s-parameter was measured using an HP 8510C vector network analyzer and Cascade microtech WPH series coplanar waveguide probing heads. The emitter area of the HBT used for this RF measurement is 2.1x5.0 μ m^2.
We obtained the maximum frequency (fmax) and the

current gain cut-off frequency (ft) of up to 53GHz and 37GHz, respectively, in spite of the thick base (200nm) and collector (600nm).

This efficiency is better than the conventional InAlAs/InGaAs HBT which was lattice-matched to the InP substrate..
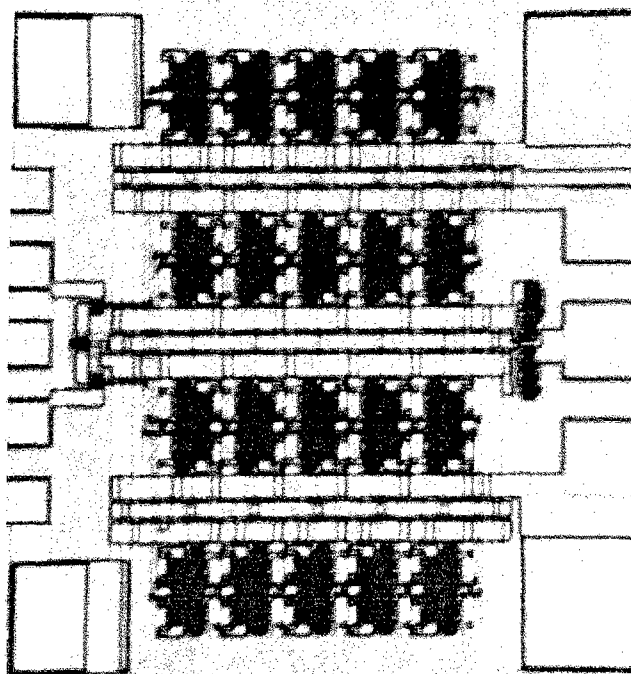
Figure 3   Photograph of our InAlGaAS/InGaAs HBT ECL ring OSC which consists of about 290 elements (size=0.8x1.0mm^2).

V. Ring oscillator
It is possible to be used in evaluate whether our InAlAs/InGaAs HBT can be used in the experimental production of the MSI level IC in making ECL gate ring oscillator and evaluating the yield. We use these HBTs on the 4-inch S.I. GaAs substrates in the design of the ECL gate ring OSC, which consists of 140 transistors, 150 resistors, and 10 capacitors. For MIM capacitors, sputtered Ta_2O_5 is used. For thin film resistors, reactive sputtered Ta_2N is used. Figure 3 shows the ECL gate ring-OSC. We achieved an ECL gate delay time of 26ps.

Figure 4 shows a typical output waveform of our InAlAs/InGaAs HBT on a 4-inch S. I. GaAs substrate.
For this trail fabrication of a ECL ring OSC IC, we obtained a 80% yield. This result shows that there is ability
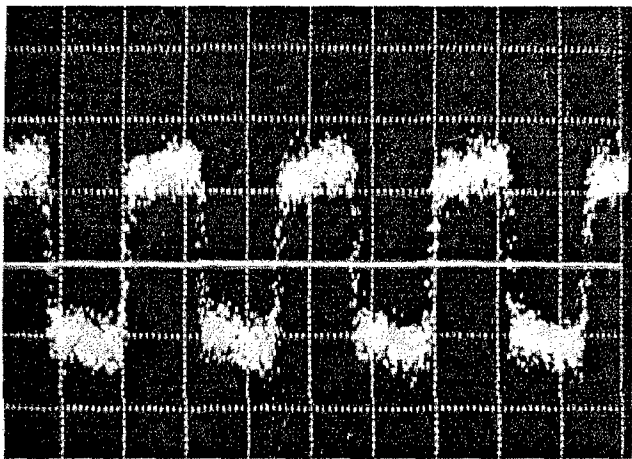
Figure 4 Typical output Waveform of our InAlAs/InGaAs
HBT ECL ring OSC on the GaAs substrate.

for the IC to be able to be sufficiently manufactured about
this constitutionally graded lattice-buffer layers process .

VI. Conclusion

We obtained high-speed InAlAs/InGaAs HBTs on 4-
inch S.I. GaAs substrates, which were made with
constitutionally graded lattice-buffer layers, and achieved
optimization of the epitaxial growth temperature. The use
of these structures leads to excellent RF characteristics in
spite of the thick base (200nm) and collector (600nm) of
the HBTs. The maximum frequency (fmax) and the current
gain cut-off frequency (ft) are 53GHz and 37GHz,
respectively.

We achieved a delay time of 26ps for an ECL gate which
consists of 130 transistors, 150 resistors, and 10 capacitors
on a 4-inch GaAs substrate.

We are now investigating to reduce the base and
collector thickness, which may enable frequencies up to
several hundreds GHz to be obtained.

Moreover, it is experimentally making the ballistic
trajectory electron orbit transistor proposed by us[5].

VII. Acknowledgment

The authors would like to thank   Dr. Hisao Nakamura,
Mr. Haruo Hosomatsu, and Mr. Yukihiro Matsuura for
their   support   with   their   encouraging   discussions
throughout this study.

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The Effects of InAlAs Strained-Superlattice Barriers Upon the Properties of InGaAlAs/InP Quantum Wells and Double Heterostructures

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OBJECTIVES: In comparison to the InGaAsP/InP system which has been the conventional materials system employed in long-wavelength lasers, the InGaAlAs/InAlAs/InP system has been relatively less studied. There are several advantages to using the InGaAlAs system. The conduction band offset between InAlAs and InGaAs is large ($\Delta E_c = 0.72 \Delta E_g$) and the bandgap of both unstrained and compressive/tensile-strained InGaAlAs, grown on InP can be adjusted to emit light in the range 1.3 μm to 1.55 μm which is important for optical fiber communications. Furthermore, the band offset is larger in the conduction band than in the valence band for InGaAs/InGaAlAs, in contrast to the case of InGaAs/InGaAsP. However, a complete study of the effects of tensile and compressive strain in quantum wells and the growth of superlattices in the InGaAlAs system has not been published.

APPROACH: In this paper, we investigate the growth of lattice-matched and strained InGaAlAs/InP heterostructures by metalorganic chemical vapor deposition (MOCVD) and the design and characterization of strained-superlattice barriers (SSLB's) to enhance the electron confinement in the InGaAlAs/InP system and study the effect of such barriers on the PL emission from InGaAlAs active regions, as well as to study the effect on devices.

RESULTS: To test the efficacy of the SSLB, for comparison purposes, two structures are compared using PL measurements, one utilizing SSLB's and the other having only conventional bulk InAlAs barriers. The SSLB test structure was grown in an EMCORE GS3200 reactor by LP-MOCVD on an InP:S substrate as follows: (1) InP buffer layer; (2) 250nm lattice-matched InAlAs cladding layer; (3) SSLB layers; (4) InGaAlAs ($\lambda \sim 1.3$ μm) QW or DH "active region"; (5) SSLB layers; (6) 250nm InAlAs cladding; (7) 10nm InP cap layer. The "standard" DH wafer was grown in the same MOCVD reactor using the same sources but employed thicker "bulk" InAlAs lattice-matched cladding layers adjacent to the active region. The structures are unintentionally doped.

The relative luminescence efficiency of these structures is evaluated by PL measurements. Figure 1 shows the 300K PL spectra for the bulk-barrier and the SSLB structure. The SSLB structure shows an increase of up to seven times in the PL intensity from the InGaAlAs active region. The increase may be due to the increased carrier confinement in the active region as a result of the SSLB and indicates the superior carrier confinement capabilities of the SSLB. An increase is also seen in PL measurements at 4K although the increase is much smaller than that observed at room temperature. This is expected because the primary loss of carriers from the active region to the cladding layer occurs by thermalization. At 4K, the loss of carriers in the bulk barrier sample is much smaller than at room temperature. Therefore, the effect of the SSLB is more evident at room-temperature where it provides a higher potential barrier to the carrier loss via thermalization. Figure 2 shows the difference in the relative 300K PL intensities from the bulk barrier and the SSLB structure as a function of laser pump power.

We have also investigated the effect of the growth temperature, T_g, and AsH$_3$ purity upon the characteristics of these SSLB QW's. The influence of T_g on the PL properties of Al-containing compounds is dramatic, as shown in Figure 3. The level of O$_2$ incorporation in the material is reduced as the growth temperature is increased, as determined by SIMS measurements. Even though the Al content of the InGaAlAs active region is smaller than the higher Al content of the InAlAs clad means that there could be a significantly higher oxygen concentration in the InAlAs barriers. Tunneling of the confined carriers in the active layers to the nonradiative centers in the InAlAs cladding layer can reduce the radiative efficiency of the active region. There is an optimum T_g above which PL intensity decreases. We also observe an improvement in the 300K PL intensity for wafers grown using an AsH$_3$ purifier, as shown in Figure 4. The design and growth of optimized SSLB's, their role in improving the performance of InGaAlAs/InP luminescence, and the characteristics of devices employing these barriers will be presented in this paper.
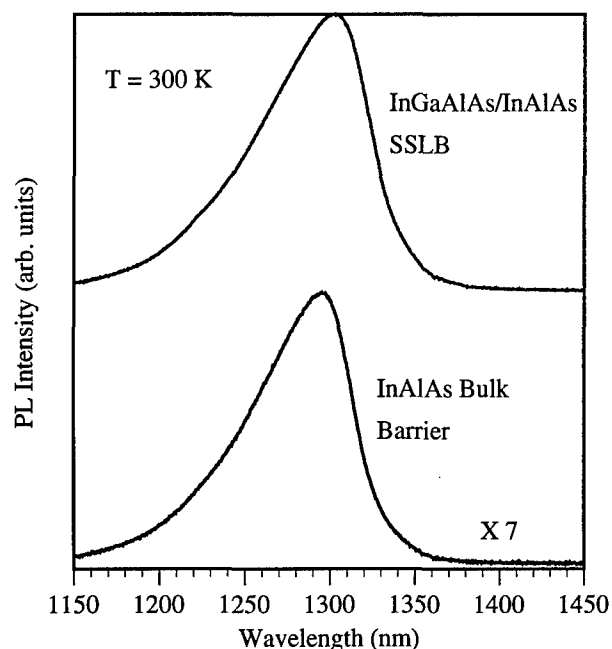
Figures:

Figure 1: PL spectra for InGaAlAs DH samples with (a) SSLB's; (b) bulk barriers.
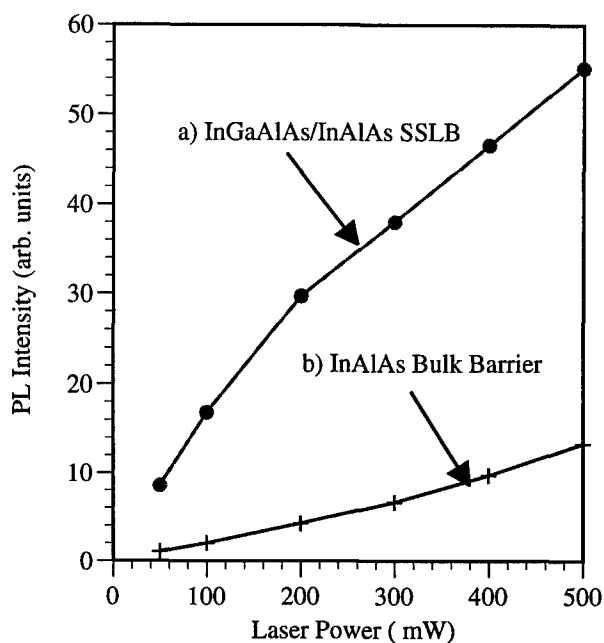

Figure 2: PL intensity vs. excitation power for InGaAlAs DH with (a) SSLB's; (b) bulk barriers
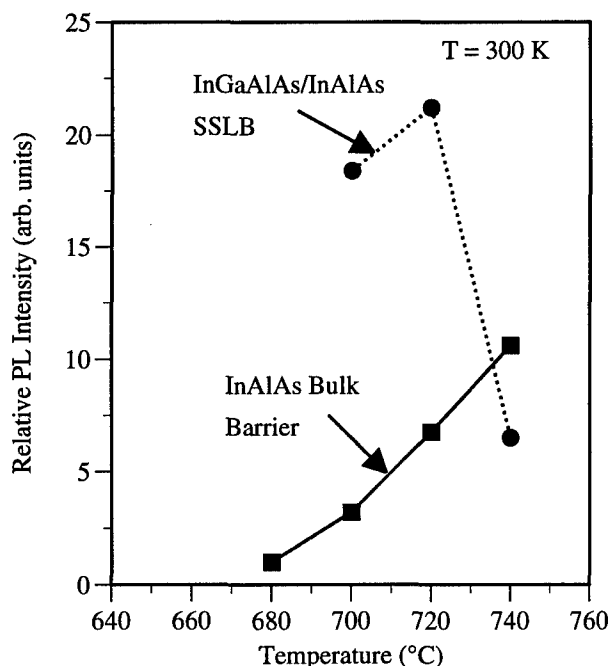
Figure 3: PL intensity vs. growth temperature for InGaAlAs DH samples with SSLB and bulk barriers.
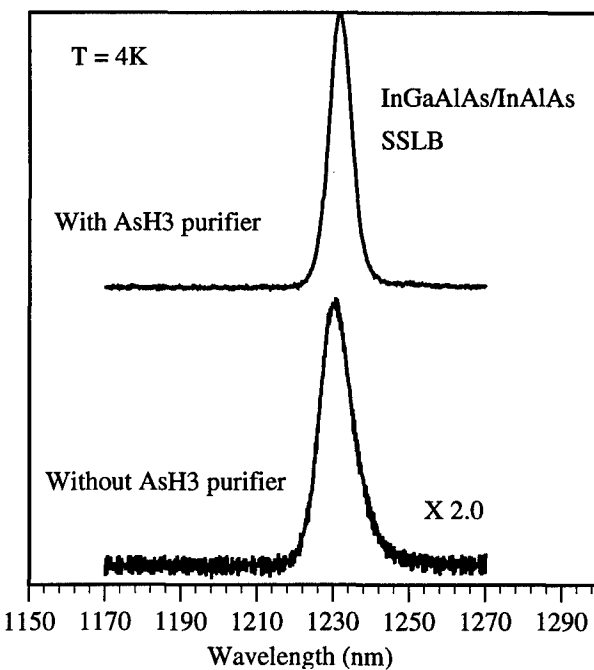
Figure 4: 4K PL comparison of InGaAlAs SSLB sample growth with and without AsH_3 purification.

STRAIN COMPENSATED GaInAs/AlInAs TUNNELLING BARRIER MD6 MQW STRUCTURE FOR POLARISATION INDEPENDENT OPTICAL SWITCHING

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Introduction

Large electro-optic modulation is available in InP based photonic devices for communication systems working in the 1.55 μm window. This is because the quantum confined Stark effect (QCSE) can be exploited to switch and modulate the light wave. But signal processing in the receiver front end often has to be polarisation independent. However, the QCSE proves to be inherently polarisation dependent. In the present work this problem was tackled by applying a tunnelling barrier QW (TBQW) structure. This concept was reported recently for the GaAs material system [1] and is transferred here to InP based devices for the first time. Its realisation necessitates to optimise the electrical, optical and structural material quality in order to make it suitable for device applications. First the investigations concerning the epitaxial growth conditions are described. Then the experimental results for TBQW structures are reported, including the polarisation independent electro-absorption characteristics of Mach-Zehnder interferometers (MZI) incorporating strained TBQWs. Such a MZI switch is the basic building block of a high speed time division demultiplexer (DEMUX). The development of the DEMUX is a part of the European ACTS HIGHWAY project.

I. Design

TM polarised light propagating in InP based waveguides interacts with light holes (LHs) only whereas TE polarised light mainly with heavy holes (HHs) [2]. Consequently it is necessary to match the energy for heavy and light hole transitions to obtain a polarisation independent phase shift in switching devices exploiting the QCSE. A degradation of LH and HH energy levels in InP based materials is obtained by

Fig. 1: Band diagram of tensile strained (-0.54 %) QW structure with thin tunnelling barriers. The different wavefunctions and confinements for light and heavy holes can clearly be identified.

introducing tensile strain. But applying an electric field an additional bandgap shift is resulting [1]:

$$\Delta E_{LH/HH} = - C\, m_{LH/HH}{}^*\, F^2\, L_{LH/HH}{}^4, \qquad (1)$$

where C is a constant, $m_{LH/HH}{}^*$ the effective mass and $L_{LH/HH}$ the effective QW thickness of LH and HH, respectively, and F the applied electric field. ΔE also has to be made equal for LHs and HHs.

If introducing two thin extension QWs in each period, each of them separated from the central QW by a very thin tunnelling barrier, a different confinement of HHs and LHs is resulting (Fig. 1). Now different effective well widths L_{HH} and L_{LH}, respectively, are existing. Provided the condition

$$m^*_{HH}\, L^4_{HH} = m^*_{LH}\, L^4_{LH} \qquad (2)$$

is satisfied [1] the degradation of LHs and HHs is still holding, irrespective of the strength of the applied electric field.

The complete design of the investigated TBQW structures was performed with a numerical program which uses the deformation potentials of strained QWs to calculate wavefunctions and energies of electrons and holes (see Fig. 1). The resulting TBQW geometry comprises extension well, tunnelling barrier, and central well with a width of 2 nm, 1.5 nm, and 8.5 nm, respectively. Thus HHs occupy a QW of 8.5 nm effective thickness and LHs of 15.5 nm. Especially the growth of the tunnelling barriers represents a challenge for epitaxy.

II. Experimental

All samples were grown in a low pressure MOVPE system at 20 mbar total pressure. A gas foil rotation susceptor is applied. The growth temperature in the range between 625 °C and 775 °C is monitored inside the susceptor body. 100 % 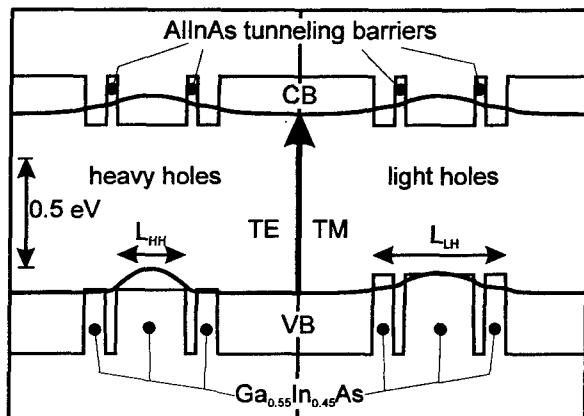pure arsine and phosphine were used as sources for the group V elements whereas the sources for aluminium, gallium and indium consisted of the respective trimethyl (TM-) compounds. Monosilan and dimethyl-zinc were used for n- and p-doping. The growth rate for AlInAs and GaInAs was kept at 0.6 μm/h and 1.1 μm/h, respectively. The doping concentrations in AlInAs are investigated with C-V-measurements to achieve reliable results. Hall measurements are not suitable since then oxygen donors are not excited [3]. The X-ray diffraction (XRD) measurements are performed with a double crystal diffractometer.

III. Optimisation of MQW material

A. Background and procedure

GaInAs QWs are preferentially combined with AlInAs rather than InP barriers. Then extremely sharp heterointerfaces can be grown since only one group V element is present. This is essential for the controlled growth of the minute details of the TBQW structure used in this work. This advantage is contrasted by the well known problem of oxygen incorporation in Al containing material.

A strong interaction of the light wave with the applied electric field needs extensive pn junctions. Only then the overlap between electric and optical field is sufficiently high. Therefore material of low background doping is required.

Bulk GaInAs and AlInAs layers as well as QW structures with five periods of 8 nm GaInAs wells and 50 nm AlInAs barriers were grown under different conditions. Then the samples were characterised by means of C-V-measurements. The effective carrier concentration within the structure can be deduced from the measured dependence of the capacitance per area on the applied voltage.

In case of the QW structures a detailed simulation of carrier distributions was done based on a self-consistent solution of Poisson's and Schrödinger's equation. Comparing the experimental and theoretical results the existing background doping level in the QW structure is then deduced.

B. Starting point:

Fig. 2 shows the effective carrier density distribution in a MQW of five AlInAs/GaInAs periods, calculated from the C-V-measurements. It illustrates the background doping level before optimisation of the material quality. A sequence of five peaks each separated by a flat floor can be observed. Peaks and floors can be identified as the individual QWs and barriers, respectively. Obviously carriers originating in the barrier
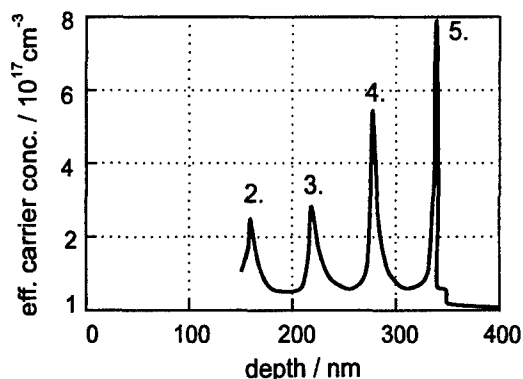
Fig. 2: Effective carrier density distribution in an AlInAs/GaInAs MQW structure as determined by C-V-measurements, before optimisation of epitaxial growth.

material are trapped within the QW. In the analysis of these data the experimental and theoretical results can be reconciled only if a background doping of around $7 \cdot 10^{16}$ cm^{-3} is assumed in the AlInAs layers. This value is too high for device applications.

C. Source material quality and growth parameters

Oxygen and silicon have to be considered as the relevant impurities in this context. The impurity incorporation is known to strongly depend on the purity of the MO sources as well as on the MOVPE growth parameters [4, 5]. Provided a leak tight growth system is used, the sources for oxygen are not only the TM-Al or arsine as often reported but also to a large extend the TM-In compound [6, 7]. A high V/III ratio $r_{V/III}$ (>200) helps to reduce the oxygen incorporation into the AlInAs material [5].

Therefore the first step to achieve low background doping levels was to exchange the source materials and to optimise $r_{V/III}$. The TBQW structures in our work were grown with $r_{V/III} = 290$.

D. Investigation of temperature dependence

The growth temperature T_{growth} is one of the key parameters for the MOVPE growth of AlInAs. It strongly influences morphology, background doping and optical properties [4, 7].

For this investigation T_{growth} was varied from 625 °C to 775 °C. All other parameters are kept constant. Four bulk AlInAs layers subsequently grown in one run, each layer at a different value of T_{growth}, served for the determination of the dependence of the background doping levels on T_{growth}. The relationship between photoluminescence (PL-) intensities and T_{growth} is evaluated with individually grown bulk AlInAs layers.

Fig. 3 depicts the measured influence of growth temperature variations. The background doping level decreases to a
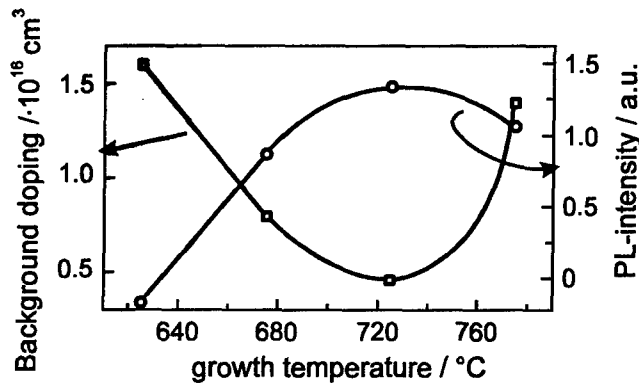
Fig. 3: Dependence of PL-intensity and carrier concentration in bulk AlInAs layers on growth temperature.

minimum of $2...3 \cdot 10^{15}$ cm^{-3} if T_{growth} rises to 725 °C. Above this temperature the carrier concentration increases anew. The PL-intensity exhibits a maximum again with samples grown at 725 °C, indicating that the best material quality is also obtained with this value of T_{growth}. Both results agree with the assumption that oxygen incorporation diminishes while increasing the growth temperature up to around 725 °C. Then the kinetics of the impurity incorporation changes and another dopant (probably silicon) becomes more dominant.

The structural quality of tensile strained TBQWs was evaluated by XRD techniques. Its growth temperature dependence is shown in Fig. 4. The X-ray satellite peak pattern with the best resolution and the lowest half width is also obtained at a growth temperature of 725 °C. At higher values the spectrum indicates a stronger degradation of the structure.

E. Results with optimised growth conditions:

After exchanging the arsine and TM-Al sources in combination with optimised growth conditions ($T = 725$ °C, $r_{V/III} = 290$) the background doping level of AlInAs and of GaInAs could be reduced to $N_D\text{-}N_A = 2...3 \cdot 10^{15}$ cm^{-3} and $N_D\text{-}N_A = 3...5 \cdot 10^{14}$ cm^{-3}, respectively (C-V-measurements). At this doping level the electric field extends far into the crystal. Therefore C-V-measurements of AlInAs/GaInAs MQW structures corresponding to Fig. 2 are not possible then, the MQW structure is not resolved.

In Fig. 5 the X-ray satellite peak pattern of a ten period strain compensated (2+1.5+8.5+1.5+2) nm TBQW structure grown under optimised conditions is compared with a simulation based on the parameters displayed in the Table. A very good agreement within an accuracy of about one atomic layer is found.

AlInAs	(+0.32 %)	17 nm
GaInAs	(-0.52 %)	2 nm
AlInAs	(+0.32 %)	1.5 nm
GaInAs	(-0.52 %)	8.5 nm
AlInAs	(+0.32 %)	1.5 nm
GaInAs	(-0.52 %)	2 nm

} 10 periods

Fig 4: XDR spectra of TBQW layers, influence of T_{growth}. 5 periods of TBQWs, width of extension well / tunnelling barrier / central well: 2 nm / 1.5 nm / 8.5 nm, GaInAs wells tensile strained (-0.54 %), AlInAs barriers grown lattice matched.

Fig. 5: Comparison between simulated and measured XRD spectra for TBQW layers as given in the table.

IV. Performance of switching devices

TBQW layer sequences with varied strain and geometrical parameters were grown under optimised conditions. The TBQWs are sandwiched between two 60 nm thick GaInAsP layers ($\lambda_g = 1.3\,\mu$m) to increase the optical confinement and imbedded in InP (on top 200 nm thick). This stack served as waveguide core in a Mach-Zehnder interferometer. On top of the core layers an 800 nm thick InP layer and a 200 nm thick p-contact layer were grown, both etched to form the 2.5 μm wide waveguide rib. The doping profile in the epitaxial layers was designed to build a pin-diode. Evaporated films of Ti/Pt/Au served as rib etching mask and contact metallization simultaneously.

Fig. 6a and Fig. 6b depict the light transmission through a 4 mm long MZI as a function of the applied voltage and light polarisation at $\lambda = 1550$ nm. Both MZI devices are fabricated with TBQW structures which are grown with the same geometrical parameters but with different tensile strain incorporated into the QWs, 10 periods of (2.2+1.5+9.3+1.5+2.2) nm TBQWs tensile strained with -0.32 % and -0.45 %, respectively, and separated by 17 nm strain compensated AlInAs.
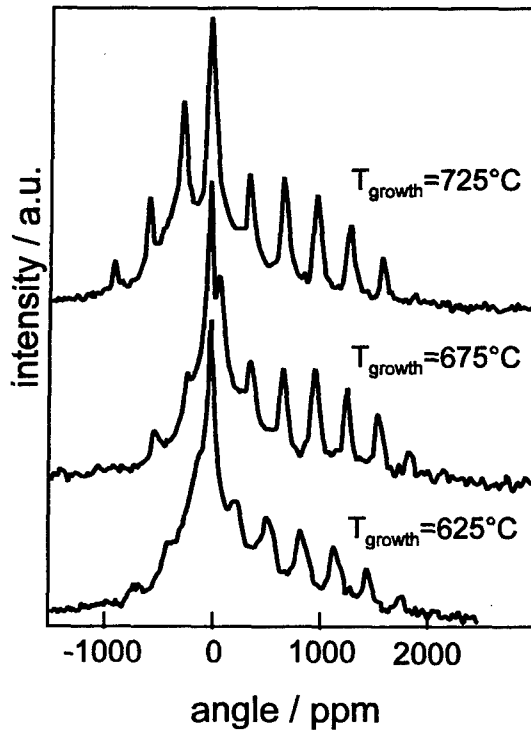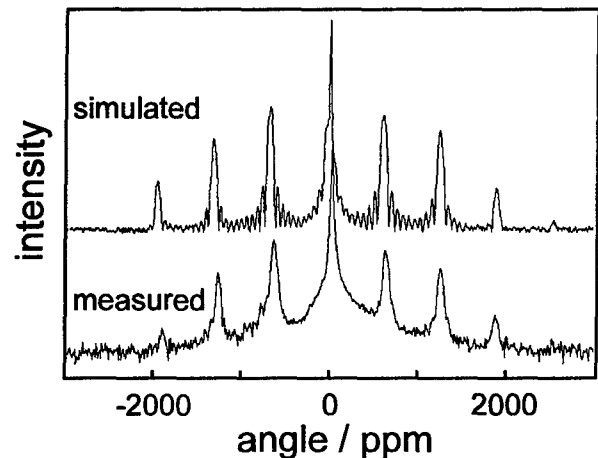
With a strain of -0.45 % the electro-absorption characteristics for TE and TM are not coinciding. But with a strain of -0.32 % there is virtually no deviation in the switching voltage of the MZI between the two polarisations. For both an extinction better than -15 dB is observed at -5 V simultaneously. The TM mode is suppressed more weakly because a second order mode is excited in the waveguide. By altering the waveguide design this can be prevented and accordingly the TM extinction ratio can be improved.

V. Conclusions

The concept of tunnelling barrier QW structures has been reviewed and investigated for InP based switching devices. It is used to exploit the quantum confined Stark effect in a polarisation independent device architecture. The evaluation of optimised growth conditions for AlInAs/GaInAs TBWQ structures has been described. By means of a fine tuning of all structural TBQW parameters a perfect matching of the switching voltages for TE and TM can be achieved simultaneously. Thus the validity of the proposed TBQW concept is clearly demonstrated.

Fig. 6: Switching characteristics of a 4 mm long MZI for TE and TM polarisation at $\lambda = 1550$ nm. 10 periods of (2.2+1.5+9.3+1.5+2.2) nm TBQWs, 17 nm AlInAs compressively strained (+0.18%) barriers.
a: QWs tensile strained with -0.45 %.
b: QWs tensile strained with -0.32 %.

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Anisotropic Polarization Properties of GaInAsP/InP Compressively-Strained Quantum-Wire Structure

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Abstract

Polarization dependence of 1.55μm wavelength GaInAsP/InP compressively-strained (CS) quantum-wire laser structures assisted by a quantum-film was measured and compared with quantum-film laser structures fabricated on the same wafer. As a result, better anisotropic polarization properties of the quantum-wire structure were obtained. PL intensity of an electric field perpendicular to the quantum-wire (Q-Wire) was about 60% of that parallel to the Q-Wire. In addition, we fabricated Q-Wire lasers with a wire width of about 25nm. As a result, a blue shift $\Delta E \sim 10meV$ and a threshold current density $J_{th}=34A/cm^2$ at 90K were obtained.

I. Introduction

To realize giga-bit transmission systems by optical interconnection between broad-bandwidth optical fiber communication systems and opto-electronic integrated circuits (OEICs), high performance of semiconductor lasers is required. This can be realized by means of introducing quantum wires (boxes) as an active region for high optical gain due to the increase of carrier concentration in these structures.[1-4] Now-a-days, much work has been done in order to fabricate such devices with low dimensional quantum structures.[5-11] For the position and size controllability of quantum wires (Q-Wires) and for a simple technology transfer to quantum box- (Q-Box) or DFB-structures, we have been investigating GaInAsP/InP Q-Wire lasers fabricated by electron-beam (EB) lithography and an etching technique followed by an organic metal vapor phase epitaxy (OMVPE) embedding growth[12-13]. In this work, we discuss the polarization dependence of the Q-Wire structure and compare it with that of the quantum-film (Q-Film) structure fabricated on the same wafer. In addition, we investigate the temperature dependence of the Q-Wire lasers.

II. Experiment

It is important to fabricate high density and highly uniform nano structures for the realization of a high performance operation of Q-Wire (-Box) lasers. Our EBX system (JEOL JBX-5FE) has a very small size fluctuation with a standard deviation of approximately 1.1nm for a period of 50nm.[14]

Figure 1 shows the cross sectional SEM view and the band profile of the Q-Wire structure. The Q-Wire structure was fabricated on a wafer consisting of a 10nm thick $Ga_{0.18}In_{0.82}As_{0.73}P_{0.27}$ compressively-strained (1%-CS) quantum-well grown on (100) p-InP substrate by making a 70nm-period line pattern with an area of $1 \times 1mm^2$. The wire pattern formed by JBX-5FE EBX system using ZEP-520 resist (30nm thick) with a line dose condition of 0.8nC/cm. After transferring the pattern into the wafer using a SiO_2 etching mask, this mask was
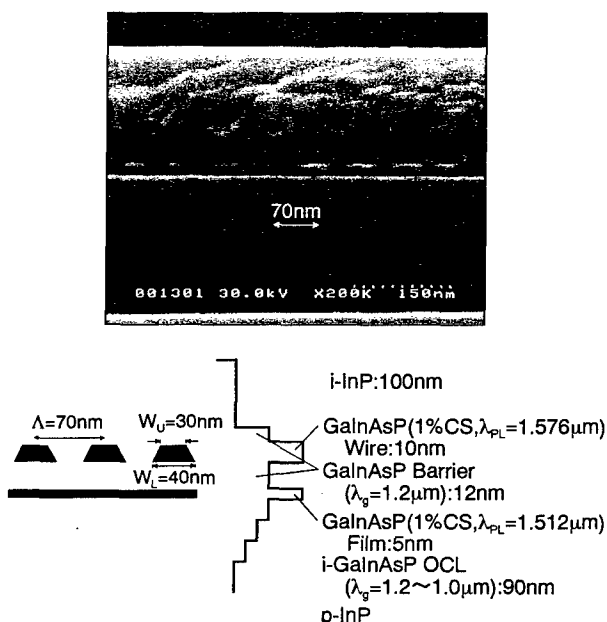
Fig.1 Cross sectional SEM view and band profile of Q-Wire structure.
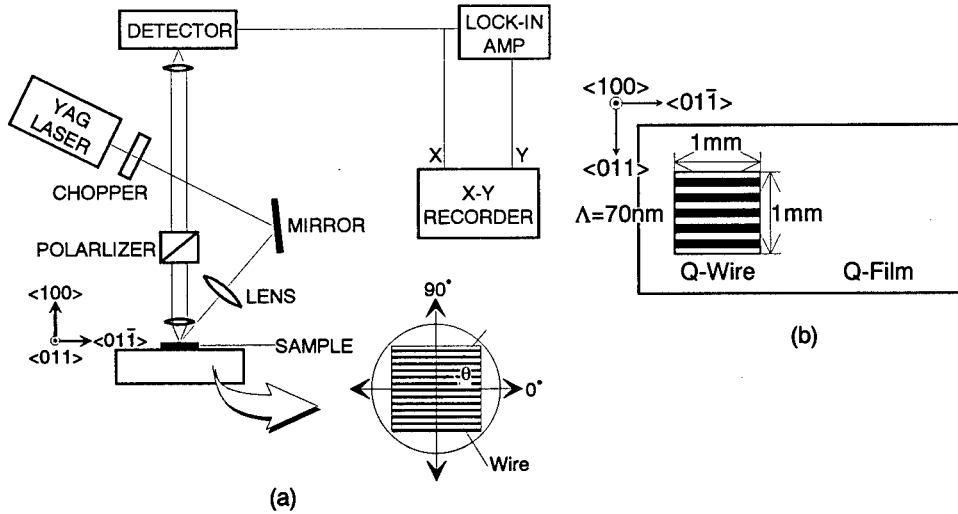
Fig. 2 (a) Photoluminescence measurement system.
(b) Sample for measurement.

removed and the Q-Wire structure was embedded in 100nm thick InP layer. To fabricate Q-Wire structures with an average width $W = (W_u + W_L)/2 = 35nm$, we used two types of etchant; one was 40ppm (volume ratio) Br-methanol for mesa-etching, and the other was $H_2SO_4:H_2O_2:H_2O$ =1:1:10 (0°C) for side etching.

Figure 2 shows (a) the experimental setup for photoluminescence (PL) measurements and (b) the sample for measurement. The sample was excited by a Nd-YAG laser (λ=1.064μm, 20mW) through a chopper. The direction of the quantum-wire was along $< 01\bar{1} >$ and the luminescence was collected from the top surface (<100> direction) by a Ge detector through a polarizer.

Then we fabricated Q-Wire lasers on a different initial wafer. The Q-wire width was around 25nm which was embedded by a thin (3nm) InP layer, GaInAsP optical confinement layer (OCL), n-InP cladding layer, and n-GaInAs contact layer. Finally 15mm wide mesa-structure stripe lasers were fabricated.

III. Results and Discussion

A. PL characteristics

The optical transition strength is given as follows;[15]

$$\langle R_{cv}^2 \rangle = a|R^2| .$$

Here a is the coupling coefficient between dipole moment and light field, and $|R^2|$ is the magnitude of dipole moment. For heavy hole band, a is given by

$$a = 1 - |\bar{k} \cdot \bar{e}|^2 ,$$

where $\bar{k}$ and $\bar{e}$ are unit vectors directed along electron wave vector and electric field of light propagation, respectively.[16] Under the assumption of $k \propto 1/W_x, 1/W_y$, where W_x and W_y are the wire width and the well thickness of the Q-Wire, respectively, $\bar{k}$ vectors are
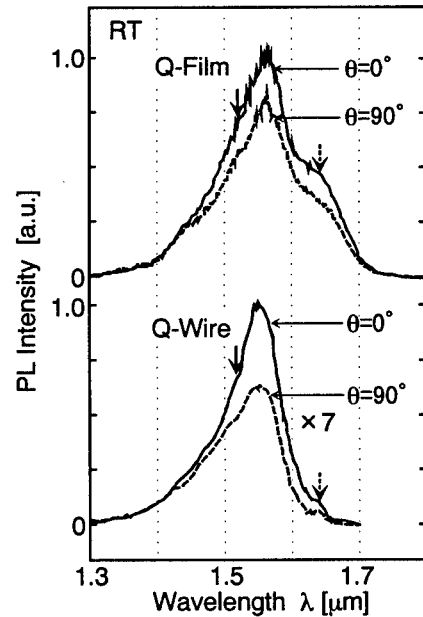
Fig. 3 Polarization properties of the PL spectrum of Q-Wire structures compared with Q-Film at room temperature.

$$\bar{k} = \left(\frac{r}{\sqrt{1+r^2}}, 0, \frac{1}{\sqrt{1+r^2}} \right) .$$

Here r is the aspect ratio of Q-Wire defined as W_y/W_x. Therefore the coupling coefficient a for TE polarization considering the direction of the luminescence from the top surface is

$$a = 1 - \frac{r^2}{1+r^2} \sin^2 \theta ,$$

where θ is the angle between wire-axis and electric field. The smaller r becomes, the coupling coefficient is like Q-Film's. On the other hand, in case of large r, the lateral confinement is strong.

Figure 3 shows the polarization properties of the PL

227

spectrum of the Q-Wire and the Q-Film structure at room temperature. Solid-line arrow marks at 1.51μm indicate the peak of the lower quantum-film and the dashed-line arrow marks at 1.64μm indicate the peak due to an As-rich layer, formed during the growth of the initial wafer. This layer was considered to be located above the upper quantum-film layer, because the intensity was reduced in case of Q-Wire's spectrum. The FWHM at θ=0° and at θ=90° for the Q-Wire were 43meV and 58meV, respectively, and that of the Q-Film was constant, i.e., 57meV. The difference of them was dependent on polarization, because at θ=0° the contribution of the

Fig. 5 Temperature dependence of Normalized PL intensity and FWHM of Q-Wire.

Fig. 4 Polarization dependence of Normalized PL intensity at room temperature.

Fig. 6 Temperature dependence of PL peak wavelength.

lower quantum film peak to the FWHM of the Q-Wire is small. The energy value of blue shift for the Q-Wire was estimated to be about 8meV, which is a reasonable value compared with the quantum-wire size of SEM view in Fig. 1.

The polarization dependence of the PL intensity of the Q-Wire at room temperature is shown in Fig. 4, compared with that of the Q-Film. Here, the direction of the angle θ=0° is along $< 01\bar{1} >$ and θ=90° is along <011>. The PL intensity at each measured point was normalized by the intensity at θ=0°. As can be seen, the PL intensity at θ=0°, which is parallel to the direction of the quantum-wire, was maximal and at θ=90°, which is perpendicular to the quantum-wire orientation, was minimal. The variation in intensity of Q-Wire is larger than that of Q-Film, i.e., 0.63 for Q-Wire and 0.87 for Q-Film. The difference was caused by the two-dimensional size effect based on the anisotropic behavior of the dipole moment in quantum wires. Dashed lines show the calculated value of coupling coefficient. In case of $r=w_y/w_x=0.29$, which corresponds to $w_x=35nm$ and $w_y=10nm$, the measured polarization dependence was much stronger than the theoretical curve. It is rather near in case of r=0.77.

We also measured the temperature dependence of the PL signal of the Q-Wire. Figure 5 shows the temperature dependence of the PL intensity. The PL intensity at each measured temperature was normalized to

the intensity at T=90K. Although the intensity of the Q-Wire was only about 14% of that of the Q-Film at room temperature, it became 80% at 90K. Considering the space filling factor of the quantum-wire structure, which is 0.5, the Q-Wire's PL intensity was 1.6 times larger than the Q-Film's intensity. The reason for this is considered due to an efficient carrier collection in quantum wires and a low damage fabrication process. Figure 6 shows the temperature dependence of PL peak wavelength of the Q-Wire compared to the Q-Film. Both temperature coefficients of the PL peak wavelength in the Q-Wire and the Q-Film were about the same (0.5nm/deg).

B. Lasing properties

Figure 7 shows the temperature dependence of the threshold current density (J_{th}) of the Q-Wire laser and the initial Q-Film laser. Although J_{th} of the Q-Wire laser showed a poor characteristic temperature ($T_0=137K$ for T<150K, $T_0=37K$ for T>150K) which can be attributed to carrier overflow in the OCL, lower threshold current (I_{th}) compared with Q-Film laser was obtained at T<170K. At T=90K, $I_{th}\approx5.5mA$ ($J_{th}=34A/cm^2$) under pulsed condition, and $I_{th}=6mA$ ($J_{th}=37A/cm^2$) under CW condition, were obtained for Q-Wire laser while those of Q-Film laser were $I_{th}=11mA$ (pulse, $J_{th}=68A/cm^2$) and $I_{th}=12mA$ (CW, $J_{th}=74A/cm^2$).

Figure 8 shows the temperature dependence of the lasing wavelength of these two lasers. The temperature coefficients of them were almost the same, about

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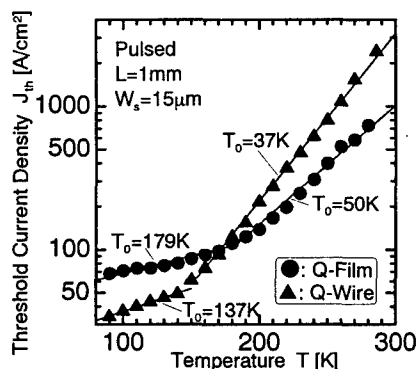
Fig. 7 Temperature dependence of threshold current density.
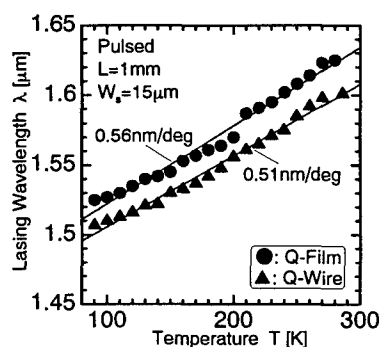
Fig. 8 Temperature dependence of lasing wavelength.

0.5nm/deg. Lasing wavelength of the Q-Wire laser was 1.601μm and that of the Q-Film laser was 1.625μm at room temperature. The value of the blue shift for the Q-Wire laser compared to the Q-Film laser was estimated to be about 11meV.

IV. Conclusion

In conclusion, an isotropic polarization of the PL signal was observed in GaInAsP/InP quantum-wire structures with relatively wide ($\overline{W}$ = 35nm) wire-size. PL intensity of an electric field perpendicular to the quantum-wire (Q-Wire) was about 60% of that parallel to the Q-Wire. In addition, the lasing characteristics of the Q-Wire laser ($\overline{W}$ = 25nm) was measured. As a result, a blue shift $\Delta E \sim 10$meV and a threshold current density $J_{th}=34$A/cm^2 at 90K were obtained.

Acknowledgment

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Tuesday
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Impact on InP-based ICs on Future Lightwave Communications Systems

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Abstract

Fiber-optic communications systems based on InP based photonic and electronic circuits will play a key role in establishing broadband network services. Single carrier and multi-carrier systems with beyond 10 Gbit/s capacity have been installed into commercial networks and new technologies can boost them into 1 Tera-bit/s world. This transmission capability is based on high-speed circuit technology and optical amplifier technology. It is important to utilize digital transmission technology based on electronic circuits from the view point of operation and maintenance administration, so a critical question is how fast can electronic circuits operate.

This paper describes recent progress in InP IC technology and presents a demonstration of a 40 Gbit/s, 320 km optical transmission experiment using these ICs. We also show the limitations of and solutions for a single-carrier system with speeds of 40 Gbit/s or more.

Introduction

Fiber-optic communications systems which will be based on InP based photonic and electronic circuits to form the network needed for broadband services. Single carrier and multi-carrier systems with beyond 10 Gbit/s capacity have been installed into commercial networks [1] and new technologies can lift this rate to 1 Tera-bit/s as shown in Fig.1. This requires the use of high-speed circuit technology and optical amplifier technology. It is important to effectively utilize digital transmission technology based on electronic circuits from the view point of operation and maintenance administration, so the question is how fast can electronics circuit operate. Next question is how high speed circuits are accommodated in equipment.
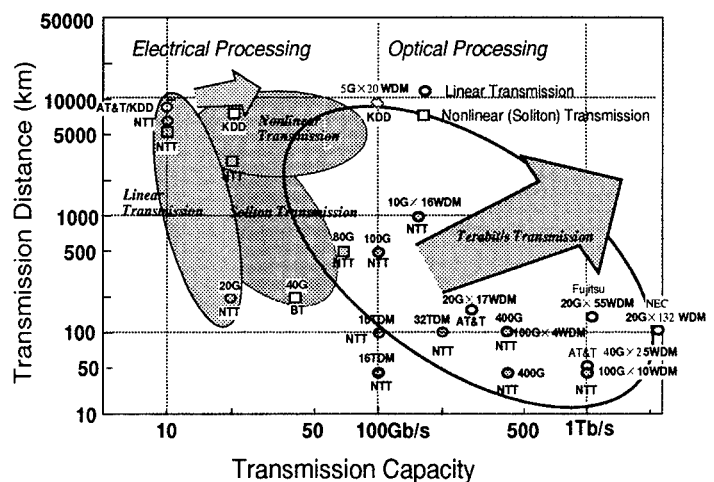
Fig. 1 Progress of Transmission Capability

System Design

A single carrier 10-Gbit/s system has been installed into commercial networks and WDM technology will enhance its transmission capacity. TDM technology provides economical and easy maintenance due to its digital signal processing based on LSI technology. However, it is necessary to overcome two major problems in order to develop high-speed TDM transmission systems: maximizing the speed of electrical and photonic circuits and the other is how to accommodate certain kinds of dispersion limitations in long-haul transmission.

Figure 2(a) shows that regenerator spacing is dominated by certain kinds of limitations, i.e., chromatic dispersion and higher order dispersion, fiber nonlinearities, and polarization mode dispersion. Chromatic dispersion is still a key issue

that must be solved. Allowable chromatic dispersion against bit-rate target is summarized in Fig. 2 (b). Higher bit-rate systems require precise dispersion control. Dispersion compensation techniques are indispensable for taking full advantage of existing fiber cables and commercially available fiber cables. We previously proposed and demonstrated several types of delay equalizers; fibers, planer lightwave circuits, and fiber grating at speeds in the 10 to 40 Gbit/s range [2]. Optical equalization is one of the most important issues for achieving ultra-high-speed transmission. Also, equalization should incorporate a modulation scheme such as duo-binary coding to increase the dispersion tolerance. Pulse duration and filter design also affect S/N ratio of transmitted signals. An up-coming issue is to determine the duty ratio of pulses and modulation formats [3], because both
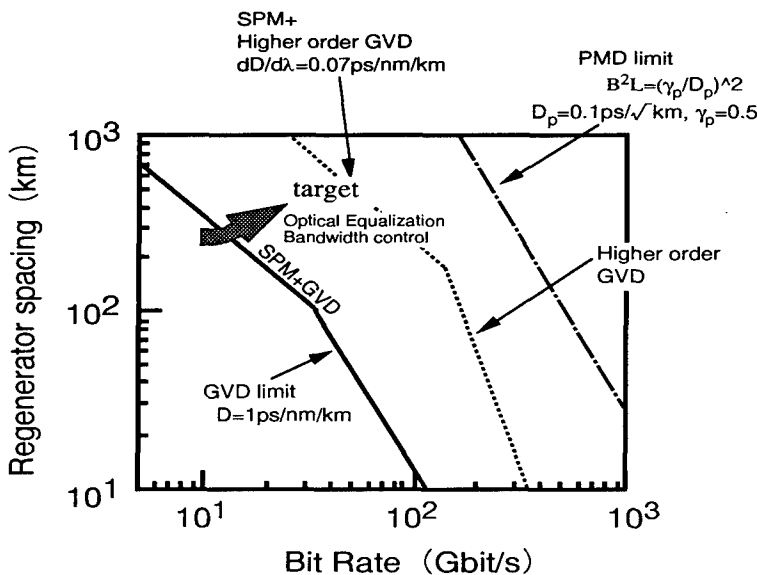
(a) attainable repeater spacing
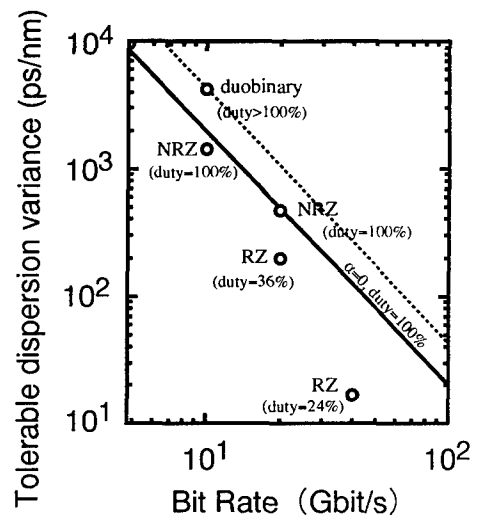
(b) allowable chromatic dispersion variance

Fig.2 Transmission Capability of Regenarator

strongly impact spectral broadening and determine to what degree dispersion is allowed as shown in Fig. 2(b). In general, the higher the system capacity is, the shorter regenerator spacing is. Economical regenerators are quite important. This requires not only high-speed operation but easier packaging. Integration technologies are essential for high-speed transmission systems.

High-speed Circuits

As for operation of high-speed circuits, the optical multiplexing technique can offer several hundreds of gigabits per second. It is not easy to accommodate many channels, so, the rate at which these electrical circuits operate is a key issue. Figure 3 shows the trend in high-speed electrical circuits. New circuit designs and the InP HEMT process yield 40-Gbit/s flip/flop Ics. The process is not yet mature but still these ICs achieve approximately 200 GHz of fT[4]. MUX and decision circuits can

Fig.3 Process Map

operate at 40 Gbit/s as shown in Fig.3. As for analog circuits, distributed amplifier circuit design exhibits significant broadband characteristics. We developed an optical receiver module which consists of a waveguide-type pin-photodiode and a GaAs distributed amplifier [5]. This module realizes the bandwidth of 33 GHz. A LiNbO3 Mach-Zehnder type optical modulator can also be employed for 40 Gbit/s operation.

The combination of 40-Gbit/s electrical circuits and optical multiplexing offers fully engineered 100-Gbit/s transmission capability.

40 Gbit/s Transmission Experiment

Figure 4 demonstrates a fundamental experiment for 40-Gbit/s transmission and beyond. InP monolithic digital circuits are promising candidate devices for 40 Gbit/s operation. Distributed amplifier technology is suitable for analog circuit design. 40-GHz optical pulses are directly generated by a mode-locked semiconductor laser and the 40-Gbit/s signal is encoded by an optical modulator. In this experiment, a short pulse source was employed that also offers higher bit-rates such as 80 Gbit/s. An optical link consists of four 75-km dispersion shifted fibers and three optical amplifiers. The total transmission distance is 300 km. Each optical amplifier accommodates a dispersion compensator to cancel the dispersion of the transmission section. Good eye-opening and bit-error rate performance are obtained through 300 km at 40 Gbit/s. A small difference among the four 10-Gbit/s channels is observed because the InP multiplexer generates a pulse width fluctuation in each of the 40 Gbit/s electrical signals.
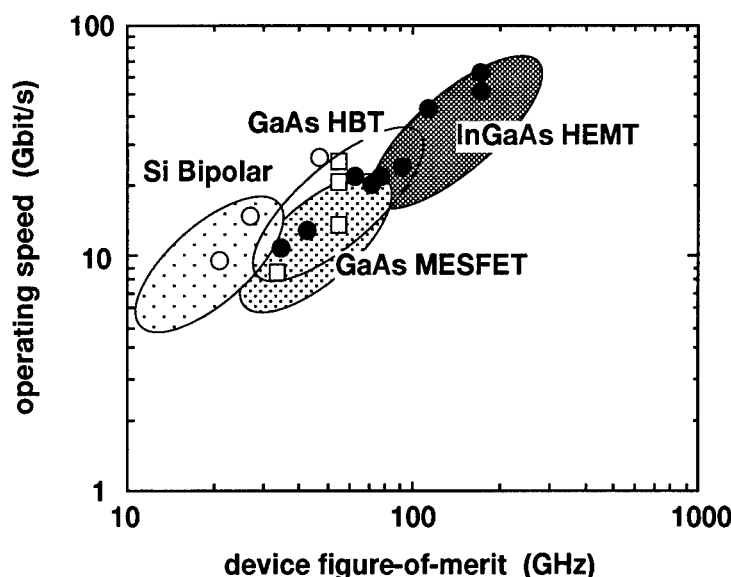
Future Prospects; Integration

40-Gbit/s transmission was demonstrated here, but the 40-Gbit/s interface between circuits is quite critical. Mounting techniques such as Flip-chip method have to be improved compared to the optical interface. Integration of photonic and electric circuits will be a good solution to realize high-speed parallel interconnection as well as serial interconnection. Integration doesn't always mean monolithic integrated circuits. It is important to eliminate higher-speed electrical interfaces in order to realize sinple and cost-effective regenerators.

Conclusion

In conclusion, fundamental repeater circuits were successfully operated at 40 Gbit/s. InP electronic and photonic circuits play an important role in 40-Gbit/s systems. The target and limitations of 40-Gbit/s repeater systems were clarified.

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Fig.4 **40 Gb/s, 300 km Transmission**
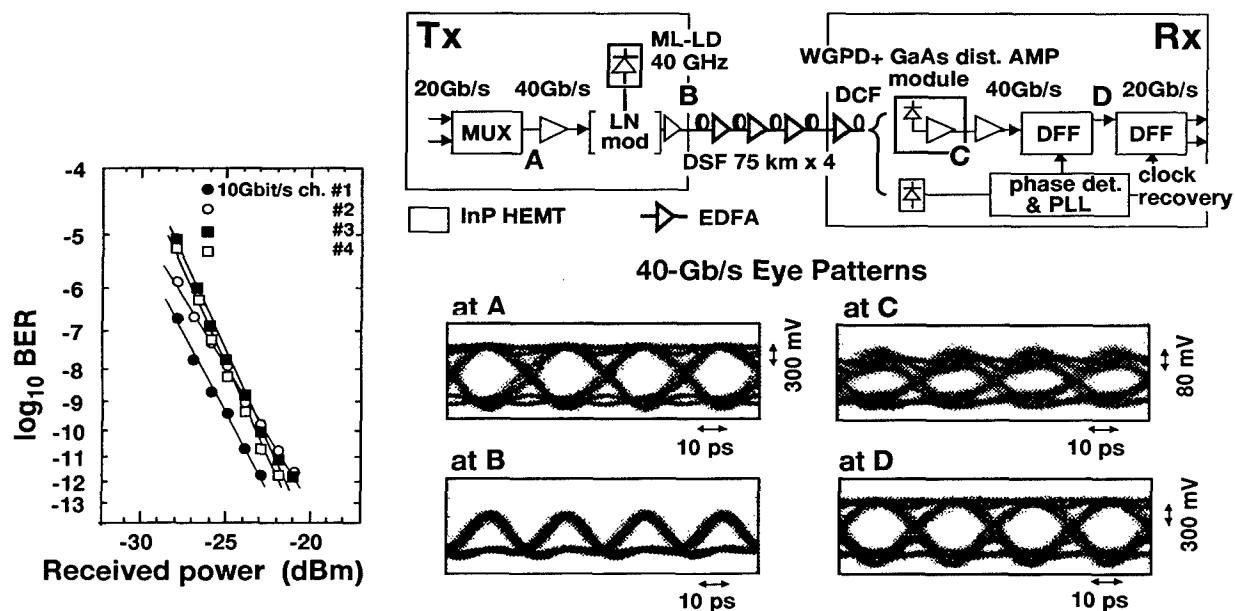
InP HBT Continuous Time 2nd Order Bandpass ΔΣ modulator and 1-to-16 DEMUX IC with Center Frequency Continuously Programmable from 0 to 70 Mhz

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Introduction

We have implemented a continuous time, 2nd order bandpass ΔΣ modulator, with center frequency tunable from 0 to 70 MHz. The modulator has a sampling rate of 4 GHz and is designed in InP Heterojunction Bipolar Technology (npn only, f_T and f_{MAX} ~ 80 GHz). At a center frequency of 62.5 MHz, the modulator exhibits an SNR ranging from 89 dB (14-bits) for a 370 kHz bandwidth to 42 dB (7bits) for a 62.6 MHz bandwidth. These results represent about a factor of 10 improvement in bandwidth, resolution and center frequency over previously reported results in any semiconductor technology. A 1:16 DEMUX is included in the die to reduce the modulator output data rate by a factor of 16. The output of the DEMUX feeds a silicon gate array for digital filtering. The complete integrated circuit contains 1560 HBTs and dissipates 4 W. A companion chip containing I/Q filters with programmable coefficients is under development as a CMOS gate array and will provide decimation and filtering for a variety of bandwidths and center frequencies.

I. Background

Delta-sigma (ΔΣ) modulation has become the method of choice for high-resolution analog-to-digital conversion. The primary advantage of the delta-sigma approach is the ability to achieve high resolution without a complicated fabrication process or active trimming techniques. These converters also simplify system integration by reducing the burden on supporting analog circuitry. Specifically, they do not require precision sample-and-hold circuitry and they relax performance requirements on the analog anti-alias filter that precedes the sampling operation. The purpose of ΔΣ modulators is to trade higher sampling speed (i.e., higher f_S) for obtaining higher resolution [1]. For example, a 2nd order low pass ΔΣ modulator achieves a 15-dB reduction of the baseband quantization noise for each doubling of f_S. We have previously demonstrated a 2nd order low pass ΔΣ modulator implemented with continuous time approach using fully differential current mode bipolar design techniques in InP HBT technology. The ΔΣ modulator operated at 3.2 GHz demonstrating 12-bit dynamic range at an oversampling ratio of 32 [2]. In this paper we have implemented a second order bandpass ΔΣ modulator using similar circuit techniques. Preliminary data of this ΔΣ modulator is reported in ISSCC Technical Digest 1997[3].

The primary motivation of bandpass converters is the simplicity they impart to systems dealing with narrow-band signals. The use of a bandpass ΔΣ modulator permits a direct conversion of an analog signal to digital form at the intermediate frequencies (IF) of radio

frequency (RF) communication systems. This allows the ADC to be moved closer to the receiver front end. Moving the digital interface closer to the antenna reduces receiver analog circuit complexity, eliminates dc-offset cancellation, inphase/quadrature (I/Q) gain calibration, dual I/Q mixers, and improves overall system robustness as mixing is in the digital domain.

II. Fabrication Technology

The IC process utilized for the fabrication reported here is the Hughes Research Laboratories' baseline 3-inch AlInAs/GaInAs heterojunction bipolar transistor (HBT) IC process [4]. It utilizes npn HBTs with an AlInAs emitter, a GaInAs base, and a GaInAs collector. The IC fabrication process (Figure 1) features mesa isolated transistors on a semi-insulating InP substrate, self-aligned base contacts for high speed operation, thin film TaN resistors and high resistivity epitaxial resistors, Si_3N_4 and polyimide capacitors, and two levels of interconnects. The IC fabrication process constructs the individual HBTs first (typically 2×2 μm^2 through 2×20 μm^2) followed by the passive elements. Then the wafers are planarized with polyimide and vias are formed through the polyimide to expose buried electrodes which are contacted with second level interconnects (overlay metal).
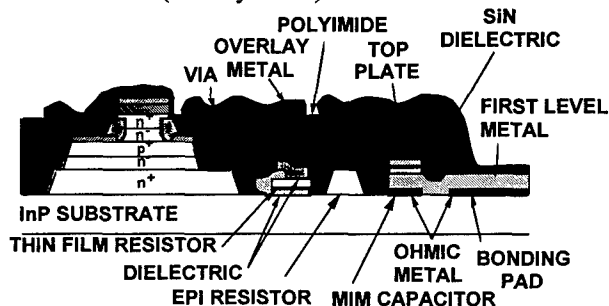
Figure 1. Cross Section of our InP HBT IC fabrication process.

The transistor characteristics of HBTs with 2×2 μm^2 emitters include common emitter current gain in excess of 40. RF characteristics include peak unity current gain cutoff frequency, f_T, of 80 GHz.

Close inspection of completed wafers and attention to process control data assisted us in making process improvements to improve IC yield and thus demonstrate more complex ICs. We utilize a wide variety of process control monitors (PCMs) which provide a window on

the wafers' status at various points within the IC fabrication process. In addition, post-fabrication PCMs help to characterize the wafers, individually, and the process lot as a whole, immediately upon completion of a fab run.

III. Circuit Design

Figure 2 shows the architecture of our fully differential realization of a second order 1-bit output bandpass $\Delta\Sigma$ modulator, which is an extension of the design in [2] and is similar to the architecture proposed by Shoaei and Snelgrove [5]. Performance of this architecture is determined primarily by the Q of the resonator. The major changes from the architecture described in [5] are the insertion of tunable transconductance (g_m) cells in the feedback path of the resonator, inclusion of an extra half clock cycle delay following the comparator and use of current-mode logic in the design. The first of these changes permits the resonator center frequency to be varied from DC to a maximum designed value. The extra half clock cycle delay following the comparator results in matched output rise and fall times which allows us to use a NRZ DAC. The use of current-mode logic reduces switching noise and also eliminates the requirement for high gain operational amplifiers in the design. Figure 3 is a micrograph of the die containing the modulator and a 1:16 DEMUX. The modulator is located in the bottom right hand corner of the die. The modulator measures $750\mu m \times 750$ μm and dissipates 1.4 Watts. The 1-to-16 DEMUX dissipates 0.5 Watts, and the 16 ECL output buffer dissipate 2 Watts.
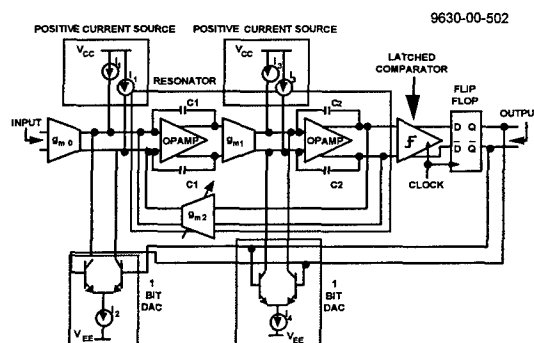
Figure 2. Architecture of the fully differential, continuous time, 2nd Order $\Delta\Sigma$ modulator used in this work.

238
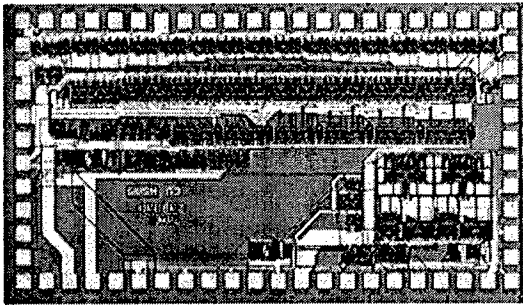
Figure 3. Chip micrograph of the ΔΣ modulator and the 1:16 DEMUX.

IV. Test Results

For testing modulator performance, we sample the 4 GHz, 1-bit output of the modulator using a HP4722A, 8 GSPS sampling oscilloscope. At least two samples per modulator clock are required as the oscilloscope clock is not synchronized to the modulator clock. 32K point FFTs using a Hanning window are performed on either the odd or even set of points after limiting the measured analog data to ± 1. The noise and distortion is then integrated over varying bandwidths to obtain SNR values. Figure 4 shows the output spectrum for various center frequencies and demonstrates notch tunability. A peak SNR of 84.9 dB, 81.2 dB and 80.5 dB was obtained corresponding to notch positions of 62.5 MHz, 41.4 MHz and 24.4 MHz respectively. In Figure 5, we plot modulator SNR as a function of bandwidth. Measurements on this bandpass modulator yield SNR values ranging from 89 dB over a 366 kHz bandwidth to 42 dB over a 62.6 MHz bandwidth.
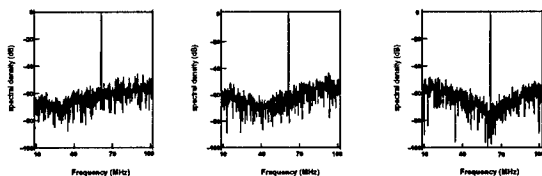
Figure 4. Modulator output spectrum corresponding to notch frequencies of 24.4 MHz, 41.4 MHz and 62.5 MHz respectively.

We test the 1-to-16 DEMUX separate from the ΔΣ modulator in a test mode with a 4 Gbit/sec known data stream. The 16 outputs were captured at 240 MHz and compared to the input pattern. The DEMUX functioned properly up to a clock frequency of 7 GHz. Figure 6 is the logic analyzer output at 240 MHz for a 4 Gbit/sec input pattern of 1110001110001110.

When the ΔΣ modulator and 1-to-16 DEMUX are operated simultaneously, the digital switching noise of the DEMUX degrades the ΔΣ modulator performance. Figure 7 is a plot of SNR versus bandwidth for a second order ΔΣ modulator output through the DEMUX with 128K FFT of data stream with Kaiser window with alpha=20. The SNR of the ΔΣ modulator with the DEMUX operating drops to 70 dB over the same 366 kHz bandwidth.
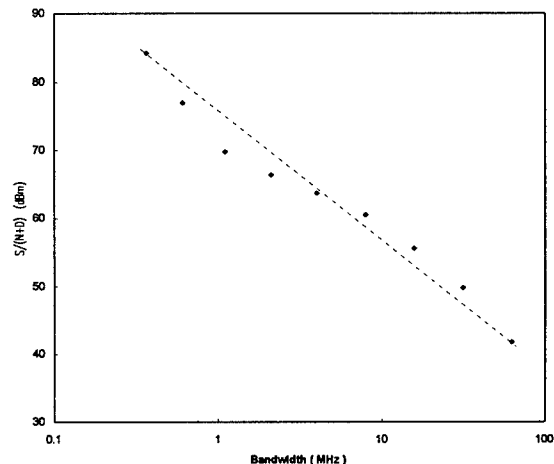
Figure 5. Modulator SNR as a function of bandwidth with the notch at 62.5 MHz.
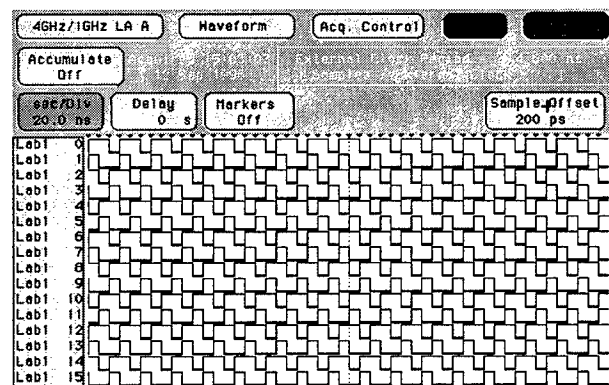
Figure 6. Demux output with signal =1/6 clock = 666.6666 Mhz.
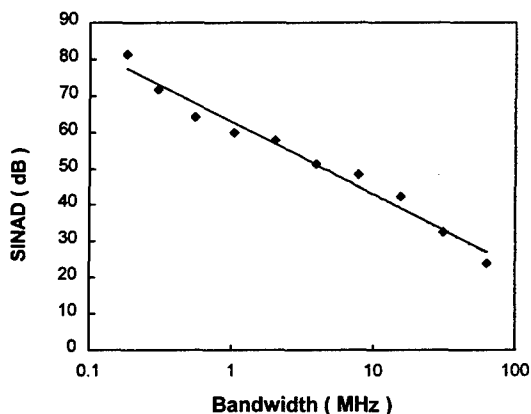
Figure 6. Signal to Noise versus bandwidth for a second order ΔΣ modulator output through the DEMUX 128K FFT of data stream with Kaiser window with alpha=20.

V. Conclusion

Bandpass A/D converters are ideal for simplifying systems dealing with narrow-band signals. The use of a bandpass ΔΣ modulator permits the direct conversion of an analog signal to digital form at the intermediate frequencies (IF) of radio frequency (RF) communication systems. This allows the ADC to be moved closer to the receiver front end.

We have implemented a continuous time, 2nd order bandpass ΔΣ modulator, with center frequency tunable from 0 to 70 MHz. The modulator has a sampling rate of 4 GHz and is designed in InP Heterojunction Bipolar Technology (npn only, f_T and f_{MAX} ~ 80 GHz) [1]. At a center frequency of 62.5 MHz, the modulator exhibits an SNR ranging from 89 dB (14-bits) for a 370 kHz bandwidth to 42 dB (7bits) for a 62.6 MHz bandwidth. These results represent about a factor of 10 improvement in bandwidth, resolution and center frequency over previously reported results in any semiconductor technology.

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D-band MMIC LNAs with 12 dB Gain at 155 GHz Fabricated on a High Yield InP HEMT MMIC Production Process

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ABSTRACT

We have developed a highly robust, high performance 0.1 μm passivated InP HEMT MMIC process with frequency capability up to 200 GHz and beyond. This process has demonstrated consistent wafer to wafer performance as well as remarkable uniformity with a wafer average Gmp of 1100 mS/mm ± 44 mS for more than 1000 sites tested over a 2 inch diameter wafer. We report a D-band InP HEMT MMIC LNA using this process which has demonstrated 12 dB gain at 155 GHz. This represents the highest frequency solid-state amplifier ever reported to date.

INTRODUCTION

High performance millimeter-wave low noise amplifiers (MMW LNAs) are a very important component for advanced communication links, smart munitions, passive imaging and radiometric applications. InGaAs/InAlAs/InP HEMTs (InP HEMTs) have demonstrated the highest extrapolated cutoff frequency and maximum oscillation frequency[1-3] for any three terminal device which make it the future technology of choice for high performance MMW LNAs. However, to date, very little data has been reported on actual InP HEMT MMIC amplifiers operating above 100 GHz. Previously, we have reported the first and only 2-stage 120 GHz and 140 GHz InP HEMT MMIC LNAs which demonstrated 12 dB and 9 dB gain respectively[4,5]. We have also reported the only hybrid 1-stage 140 GHz InP HEMT LNAs with 7.7 dB gain[6]. In this paper, we present the first successful 3-stage 155 GHz MMIC LNA which yields 12.5 dB gain from 153-155 GHz. This demonstration signifies that the extrapolations on our InP HEMT device performance to these frequency levels is valid and that MMIC LNAs designed based on our InP HEMT devices should provide useful gain up to 220 GHz. Furthermore, the 0.1 μm InP HEMT MMIC process used to build this chip has attained a high level of maturity, with consistent wafer to wafer uniformity and unprecedented uniformity over a wafer and is suitable for higher levels of production volumes.

PROCESS DESCRIPTION

We have developed our InP HEMT MMIC process[7] based on our space-qualified GaAs HEMT MMIC process[8,9] to take advantage of our vast knowledge from GaAs HEMT MMIC production development with 70% process commonality. The objective for our layer structure design and process flow was to develop the highest performance device possible that would be manufacturable for MMIC applications. The wafers were grown by molecular beam epitaxy (MBE) on 2" InP semi-insulating substrates. The baseline 0.1 μm InP HEMT structure is shown in Figure 1. The channel is a 150Å pseudomorphic
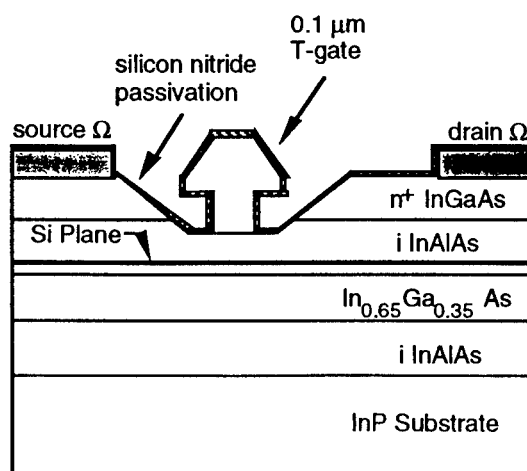
Figure 1. Cross Sectional Layers of InGaAs/InAlAs/InP HEMT Device Grown by molecular beam epitaxy

65% Indium composition InGaAs layer which provides superior transport properties and high electron sheet densities. Typical room temperature Hall mobility of 10500-11000 cm2/V-sec and Hall sheet carrier concentration of 3.5E12/cm2 are measured on undoped cap layer calibration samples.

The devices are isolated using a combination wet etch/boron implantation process which provide better than 10 MΩ/sq. resistance. Source and drain ohmic contacts with Ni/Au-Ge/Ag/Au ohmic contacts alloyed at 400°C using rapid thermal annealing provide very low ohmic contact resistance of 0.06 ohm-mm and source resistance of 0.2 ohm-mm. 0.1 μm gate stripes are fabricated with a bi-layer PMMA/PMMA-MAA resist profile for metal liftoff and are offset 0.6 μm from the source pad. Prior to metallization, the devices are gate recessed etched to a predetermined current level. The target device pinchoff voltage is -0.25V with the voltage at peak transconductance (Vgp) of +0.1V. Typical device transconductance of 1000 mS/mm are attained with the 65% Indium composition InGaAs channel, with a cutoff frequency of 200 GHz. Device reverse breakdown voltage defined at 0.2 and 1.0 mA/mm reverse gate leakage current are 1.5 and 2.5V, respectively.

The devices are passivated with 750Å silicon nitride deposited using PECVD. For the MMIC process, we form precision NiCr resistors with a target resistance of 100 ohm/square and silicon nitride MIM capacitors with a target sheet capacitance of 300 pF/mm2. After frontside processing, the wafers are lapped and polished to 75 μm (3-mil) thickness. Then ground via holes are wet-chemical etched and 3.5 μm gold is plated on the backside of the wafers to complete the MMIC processing.

DEVICE RESULTS AND DISCUSSION

For the demonstrated 155 GHz MMIC in this paper, 0.1 μm pseudomorphic 65% InGaAs channel devices have been used. For each wafer fabricated, d.c. characteristics are measured on up to 20 test devices (2 finger, 80 μm total gate width). Figure 2 show the wafer average peak transconductance for 24 two inch InP HEMT

wafers constituting 5 wafers lots fabricated over a 5 month period. The wafers on which the 155 GHz MMIC design were fabricated upon are part of this set of 24 wafers.
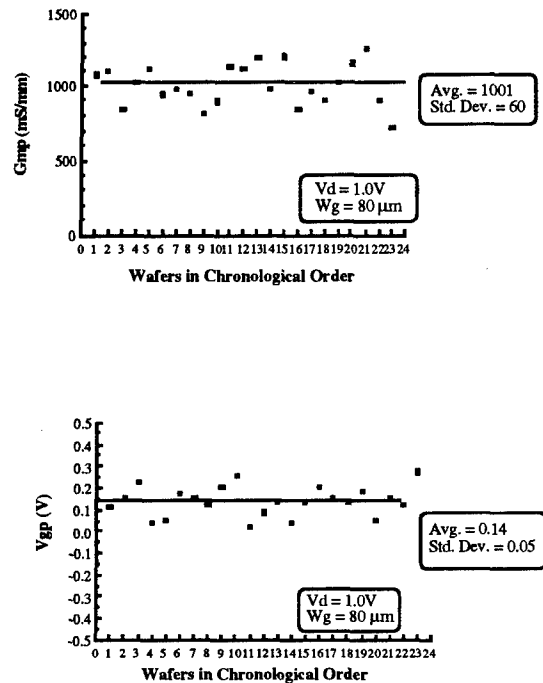
Figure 2   Trend Charts of Wafer Average Gmp (peak transconductance) & Vgp (Vg at Gmp) for InP HEMT wafers processed over a 5 month period (Vd = 1.0V)

Outstanding wafer to wafer device performance repeatability has been achieved for our InP HEMT process as can be seen from this data. The wafer average Gmp at 1V drain bias exhibits 1000 mS/mm average with a standard deviation of only 60 mS/mm. Wafer average Vgp (gate voltage at peak Gm) at 1V drain bias was +0.14V average with a standard deviation of 50 mV.

We have achieved even more remarkable data on wafer uniformity over a 2 inch InP HEMT discrete device wafer. After completion of front side lithography on one device wafer lot, we measured d.c. parameters on over 1000 devices over a two inch InP HEMT wafer. Figure 3(a),(b) shows the parameter histograms measured at 0.7V drain bias for Gmp and Vgp for this wafer.

242
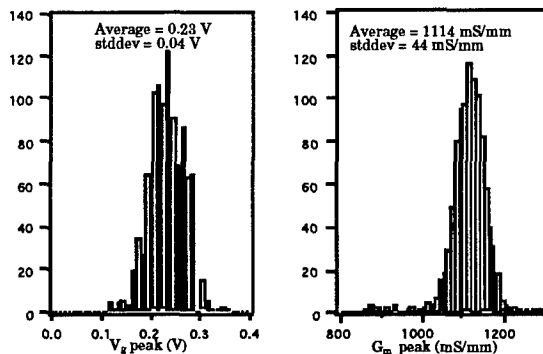
Figure 3. Histograms of Vgp and Gmp for 1000 InP HEMTs over a two inch wafer (0.1 μm x 20 μm device, Vd = 0.7V)

A standard deviation of less than 50 mS/mm for Gmp and less than 40 mV for Vgp was achieved. This data demonstrates the excellent quality and uniformity of our MBE growth, gate lithography, gate recess etching process and wafer fabrication processes.

155 GHz LNA RESULTS AND DISCUSSION

We have developed a family of MMIC LNAs extending from 35 GHz to 160 GHz, including a first iteration 155 GHz MMIC LNA design. A picture of the 3-stage 155 GHz LNA is shown in Figure 4. The 155 GHz amplifier is a three-stage single-ended design with a 4 finger 30 μm device in each stage. The chip was tested in a G-band (140-220 GHz) test fixture with microstrip to waveguide E-plane probe transitions fabricated on 3-mil quartz.
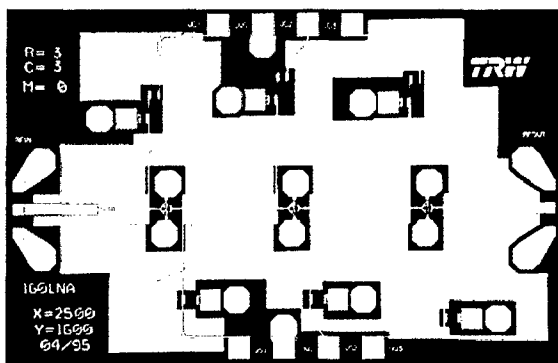
Figure 4. Photograph of fabricated 3-stage InP HEMT MMIC LNA

The measured insertion loss for back-to-back transitions was 2.5 dB with a return loss of better than 15 dB from 152 to 168 GHz. Figure 5 shows the gain and input/output return loss for the amplifier from 148 to 158 Ghz.

The amplifier exhibits a peak gain of 12.5 dB from 153-155 GHz corrected for the transition losses and demonstrates greater than 10 dB gain from 151-156 GHz with an input return loss better than 5 dB and an output return loss better than 10 dB. Furthermore, the d.c. power consumption of this chip was only 35 mW (Vd = 1.4V and Id = 25 mA). With Vd = 1.0V and Id = 25 mA bias conditions, the peak gain was reduced by 2 dB to 10.5 dB at 153 GHz.
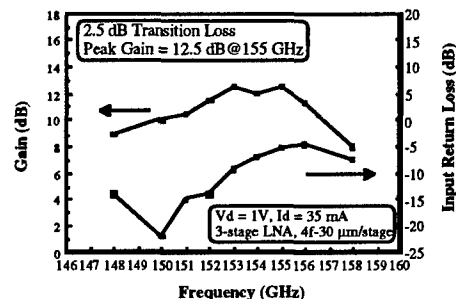
Figure 5. (a) Gain and Input Return Loss vs. Frequency for 3-stage InP HEMT MMIC LNA (Bias at Vd = 1.4V, 25 mA)

One of the significant results of this MMIC LNA demonstration is that our small signal InP HEMT device model is verified to 155 GHz and the extrapolated fT & Fmax values for our InP HEMT devices are validated. Figure 6 shows the frequency dependence of gain per stage for TRW InP HEMT MMIC amplifiers operating between 94-155 GHz and the calculated maximum available gain from the small signal InP HEMT device model.
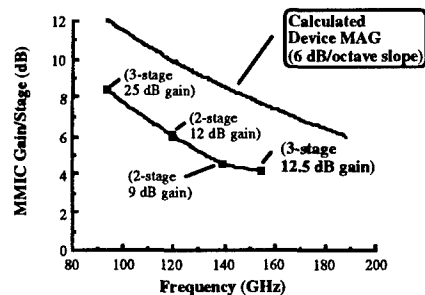
Figure 6. Gain/stage vs. Frequency (Frequency range from 94 to 155 GHz) for 4 multi-stage TRW InP HEMT MMIC LNAs

243

The gain per stage is degraded compared to the maximum available gain of the InP HEMT due to parasitic inductance from the wet-etch via hole and losses in the transmission lines and matching networks. Future work to extend the frequency operation to 220 GHz and beyond and to increase gain/stage for LNAs operating at these high frequency will focus on improving device transconductance, reducing device capacitances, developing smaller inductance via holes and reducing transmission line loss.

CONCLUSION

In conclusion, we have described the development of a 3-stage MMIC InP HEMT LNA operating at 155 GHz with 12.5 dB gain. This amplifier is the best of our knowledge, the highest frequency 3-terminal amplifier ever demonstrated to date. Based on the results achieved here, we project that MMIC LNAs operating at 220 GHz and beyond with usable gain are achievable with InP HEMT technology in the near future.

ACKNOWLEDGMENTS

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80–100 GHz Broadband Amplifier MMIC Utilizing CPWs and Quarter Micron InP–Based HEMTs

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Abstract— A broadband monolithic amplifier utilizing coplanar waveguides on InP substrate for applications in the frequency range from 80–100 GHz (*W*–band) is presented. The circuit is realized with lattice matched InAlAs/InGaAs/InP HEMTs with a gate–width of $W_G = 2 \times 40\,\mu$m and T–gates with a gate–length of $L_G = 0.25\,\mu$m. Coplanar waveguides and lumped elements are used for the matching and biasing networks. The modeling of the amplifier was based on small signal equivalent circuit descriptions using lumped elements for all discontinuities such as airbridges, T–junctions and MIM–capacitors. The circuit is fully passivated and contains common ports for the gate and the drain bias. At a frequency of 94 GHz the amplifier reaches a gain of 15.5 dB, an input matching better than -8 dB, and an output matching better than -20 dB. The 3 dB–bandwith of the amplifier is greater than 20 GHz.

I. INTRODUCTION

IN the past, the best high–speed and low–noise performance of any type of transistor up into the millimeter wave range was demonstrated by InAlAs/InGaAs/InP–HEMTs [1], [2]. Therefore this type of device is very attractive for communication and sensor system applications especially in the millimeter wave region and serves as a complement to GaAs–based devices for very high frequencies. For front–end transmit/receive modules there is a need for low–noise amplifiers with high power gain in the receiver part of the system. While mostly microstrip lines (MSLs) are used in MMICs as the transmission media, coplanar waveguides (CPWs) are now becoming an interesting alternative [3] – [5]. For commercial applications the use of a low–cost fabrication technology is highly recommended. This can be provided by using CPWs since the circuits are easier to fabricate (no substrate thinning, no via holes and no backside metallization) and they show better electrical behavior (lower grounding parasitics, lower dispersion).

II. CIRCUIT FABRICATION

The active devices inside the amplifiers were realized in the lattice matched InAlAs/InGaAs/InP material system using a very thin low–temperature (LT) InAlAs buffer layer and a surface depleted cap layer as shown in Tab. I. One great advantage of the very thin buffer layer is that mesa isolation and final mesa height is much more reproducible due to the high selectivity of wet chemical etchants between InAlAs and InP. Furthermore all contact pads and all transmission lines are placed on top of the semi–insulating substrate which leads to reduced parasitic capacitances. The devices have a U–layout with a gate width of $2 \times 40\,\mu$m. We use a conventional device process originally developed for GaAs–based devices and circuits, however material relevant steps such as mesa sidewall and gate recess etching are modified. The gate–length of the devices is $L_G = 0.25\,\mu$m and the gates have a T–shaped cross–sectional area formed using a novel polyimide–assisted process. For the gate recess we use a material–selective wet chemical etchant to improve the reproducibility of the gate recess and the device homogeneity. For the passivation of the circuits we use Si_3N_4 which also serves as the insulator of the MIM–capacitors. All transmission lines, all contact pads and all intercon-

TABLE I
LAYER STRUCTURE USED FOR THE AMPLIFIER "MAXWELL"

11 nm	$In_{0.53}Ga_{0.47}As$	surface depleted
22 nm	$In_{0.53}Ga_{0.47}As$	undoped
22 nm	$In_{0.52}Al_{0.48}As$	undoped
	δ–Doping Pulse	$7\,E\,12\,cm^{-2}$ (Si)
4 nm	$In_{0.52}Al_{0.48}As$	undoped
20 nm	$In_{0.53}Ga_{0.47}As$	undoped
10 nm	$In_{0.52}Al_{0.48}As$	undoped
1.2 nm	$In_{0.53}Ga_{0.47}As$	undoped
5 nm	$In_{0.52}Al_{0.48}As$	undoped
1.2 nm	$In_{0.53}Ga_{0.47}As$	undoped
53 nm	LT $In_{0.52}Al_{0.48}As$	undoped
400 μm	InP (Fe) substrate	semi–insulating

nections are made with the $3\,\mu m$ thick sputtered and electroplated gold.

III. DEVICE AND CIRCUIT MODELING

The active devices have been measured (both DC and RF) and modelled using a small signal equivalent circuit (SEC). The measured DC performance is as follows: $g_{m(max)} = 700\,mS/mm$, $I_{DS}(g_{m(max)}) = 250\,mA/mm$, $I_{DS(max)} = 500\,mA/mm$. Based on RF measurements up to 50 GHz we calculated a maximum current gain cut–off frequency of $f_T = 120\,GHz$ and a maximum power gain cut–off frequency of $f_{max} > 250\,GHz$. The minimum noise figure and the associated gain of a single device have been measured at $f = 18\,GHz$ ·(Fig. 1). At this frequency point the device has a minimum noise figure of 0.5 dB with an associated gain of 10.5 dB.
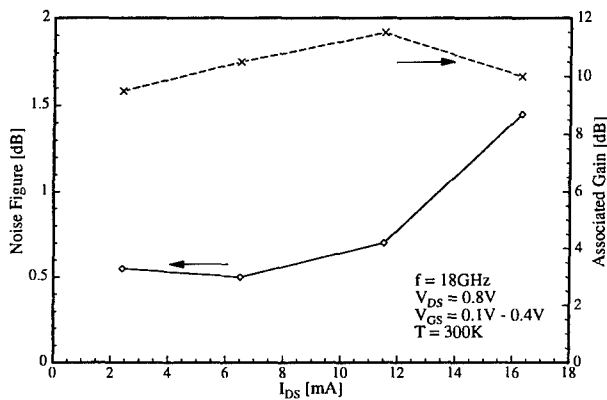
Fig. 1. Measured noise figure and associated gain at $f = 18\,GHz$ for a single device with a gate geometry of $2 \times 0.25\mu m \times 40\,\mu m$

In this paper, a monolithic amplifier on InP substrate with four stages utilizing coplanar waveguides is presented. The 4–stage amplifier "MAXWELL" was designed for broadband amplification between $f = 80\,GHz$ and $f = 100\,GHz$. The simulation and optimization of the amplifier was performed using the Hewlett–Packard *Microwave and RF Design System*® software package. The transmission lines and all discontinuities such as MIM–capacitors (Figs. 2 + 3), T–junctions (Fig. 4) and airbridges were modelled using an equivalent lumped element description. The characteristic parameters of the CPWs (Z_W, α, $\varepsilon_{r,eff}$) were determined using a software tool which calculates these parameters based on a full–wave analysis of the coplanar lines including conductor–loss effects [6]. The amplifier contains only three different matching networks (input, output and interstage matching). We designed one single interstage network, and this network is used three times in the 4–stage amplifier. This modeling procedure makes circuit design much faster.

For the amplifier we use coplanar waveguides with three different characteristic impedances and geome-
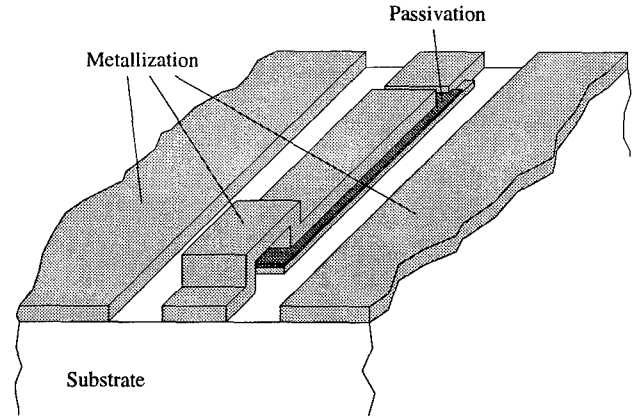
Fig. 2. Principle layout of the MIM serial capacitor used as the interstage blocking capacitor (ground metallization is on bottom, coplanar center stripline is at one side contacted to the dielectric layer using an airbridge).
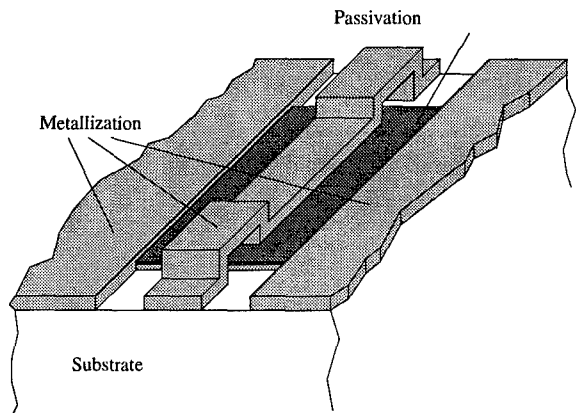
Fig. 3. Principle layout of the MIM parallel capacitor used inside the bias and matching networks (ground cross metallization is on bottom, coplanar center stripline is contacted to the dielectric layer using two airbridges).

tries. We decided to have only three discrete values of Z_L (50 Ω for ideal matching, 35 Ω, and 70 Ω). Referring to our design rules the minimum linewidth for structures being fabricated with electroplated gold is $\geq 10\,\mu m$ for both metallized and non-metallized structures. To avoid an increase in frequency dispersion, to lower distributed effects and to save chip size we have chosen the geometries for the CPWs being the smallest geometry possible. The different CPWs used for

TABLE II
CHARACTERISTIC IMPEDANCES AND GEOMETRIES OF THE
COPLANAR WAVEGUIDE TRANSMISSION LINES

Z_L @ 94 GHz	w	s
35 Ω	40 μm	10 μm
50 Ω	20 μm	17 μm
70 Ω	10 μm	30 μm

246
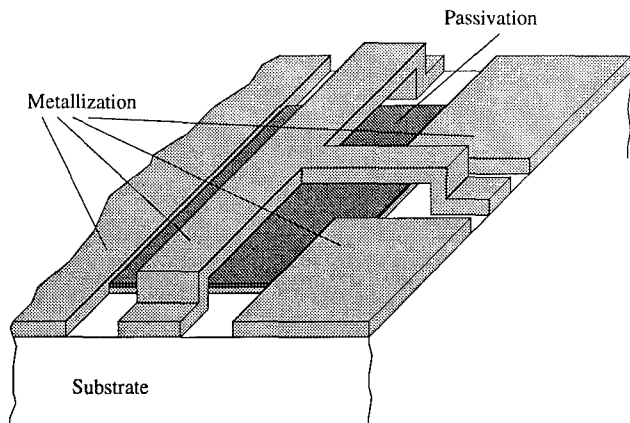
Fig. 4. Principle layout of the T–junction used inside the amplifier (ground cross metallization is on bottom, coplanar center striplines are airbridges.

the circuit can be found in Tab. II.

The T–junctions (Fig. 4) have been modelled using an SEC with only four lumped elements (Fig. 5). The values of the lumped elements show a dependence on the geometry of the different CPWs which are connected by the T–junction. If the width of the center stripline of the CPW increases the value for the inductance decreases but the value for the capacitor increases which is the expected behavior (one can model the inner part of a T–junction as three microstrip lines with an dielectric layer being air ($\varepsilon_r = 1$) and for MSLs the larger geometries show a lower inductivity but a higher capacity). It is worth notifying that the values for the three inductances even are not the same although the three CPWs have the same geometry and therefore the same characteristic impedance. This can be explained by the unsymmetry of the T–junction. The T–junction described here has two 90° angles and one 180° angle instead of three 120° angles for a fully symmetric T–junction. Due to cou-
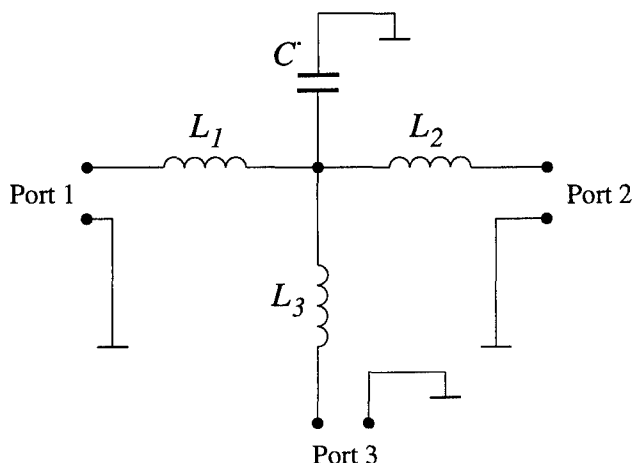
Fig. 5. Small signal equivalent circuit used to model the behavior of the T–junctions.

pling effects between the lines the phaseshift of S_{12} is higher than that of S_{13} and therefore the value for L_3 differs from the values for L_1 and L_2. For example, for a T–junction with three $50\,\Omega$ CPWs ($w = 20\,\mu$m, $s = 17\,\mu$m) the values for the lumped element description are $L_1 = L_2 = 14.1\,$pH, $L_3 = 12.6\,$pH and $C = 14.7\,$fF [7].

The layout of the MMIC meets all the requirements for a low–cost and high–yield fabrication process. The amplifier contains common ports for the gate and the drain bias, and all biasing and matching networks are included on chip. To avoid losses inside the matching subcircuits only reactive LC–networks were used as input, output and interstage transformers. The inductances are represented by sections of CPW lines and the capacitances are realized with MIM–capacitors. For the stage separation and for the biasing and matching networks we use MIM–capacitors and epitaxial resistors.

IV. Circuit Performance

The amplifier (Fig. 6) was measured on–wafer between f = 75 GHz and f = 110 GHz. The measured S–parameters for the amplifier as a function of frequency are shown in Fig. 7. Over the entire measurement frequency range, the MMIC was unconditionally stable (K > 1). The power gain of the broadband 4–stage amplifier shows a 3 dB–bandwith of more than 20 GHz between f = 78 GHz and f = 100 GHz with an average value of more than 15 dB. At f = 94 GHz, the amplifier shows a power gain of 15.59 dB, an input matching better than −8 dB, and an output matching better than −20 dB. The noise figure of the amplifier has not yet been measured; however, the noise figure of the amplifier has been calculated based on the measurements of single devices to be less than 6.5 dB at f = 94 GHz. These are excellent values for circuits with $0.25\,\mu$m fully passivated HEMTs.

V. Conclusion

We have reported a broadband 4–stage monolithic amplifier for the frequency range from 80–100 GHz (W–band) utilizing lattice matched InAlAs/InGaAs/InP HEMTs and coplanar waveguide technology. For the active devices we have used a polyimide assisted T-gate process. The gate geometrie has been 2 × $0.25\,\mu$m × $40\,\mu$m. At a frequency of 94 GHz the amplifier reaches a gain of 15.5 dB, an input matching better than −8 dB, and an output matching better than −20 dB. The 3 dB–bandwith of the amplifier is greater than 20 GHz.

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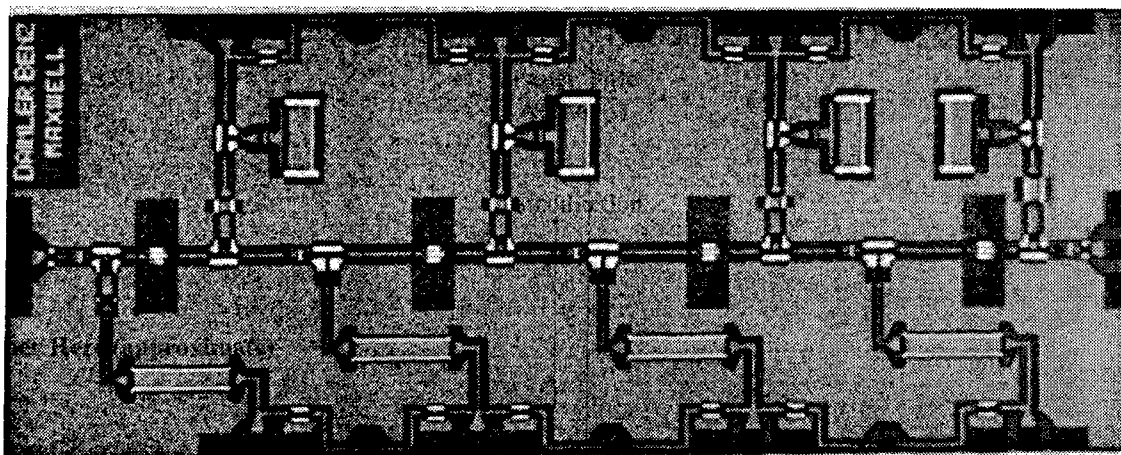
Fig. 6. Photograph of the 4–stage broadband 80–100 GHz amplifier chip "Maxwell". The chip dimensions are 1.3 mm × 3.4 mm.

M1
M1=13.541E+00
I1=78.500E+09

M2
M2=15.591E+00
I1=94.000E+09

M3
M3=12.963E+00
I1=100.00E+09

```
75.0E+09      FREQ      110.0E+09 A      75.0E+09      FREQ      110.0E+09 A
75.0E+09      FREQ      110.0E+09 B      75.0E+09      FREQ      110.0E+09 B
dB(S11)                  dB(S22)         dB(S12)                  dB(S21)
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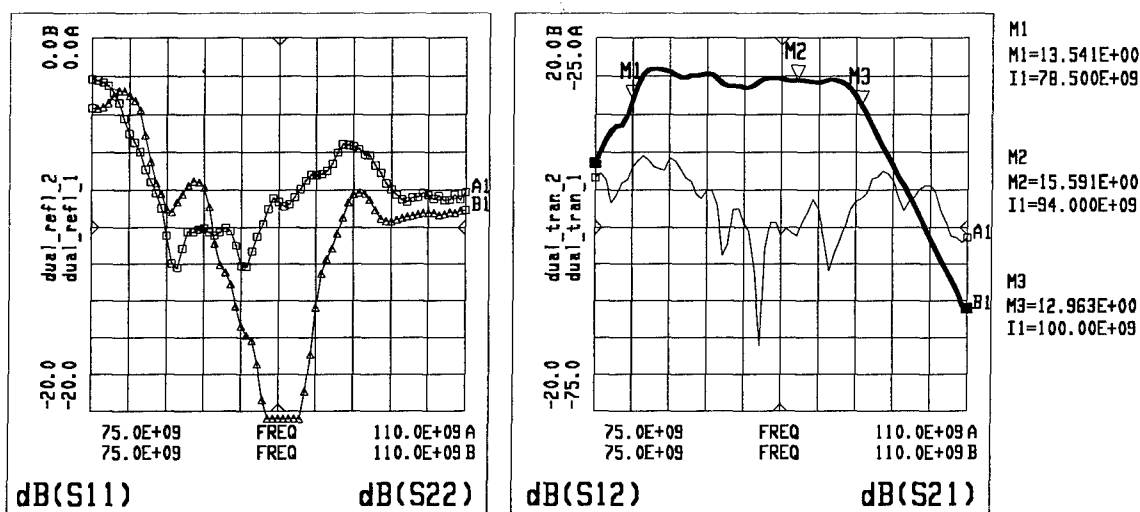
Fig. 7. Measured S–parameters of the 4–stage broadband 80–100 GHz amplifier "Maxwell": $|S_{11}|^2$ [dB] (—□—□—□—), $|S_{22}|^2$ [dB] (—△—△—△—), $|S_{12}|^2$ [dB] (small ——), and $|S_{21}|^2$ [dB] (thick ——).

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W-BAND HIGH-GAIN AMPLIFIER USING
InP DUAL-GATE HEMT TECHNOLOGY

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Introduction

High Electron Mobility Transistors (HEMTs) based on InP have proven to be the best performing three terminal devices at millimetre frequencies (1). This makes them an attractive alternative for MESFET technology to be incorporated in monolithic microwave integrated circuits (MMIC) with operating frequencies up to 100 GHz and beyond. In this paper we first present a coplanar technology for fabrication of InP HEMTs as well as passive components, involved in MMICs. A W-band high-gain amplifier based on this technology was designed and realised and results are presented, demonstrating the capabilities of InP HEMTs at frequencies in the range of 100 GHz.

I. HEMT Fabrication

To obtain an optimally performing HEMT both the heterostructure and the process that is applied to it must be adjusted to each other.

A. The Heterostructure

In this work a lattice matched MBE-grown $In_{.53}Ga_{.47}As$ / $In_{.52}Al_{.48}As$ heterostructure on a 2" semi-insulating InP substrate is used. For reproducibility, needed in optimising the process, a basic epitaxial layer sequence compared to others (2,3) is chosen. This is shown in Fig. 1.
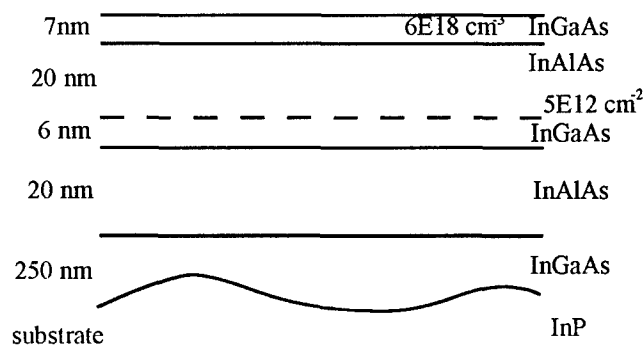
Fig. 1. $In_{.53}Ga_{.47}As$ / $In_{.52}Al_{.48}As$ heterostructure grown lattice matched on InP with Si-doped cap and Si delta-doping.

On top of a 250 nm $In_{.52}Al_{.48}As$ buffer layer the 20 nm $In_{.53}Ga_{.47}As$ channel is grown, followed by the high band-gap $In_{.52}Al_{.48}As$. At this interface a 2-dimensional electron gas (2-DEG) will arise in the channel layer as a consequence of the discontinuity in the conduction band. The channel is provided with electrons by the $5*10^{12}$ cm^{-2} Si delta-doping, separated from the channel by a 6 nm spacer layer. The 20 nm $In_{.52}Al_{.48}As$ layer will act later on as a Schottky barrier for the gate. Finally, a 7 nm $6*10^{18}$ cm^{-3} Si-doped $In_{.53}Ga_{.47}As$ cap layer is applied to facilitate the forming of ohmic contacts and to prohibit oxidation of the Schottky layer.

At room temperature this epitaxial sequence results in an electron density $n_e = 2.1*10^{12}$ cm^{-2} and a low-field mobility $\mu = 10500$ $cm^2/V.s$. Although higher values are reported in literature, this commercially available layer is a good tool to demonstrate the performance of InP MMIC technology.

B. Device Processing

The first step in device processing is mesa isolation. This is done in a phosphoric acid based solution for removal of the active layer, directly followed by an etch step in a succinic acid based mixture. This selectively etches the $In_{.52}Al_{.48}As$ channel material, resulting in a reduction of the sidewall leakage from gate to channel (4).

After cleaning and the second optical lithography step the metal for ohmic contacts is applied by e-beam evaporation. For better adhesion of the metal to the semiconductor we start with a thin (2.5 nm) layer of Ni,

followed by 80 nm Au and 40 nm Ge. To cap the metal and facilitate later contacting 5 nm of Ni and 60 nm of Au complete the metallisation. After lift-off the ohmic contacts are alloyed at 280° C during one minute (5). In this step the Au and Ge diffuse into the semiconductor to form an ohmic contact with the channel. By TLM methods the contact resistance is determined to be around 0.2 Ω.mm or even below. Also the square resistance of the unrecessed active layer can be measured ($\sim$ 200 Ω/square).

The most critical step in device processing is the definition of the gate lithography combined with the recess etching of the cap layer. To achieve gate lengths in the deep sub-micron range, e-beam lithography is used. Although slower than parallel exposure methods, it is a flexible tool in the trajectory of process development. E.g., to obtain mushroom shaped gates we used different dose levels on a two-level resist. Fig. 2 gives a schematic cross-section of this exposure.
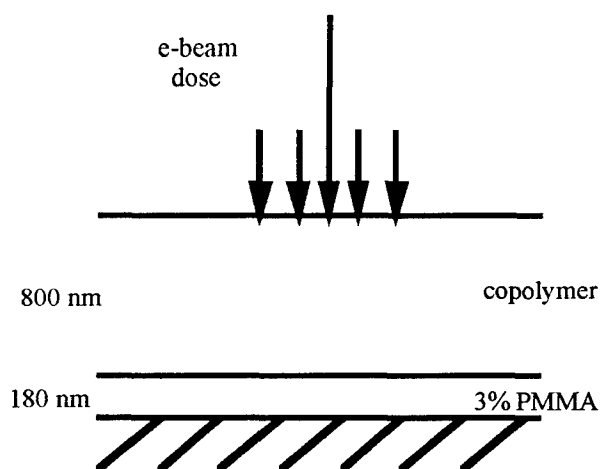
Fig. 2. E-beam exposure on two-level resist with high-dose single scan and low-dose side scans.

The resist consists of a thin layer of diluted (3%) PMMA with on top a more sensitive thick (800 nm) layer of copolymer resist. The high-dose single scan opens both layers for footprint definition, while the low-dose side scans only open the top layer. Fig. 3 shows a SEM picture of the resist profile after exposure and development.

For the recess etch of the cap layer an etchant based on succinic acid is used. This mixture, as used in mesa definition, etches In$_{.53}$Ga$_{.47}$As with a selectivity of approximately 23:1 over In$_{.52}$Al$_{.48}$As. This results in a very low spread in the threshold voltage of 0.05V, as well on a single wafer as from wafer to wafer. After the etchant has reached the Schottky layer only lateral etching is performed, increasing the gate isolation. Gate leakage current and gate-drain breakdown voltage can be improved by overetching, still keeping the same treshold voltage. Gate-drain breakdown voltage can be tuned from 5V for a moderately overetched device up to 11 V for a completely removed cap in the source-drain opening. Cap removal results in an increase in source and drain

resistance, so a trade-off has to be made. The recess etch can be completed by a short dip in a phosphoric based etchant to remove oxides, originating from the succinic recess etching.
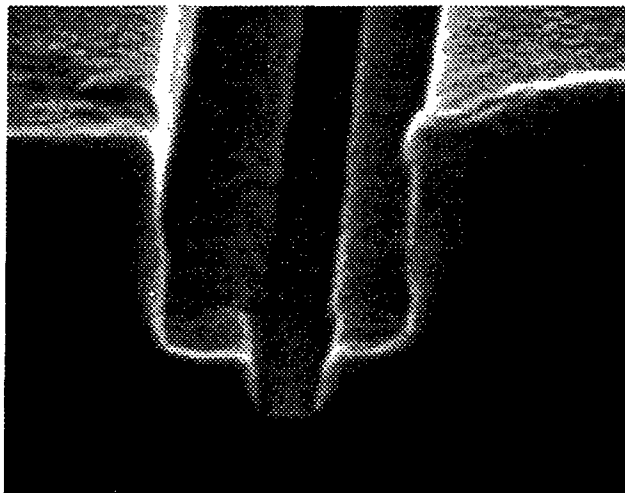
Fig. 3. Cross-section of two-level resist after e-beam exposure. The footprint is 150 nm wide.

Gate contact metal is applied by e-beam evaporation and starts with Pt to assure a maximum Schottky barrier height to the semiconductor and finishes with thick Au to reduce the gate resistance. Again lift-off is performed to remove the superfluous resist and metal.

Final step in HEMT fabrication is the passivation of the device by PECVD of Si$_3$N$_4$ to stop oxidation of the recessed area and stabilise the gate mechanically. This dielectric material is used as well in the fabrication of on-wafer MIM-capacitors.

Transistors based on the technology described above show a DC transconductance g_m = 800 mS/mm. Extrapolation from HF S-parameter measurements gives a cut-off frequency f_T = 165 GHz and a maximum oscillation frequency f_{MAX} = 300 GHz (both extrinsic values).

II. Passive Components

Besides active components also passive components are needed on-wafer for completion of the integrated circuit. Resistors, capacitors and inductors are introduced in this section.

Resistors are realised with thin sputtered NiCr films ($\sim$ 100 nm), resulting in a square resistance of typically 15 Ω/square. A typical value of 50 Ω can be achieved on a small area of 10x35 μm^2. MIM-capacitors consist of a 200 nm PECVD-grown Si$_3$N$_4$ dielectric layer, sandwiched between two metal levels. A typical value of capacitance is 3 pF for a 100x100 μm^2 area. Inductances are realised by spiral inductors yielding values up to 2 nH.

The geometric complexity of integrated circuits and the use of spiral inductors and MIM-capacitors make it necessary to incorporate airbridges in the applied technology. Airbridges are realised by thin contact metal deposition on a resist pattern (via level), directly followed by a second resist level and exposure for definition of the area to be plated. By this electro-plating process a final 1.5 μm layer of Au is applied. After subsequent removal of top resist, superfluous contact metal and bottom resist, free-standing airbridges are the result. Fig. 4 shows a detail of a circuit with a resistor and a MIM-capacitor.
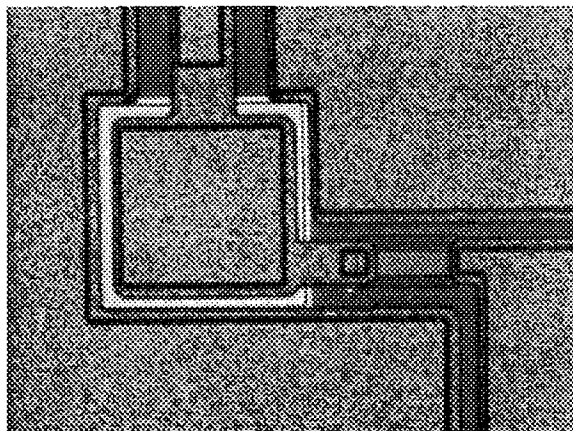
Fig. 4. 100x100 μm² capacitor and thin film resistor (right), surrounded by plated ground plane.

The top electrode crosses the edges of the nitride via airbridges, forming a parallel capacitance to ground.

III. W-band amplifier

Based on the technology presented in the preceeding two chapters an amplifier has been designed for maximum gain at 94 GHz.
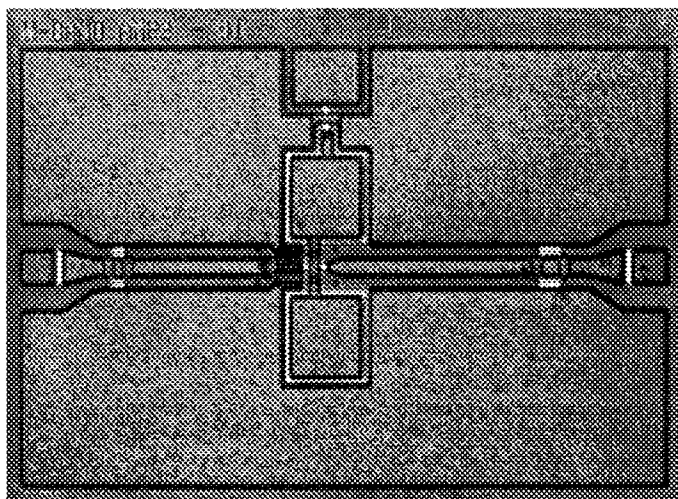
Fig. 5. Coplanar W-band high-gain amplifier (500x750 μm²).

Fig. 5 shows a photograph of the realised circuit. In this 1-stage small band amplifier a 2x50 μm dual-gate HEMT is used. This technique has shown its advantages in several applications (6,7). Additional biasing of the DC gate gives the opportunity of increasing and controlling the gain. Also the kink-effect, generally associated with deep-level traps (8), and the correlated impact ionisation (9) in the InP HEMT can be suppressed (10). Disadvantages of dual-gate devices are the need for a higher supply voltage (up to 4V) and a possibly lower yield.

The in- and output matching networks consist of a transmission line and a capacitor. The contact pad for the DC gates is de-coupled by two capacitors.

Simulations of the design predict a gain of 12.8 dB. On-wafer S-parameter measurements as plotted in fig. 6 show a maximum gain of 12.4 dB at exactly 94 GHz.
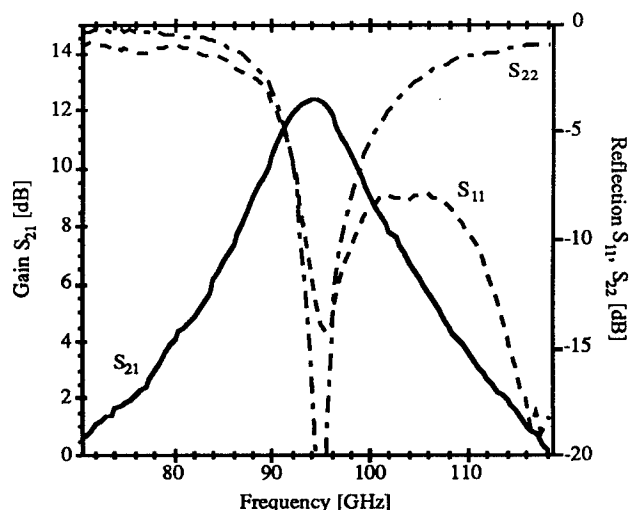
Fig. 6. Measured gain and reflection of a coplanar 1-stage W-band amplifier on InP (V_d=4V, V_g=0.05V, V_{g2}=1V) .

The measurements also show in- and output reflection coefficients (S_{11} and S_{22}) below -11 dB at the operating frequency. The saturated power P_{sat}= 6.5 dBm with the compression point P_{1dB} = 3 dBm.

IV. Conclusions

We have presented a coplanar MMIC technology with dual-gate HEMTs on InP, including passive components. Based on a relatively basic lattice matched heterostructure, a design for a single-stage W-band high-gain amplifier has been made and realised. A gain of 12.4 dB at 94 GHz is combined with an excellent in- and output reflection.

Acknowledgements

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FEEDBACK CONTROL OF SUBSTRATE TEMPERATURE AND FILM COMPOSITION DURING MBE GROWTH OF LATTICE-MATCHED InGaAs on InP

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Introduction

The use of *in situ* sensors to achieve real-time control of MBE growth is a rapidly evolving technology that promises to revolutionize MBE in terms of process repeatability and first-pass success, and consequently, to improve the overall yield and reduce the cost of the process. For the growth of InGaAs and related materials on InP, the most critical process variables to control are the substrate temperature and the epitaxial layer composition, insofar as both of these parameters can have dramatic effects on the performance of heterojunction bipolar transistors and other electronic and opto-electronic devices grown on InP. To achieve robust real-time control of the MBE growth process, we have constructed a multiple-sensor control system comprising *in situ* sensors for substrate temperature, effusion cell fluxes, and epitaxial layer composition and thickness, along with advanced software to manage the sensor information and execute sensor-feedback control algorithms. The design and operation of this system is described and its performance is illustrated through examples of real-time sensor-feedback control of substrate temperature and layer composition during the growth of InGaAs on InP.

I. Background

Molecular beam epitaxy (MBE) is currently the most powerful and flexible growth method available for the fabrication of advanced device structures in InGaAs and related materials grown lattice-matched to InP. The ability of MBE to controllably grow the extremely thin monolayer-scale films required for devices such as resonant tunneling diodes, as well as the capability to grow lattice-matched device layers with arbitrary composition and doping profiles, is unequaled. However, MBE as traditionally practiced suffers from poor repeatability, and this is due in part to the lack of any means to sense and control the two basic process parameters that determine the outcome of the growth: namely, the substrate temperature and the effusion cell fluxes. To address this obvious shortcoming of MBE, a great deal of research over the past decade has been directed toward the development of *in situ* sensors. This sensor technology is now sufficiently mature to make real-time sensor feedback control of the major process parameters of MBE feasible .

For substrate temperature sensing, absorption-edge spectroscopy (ABES), in which the temperature dependence of the substrate bandgap is exploited to determine the temperature, has proven to be a robust and accurate method. The ABES technique, originally developed at Stanford [1], is based on locating the wavelength position of the absorption edge of the substrate wafer from either transmission or reflection spectra. The absorption edge location shifts with temperature as the bandgap changes, thus allowing the temperature to be inferred once the dependence of the bandgap on temperature has been established for the particular substrate material. ABES works best in a transmission configuration, but has also been implemented using specular reflectance [2] and diffuse reflectance [3] embodiments, and recently has even been extended to the use of thick, optically opaque overlayers as well [4].

Direct *in situ* sensing of the flux of atoms delivered to the substrate surface from the effusion cell sources has been demonstrated using optical absorption of light from an atomic resonance lamp made of the same material as the element to be sensed [5]. This atomic absorption technique, which for convenience we refer to as optical flux monitoring (OFM), has now reached a state of development where its precision and accuracy are adequate for real-time control of III-V MBE growth [6-8], and OFM has proven valuable both for the elimination of flux shutter transients and also in conjunction with film composition control, as described below.

The composition of a growing epitaxial layer can be determined from *in situ* spectroscopic ellipsometry (SE) measurements, and the use of SE for real-time composition control has been reported for AlGaAs and HgCdTe [9,10], and for both MBE and MOCVD growth. However, for the case of InGaAs, the optical "constants" needed to apply SE have only recently become available. Consequently, the use of SE to control InGaAs composition is in a very early stage of development, however the initial results are promising.

In order to achieve the maximum benefit of the *in situ* sensing techniques just described, we have constructed an MBE growth system which incorporates ABES, OFM and SE sensing in a common growth chamber, and have developed special supervisory and control software to manage the acquisition and interpretation of the sensor data and to implement regulation and control algorithms based on the real-time information about the growing epitaxial film. The design, construction and application of this multi-sensor control system is described below.

II. Experimental

To accomodate sensors for substrate temperature, effusion cell fluxes, and layer composition and thickness, a multi-port growth chamber was retrofitted onto an otherwise standard Vacuum Generators V80H MBE system. In addition to having pairs of optical viewports situated appropriately to allow for optical absorption flux monitoring and spectroscopic ellipsometry, a key feature of this modified growth chamber is a new in-line substrate manipulator (also manufactured by VG) that features a clear bore down the rotation axis. A quartz light pipe was installed down the bore of the manipulator, with one end terminating aproximately 5mm behind the substrate position and the other end butted against a pyrex viewport mounted on a mini-conflat flange at the top of the manipulator. In order to make ABES transmission measurements, a chopped white light source outside the vacuum chamber is focused using a lens onto the front side of the substrate wafer. The transmitted light enters the end of the light pipe just behind the wafer, and is collected at the other end of the rod by a fiber optic bundle placed just outside the vacuum viewport. The actual measurement of the transmitted spectrum, and the conversion of the spectral data into a substrate temperature reading is accomplished using a commercially available instrument, the model NTM-1 Non-contact Temperature Measurement system manufactured by CI Systems, Inc., in Westlake, CA.

For spectroscopic ellipsometry, we used a Model M-88 Ellipsometer from the J. A. Woollam Co., Lincoln, NB. This instrument records ellipsometric data at 88 wavelengths from 277-762 nm, and includes software for both composition and thickness determination, based on stored optical constant data for InGaAs obtained under MBE growth conditions.

Optical absorption flux monitoring was accomplished using an instrument of our own design which employs atomic resonance lamps for In, Ga and Al, and free-space optics to combine the three sources into a single optical beam. This beam passes through the growth chamber parallel to the substrate, approximately 1-2 cm away from the wafer surface. The transmitted beam is reflected at the opposite side of the chamber and passes a second time through the path of the effusion cell fluxes. Light from each separate resonant lamp is absorbed only by atoms of the identical type to those in the lamp, and consequently the individual absorption signals can be separated by using a grating to disperse the components, and individual detectors for each element's absorption line. The net absorption signal is translated to a flux value using

calibration constants determined empirically by relating actual growth rates of binary compounds to the absorption values measured using the OFM sensor.

III. Results and Discussion

A. Substrate Temperature Control

During the growth of InGaAs on InP, several important effects occur which cause the substrate temperature to vary considerably. The largest of these is the temperature rise that occurs due to the increase in absorption of radiant energy from the heater when the smaller bandgap InGaAs is deposited. This effect, which was first reported by Shanabrook, et. al [11] for InAs growth on GaAs, is due to the fact that InP is largely transparent to heater radiation since most of energy falls at wavelengths below the InP bandgap, whereas InGaAs, by virtue of its smaller gap, absorbs much of the radiant energy that would otherwise be transmitted through the substrate. Figure 1 shows the temperature rise measured using ABES, for InGaAs layers grown on double-polished InP, and on single-polished InP where the back side of the substrate had an etched (moderately rough) surface texture. As shown in the figure, the net temperature rise is more than 125°C for double-polished InP, and more than 65°C for an etched substrate. Of the total observed rise in temperature, approximately 25-30°C is due to the radiant energy emitted by the effusion cells when the In and Ga shutters are opened, and the remainder is due to the absorption effect described above. The absorption-induced rise is less for single-polished wafers because the roughness of the back surface makes such wafers behave as if they are optically thicker (and thus more absorbing), hence the net increase in absorption when InGaAs is deposited is less than for the double-polished substrate case.

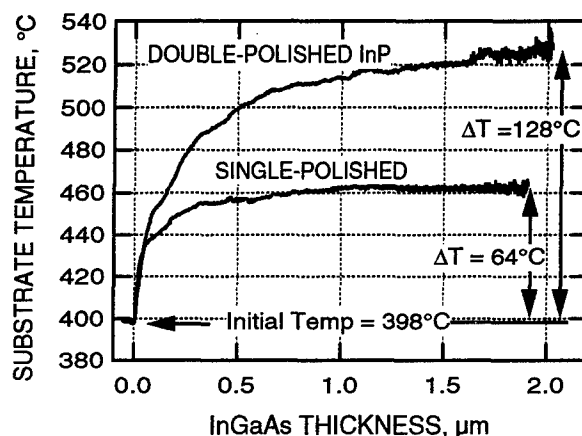*Figure 1. Substrate temperature measured by ABES during growth of x=0.532 InGaAs on an InP free-mounted substrate.*

An important feature of temperature measurement using ABES in the transmission mode is implicit in the data of Fig. 1, namely, that valid measurements can be made even with quite thick overlayers of InGaAs present, in spite of the substantial attentuation of the transmitted spectrum that occurs

due to absorption of light in InGaAs for wavelengths near the InP band-edge, i.e., the region used to determine the temperature. We have succeeded in making temperature measurements for InGaAs thicknesses up to 2.5μm, a thickness more than sufficient to accomodate most modern device structures. In comparison, ABES measurements made in reflection, including either specular or diffuse reflectance modes of operation, are limited to InGaAs thicknesses less than approximately 0.5 μm because light must pass through the epitaxial overlayer twice and therefore is attenuated much more seriously.

Given the ability to accurately measure the true substrate temperature in real-time using ABES, it is possible to completely eliminate the changes in substrate temperature which occur due to shutter opening/closing and due to absorption changes when an epilayer is grown. The method we have employed to accomplish this uses the ABES sensor signal in a nested PID-loop scheme. The substrate thermocouple is retained in the inner control loop for robustness and safety reasons. The fact that the thermocouple does not sense the actual substrate temperature is irrelevant in this scheme because the outer PID loop uses the ABES sensor signal to compare with the user-supplied substrate temperature set point. The outer loop then calculates thermocouple setpoint values to send to the inner regulation loop, as necessary to cause the substrate temperature to attain the desired value. This approach works very well in practice, as shown by the experimental temperature data presented in Fig. 2. Here we have plotted the true substrate temperature, the thermocouple temperature, and the power applied to the substrate heater by the inner loop controller. The experiment consisted of first desorbing the oxide from the InP substrate, using true substrate temperature ramps up and down, followed by the growth of a complete RTD structure at a constant substrate temperature of 480°C and the growth of a complete InGaAs/InAlAs HBT at a different constant temperature of 450°C. The total quantity of InGaAs grown was over 2.2μm.
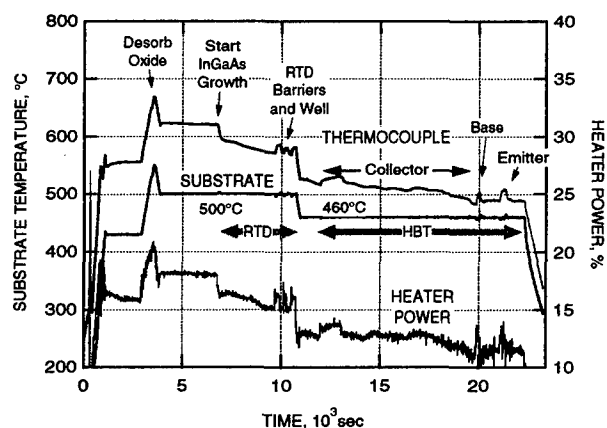
Figure 2. Substrate temperature, thermocouple temperature and heater power recorded during growth of InGaAs/InAlAs RTD and HBT on InP using ABES-feedback control of the true substrate temperature.

It can be seen from the figure that through the use of ABES sensor feedback, the substrate temperature is maintained at the nominal values to better than ±2°C throughout the growth of more than 8 different types of layers, and more than 20 shutter opening and closing events. The substrate temperature rise that would normally occur due to absorption by the InGaAs epilayer has been completely eliminated. Although the substrate temperature remains constant due to feedback control, it is obvious from the numerous fluctuations in the thermocouple temperature and the heater power traces that substantial changes would have occured in the substrate temperature if sensor feedback had not been employed.

B. InGaAs Composition Control

As described above, film composition is determined from spectroscopic ellipsometry measurements made during growth. Real-time feedback control of the composition is achieved using a nested-loop approach similar to that described above for substrate temperature, but with the addition of a third control loop. The innermost control loop uses the effusion cell thermocouple to set the effusion cell heater power. Around this inner loop is a software PID controller that uses the OFM flux sensor signal to derive thermocouple setpoint values for the inner loop in order to regulate the flux at a specified value. This portion of the control operates quite effectively as a flux controller, and is used routinely to eliminate flux shutter transients and also for the execution of growth recipesthat are written in terms of fluxes rather than thermocouple temperatures. For composition control, a third, outer loop takes the composition setpoint supplied by the user (or recipe) and calculates appropriate flux setpoint values for the middle (flux control) loop. In actuality, there are separate middle loops for both the In and Ga effusion cells, but only one of the two is controlled by the outermost (composition) loop, since only one flux needs to be varied to drive the film composition to its target value.

Figure 3 shows composition data from SE, taken during the growth of InGaAs under feedback control.. A step function change in x-value from 0.522 to 0.502 was programmed into the recipe, and it is evident that the change was properly executed by the controller. However, the figure also points out one of the main limitations of this approach to composition control, namely, that the response time is very long, such that abrupt changes in composition over times less than about a minute are difficult to achieve. The primary cause of this slow response is the time required for the ellipsometer software to reliably detect changes in the composition at the surface of the growing epitaxial film. For InGaAs, it is much more difficult to obtain accurate composition values by SE than for AlGaAs, for example, because the optical functions are much less sensitive to composition. Moreover, the degree of composition control required to achieve acceptable lattice-matching to InP pushes the sensing technology to the limit. Nevertheless, based on these early results, we believe that routine composition control of InGaAs growth on InP using SE is feasible.
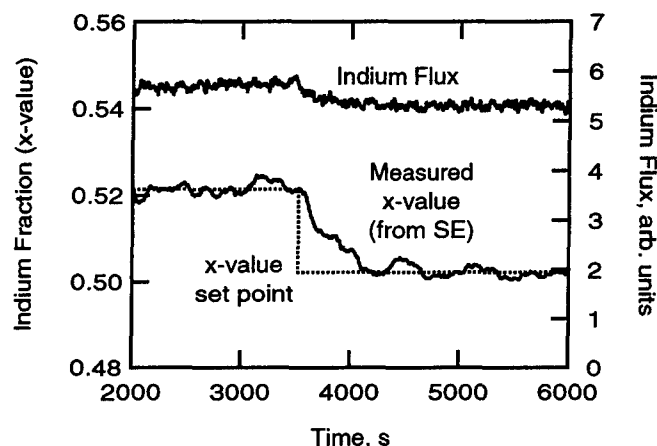
Figure 3. Measured x-value and indium flux during feedback-controlled growth of InGaAs using SE and OFM sensors to regulate the composition according to the setpoint trajectory indicated by the dotted line.

IV. Summary

By using multiple *in situ* sensors for substrate temperature, effusion cell fluxes, and composition and thickness of the growing epilayer, together with a nested-loop PID control scheme, we have successfully achieved real-time feedback control of the most critical parameters for the growth of high-quality InGaAs on InP. This sensing and control technology is in daily use on several research MBE systems in our lab, and certain components are currently being transitioned to the production MBE environment. Key challenges are to improve the reliablility of the sensors and to develop a simple, effective way to specify the desired modes of sensor feedback control within a growth recipe.   Work in both these areas is in progress.

Acknowledgment

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IN-SITU MONITORING OF ARSENIC-PHOSPHORUS EXCHANGE IN MOVPE GROWTH OF InGaAs/InP QUANTUM WELLS BY KINETIC ELLIPSOMETRY

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ABSTRACT

In InGaAs/InP heterostructures, interdiffusion of arsenic and phosphorus at the hetero interfaces (As-P exchange) during epitaxial growth degrades the interface abruptness. This is a significant problem when a very thin InGaAs/InP quantum well is required. In this paper, a spectroscopic and kinetic ellipsometry is used to monitor the As-P exchange *in-situ* in metal-organic vapor phase epitaxy (MOVPE) with TBAs and TBP as group V precursors. As a result, it is found that the monitoring of As-P exchange is possible by kinetic ellipsometry and that useful information to improve gas switching sequence is acquired from such observation. An InGaAs/InP quantum well grown by making use of such information has exhibited the best photoluminescence characteristics.

I. Background

In quantum wells based on InGaAs(P)/InP heterostructures, interdiffusion of arsenic and phosphorus at the hetero interfaces degrades interface abruptness. This problem limits the use of thin quantum wells in this material system. By optimizing growth temperature, pressure, gas switching sequence, and other growth parameters, one may achieve relatively sharp interfaces, but this "trial and error" optimization is inefficient.

In-situ monitoring of epitaxial growth is very helpful for understanding what is happening on the epitaxial surface at the growth temperature. Since the electron- or ion-beam probing, such as RHEED (reflection high energy electron diffraction) in MBE (molecular beam epitaxy), can only be used under high vacuum environment, we need to use other techniques for MOVPE (metal organic vapor phase epitaxy) where the growth is done near atmospheric pressure. There are several optical-beam probing techniques available for this purpose [1-5]. Among these, ellipsometry has an ability of collecting information both from the bulk and from the surface of epitaxial layers.

In this paper, we have studied the arsenic-phosphorus exchange process at the hetero interface between InGaAs and InP in MOVPE by means of an *in-situ* kinetic ellipsometry, and have applied the results to improve the quality of thin InGaAs/InP single quantum wells.

II. Experimental

We used an MOVPE system (AIX200/4) with a horizontal reactor and with substrate rotation. TBP (tertiarybutylphosphine) and TBAs (tertiarybutylarsine) were used as group V precursors, and TMGa (trimethylgallium) and TMIn (trimethylindium) were used as group III precursors. The epitaxial surface was monitored *in-situ* by a spectroscopic ellipsometry (UVISEL-IR) attached to the reactor. We carried out spectroscopic and kinetic ellipsometry with a fixed angle of incidence, approximately 75°.

The experimental conditions, under which most ellipsometry measurements were performed, were as follows. Substrate temperature was 610°C and total pressure was 10^4 Pa (InGaAs/InP quantum wells described later were grown under the same condition). Photon energy used for kinetic ellipsometry measurement was 2.65 eV or 2.05 eV. The angle of incidence was calibrated frequently by measuring a standard Si substrate. The substrate rotation was used throughout the kinetic ellipsometry, the speed of which was either 79.2 rpm or 33.8 rpm. Time interval between data acquisition was typically 200 ms, which was short enough to do the kinetic analysis.

III. Results and Discussion

A typical example of source gas switching sequence for
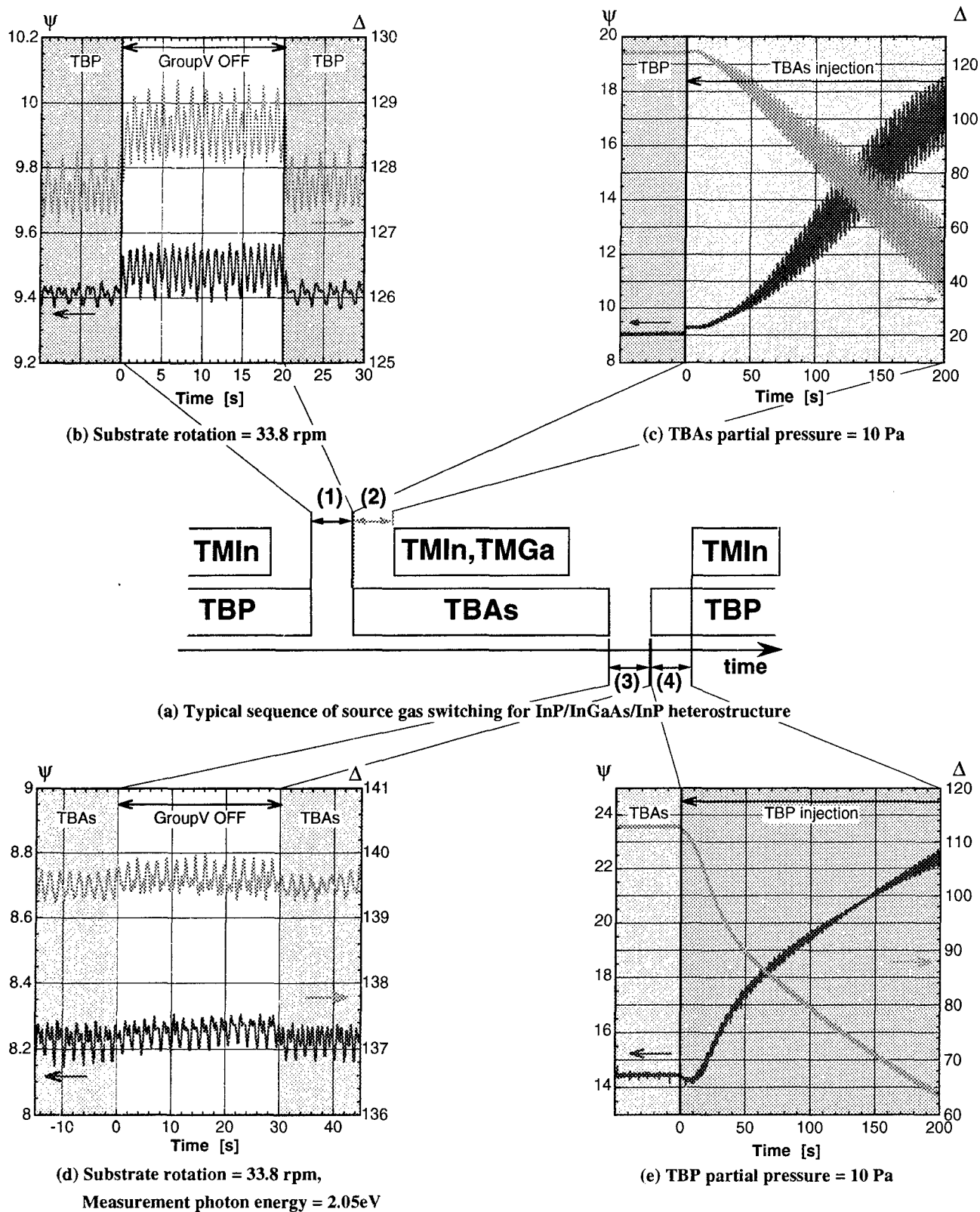
Fig. 1. Gas switching sequence (a) and ellipsometric signals (ψ and Δ) from InP (b and c) and InGaAs (d and e) surfaces, on which As-P exchange occurs by TBAs or TBP injection. Substrate temperature was 610°C, total pressure 10^4 Pa, substrate rotation 79.2 rpm (besides b and d), and measurement photon energy 2.65 eV (besides d).

Fig. 2. Ellipsometric signals (ψ and Δ) from InP surface where TBP is switched off several times (0.2sec, 0.8sec, 3sec, 10sec and 60sec). Measurement photon energy is 2.65eV, the angle of incidence 75.0°, and substrate rotation 79.2rpm.

Fig. 3. Ellipsometric signals (ψ and Δ) from InP surface where TBAs is substituted for TBP several times (0.2sec, 0.8sec, 3sec and 6sec). TBAs partial pressure is 10Pa, measurement photon energy 2.65eV, and the angle of incidence 75.1°.

InGaAs/InP quantum well growth is illustrated in Fig. 1 (a). Signals obtained from the ellipsometric measurement, ψ and Δ, at several different duration in the sequence are shown in Figs. 1 (b), (c), (d) and (e). The length of these periods decides the degree of arsenic-phosphorus exchange and the desorption of phosphorus on InP or arsenic on InGaAs. Characteristics of quantum structure very much depend on these parasitic effects. The signals from the InGaAs layer (d and e) were measured after a thick InGaAs layer was grown so as not to be affected by the underlying interface between InP and InGaAs.

Due to the substrate rotation, the signals change at a short period. This change is caused by anisotropy of the ellipsometric signals with respect to crystallographic orientations of the substrate as well as a small fluctuation of the incident angle. As compared with other optical probing techniques that measure reflectivity directly, the substrate rotation has little effect in ellipsometry.

From Fig. 1 (b), we notice that the switching the group V precursors off causes larger amplitude of signal oscillation. This phenomenon can be attributed to larger anisotropy of the InP surface when the group V precursors are shut off. The anisotropy is caused by surface reconstruction of InP through desorption of phosphorus or of P-containing species decomposed from TBP. Figure 2 shows the change of ψ and Δ with different group V switch-off time on InP. In Fig. 2, the transition from one surface state to the other is completed within 800 ms at this temperature. Therefore, if one intends to use the period (1) for purging excess phosphorus, 1 second is good enough. If this period is too long, depletion of phosphorus may occur; when it was over 15 seconds at this temperature, ellipsometric signals gradually shifted due to surface degradation of InP. Kinetic ellipsometry was found very useful for determining appropriate length of the switching periods, as shown above.

The injection of TBAs on InP causes an instantaneous change of the signals as shown in Fig. 1 (c). Then the signal stays at the same level for approximately 6 seconds, followed by a gradual but large shift after that. The amplitude of the signal vibration becomes notable simultaneously. The first abrupt change may be because of substitution of arsenic into surface phosphorus sites. The second gradual shift corresponds to diffusion of arsenic into the topmost InP layer. Because of large lattice mismatch between InP and InAsP, the surface becomes rough and anisotropic to result in the changes of the ellipsometric signals.

Figure 3 is to show how the InP surface exposed to TBAs recovers the original surface by switching back to TBP. As seen in the figure, the first instantaneous change by TBAs injection finishes in approximately 800 ms. The recovery time after TBAs is replaced by TBP is found to be about 30 seconds in the same figure. If the TBAs injection time was less than 6 seconds, the change of the surface state was reversible as in Fig. 3. However, when we injected TBAs on to InP surface more than 6 seconds, the amplitude of signal vibration became larger (see Fig. 1 (c)), and InP surface never came back to the original even if TBP was supplied. Therefore, the period (2) should not be longer than 6 seconds at this growth temperature.

In Fig. 1 (d), switching off TBAs on InGaAs surface causes little change of the ellipsometric signals. This means that the change of the InGaAs surface is negligibly small at least as compared to the sensitivity of this ellipsometric measurement. Nevertheless, it is possible to say that stopping TBAs supply is not enough to purge excess arsenic on InGaAs away at this temperature.

The injection of TBP on InGaAs in Fig. 1 (e) causes immediate change of the signals but, unlike before, they keep shifting without having a plateau. Illustrated in Fig. 4 is the results of the similar experiment as in Fig. 3; TBAs was re-injected after short

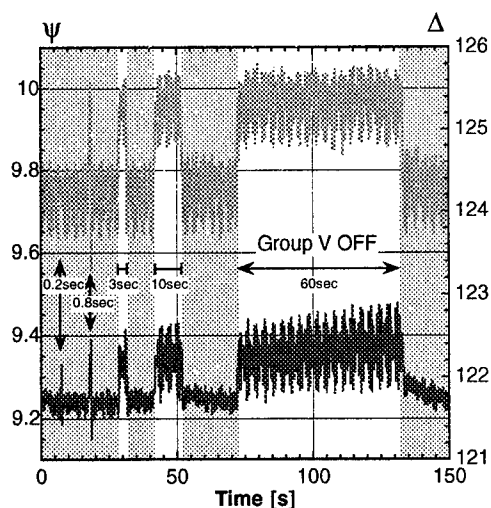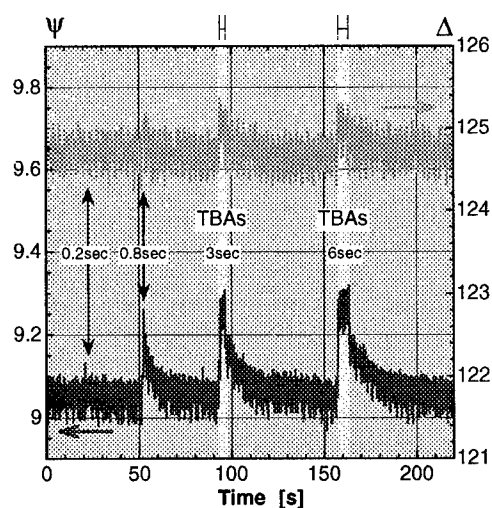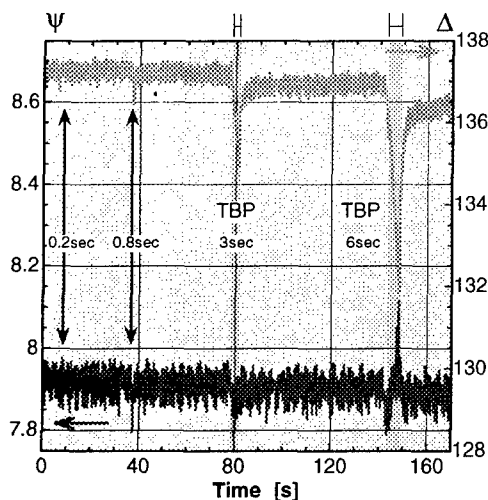Fig. 4. Ellipsometric signals (ψ and Δ) from InGaAs surface where TBP is substituted for TBA several times (0.2sec, 0.8sec, 3sec and 6sec). TBP partial pressure is 10Pa, measurement photon energy 2.05eV, and the angle of incidence is 74.9°.

Fig. 5. Measured PL peak energy and FWHM at 77K from single quantum wells prepared by using different pre-growth TBP injection time, namely, period (4) in Fig. 1 (a). Well width was intended to be 7 monolayers (~2.05 nm).

TBP injection on InGaAs. It is found in the figure that the surface does not recover original state even after 0.8 seconds of TBP injection (see Δ). Longer TBP injection results in larger difference between the values before and after the TBP injection. This suggests that the diffusion of phosphorus into InGaAs starts right after the TBP injection, thus causing irreversible changes to the InGaAs surface and layers underneath. Therefore, the period (4) needs to be as short as possible to obtain an abrupt interface.

In order to verify this, we grew InGaAs/InP quantum wells using different periods of the pre-growth time (4) for TBP, and measured peak energy and FWHM (full width at half maximum) of photoluminescence (PL) at 77K from the quantum wells. The results are shown in Fig. 5. In the figure, the PL peak energy becomes large with the preceding TBP injection time. The shift is notable even at 1 second. The FWHM becomes wider at the same time with the TBP time. These changes can be explained as follows; by the TBP pre-growth flow, arsenic in a few monolayers of InGaAs from the surface was exchanged with phosphorus. Therefore, the width of the wells became narrower and the interfaces became obscure. This result is consistent with the above ellipsometry observation.

IV. Conclusion

We have found that in-situ monitoring of arsenic-phosphorus exchange at interfaces of InGaAs/InP heterostructures in MOVPE is possible by kinetic ellipsometry. We have been able to determine appropriate length of periods in the gas switching sequence at the interfaces by utilizing information from the in-

situ ellipsometric observation. It turns out to be very helpful for the optimization of gas switching sequence to secure interface abruptness.

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THE EFFECT OF IMPURITY PROFILE AND OXYGEN ON THE PEAK-TO-VALLEY RATIO OF HETEROSTRUCTURE INTERBAND TUNNELING DIODES (HITD).

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Introduction

We present work on the performance of HITDs. SIMS and other experimental techniques (TEM, and Polaron) are used to study the effect of dopant compensation and dopant diffusion into the well regions, on the I-V characteristic and the peak to valley ratio (PVR) of the HITDs. The data shows an exponential dependence of the PVR on Oxygen concentration in the sample. It also shows that the presence of doping impurities in the well region (which is determined using SIMS analysis) has a dramatic effect on the PVR and the peak current density. Finally, it is mentioned that simulated results confirm the effect of these two mechanisms on the performance of the HITDs and an attempt on studying each separately is made.

Background

Resonant interband tunneling diodes first proposed by Sweeny and Xu[1] have demonstrated high peak to valley ratios (PVR)[2], and have a potential to produce analog and digital circuits with reduced complexity and size. This is very desirable in future circuits since the semiconductor industry is moving towards smaller features and circuits. Several memory and logic devices (SRAMs, XNORs, etc.) have been demonstrated[34] which use tunneling diodes. The challenge has been to obtain repeatably high PVRs as a function of material parameters and growth[5]. The material system considered in this paper is InGaAs/InAlAs/InP in which HITDs having the highest reported PVR of 144 (ref. 2) were made. We show that doping levels and impurities in the quantum wells play an important role in determining the PVR and current densities of the diodes.

The main factors that this paper addresses are: the presence of oxygen in the epitaxial layers (and therefore the compensation of dopants), dopant diffusion through the various heterojunctions (specifically Be diffusion) and the presence of impurities in the double quantum well (DQW) region. The experimental results that we present are validated with simulated results that model the effect of dopant compensation and diffusion on the PVRs and the peak current densities (Jp)

Experimental

The HITDs are MBE grown at 465 °C. The substrates are epi-ready semi-insulating InP. The growth starts with a 5000Å $In_{0.522}Al_{0.478}As$ buffer layer (undoped), we then grow a 2000Å $In_{0.532}Ga_{0.468}As$ Si-doped ($1-2 \times 10^{19}$ cm^{-3}) layer for contact purposes. The next layer is 2000Å of Si-doped ($1-2 \times 10^{19}$ cm^{-3}) $In_{0.522}Al_{0.478}As$, which is followed by the DQW region. This not intentionally doped (nid) region consists of two 40Å $In_{0.532}Ga_{0.468}As$ wells that are separated by a 20Å $In_{0.522}Al_{0.478}As$ barrier layer . The thicknesses of the barriers and quantum wells were optimized for maximum PVR and Jp. Finally 2000Å of Be-doped (1×10^{19} cm^{-3}) $In_{0.522}Al_{0.478}As$ and a 200Å cap of Be-doped $In_{0.532}Ga_{0.468}As$ (top contact layer) are grown. The wafers are then processed into circular mesas (wet etched) of different diameters varying from 50μm to 200μm. The contact metals are Ti/Pt/Au for the p-type contact and Ni/Ge/Au for the n-type contact. The band structure and cross section of these devices are shown elsewhere.[67]

The PVR of these diodes varies from wafer to wafer because of variations in the doping profiles and background impurity levels. Figure 1 shows a typical I-V curve of a HITD having a PVR of 44. The diode shown below is a 50μm diameter mesa with Jp = 2.24×10^3 A/cm^2.
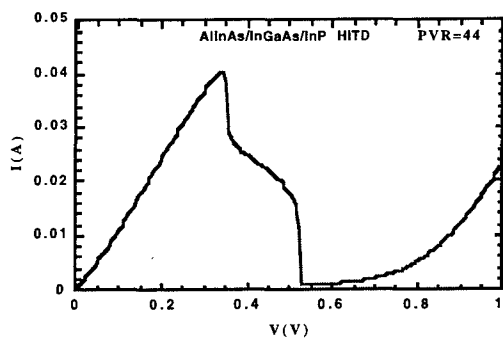
Figure. 1 I-V curve of an HITD showing J_p=44 mA and J_v= 1mA resulting in a PVR of 44.

The presence of oxygen in the sample has a dramatic effect on the PVR of the HITDs. Fig. 2 shows a SIMS analysis for two different samples grown within a few days of each other. One has a PVR = 4 and a Jp = 8.41 A/cm^2, while the other has a PVR = 47 and Jp = 713 A/cm^2. The oxygen distribution in the two diodes is approximately uniform and differs by a factor of 2.5 (0.8 X10^{18}cm^{-3} for PVR = 47, and 2X10^{18}cm^{-3} for PVR = 4). This difference decreases the PVR by one order of magnitude, and Jp by two orders of magnitude. Carrier compensation both in the wells and access regions thus affects the PVR.

Also observed is a slight diffusion of Be into the DQW region in both samples. Both wells contain diffused Be yet a high PVR (i.e. 47) is obtained for one diode. This shows that the greater PVR degradation effect is the oxygen concentration. The lower PVR sample has higher oxygen which compensates the impurities in the DQW region.
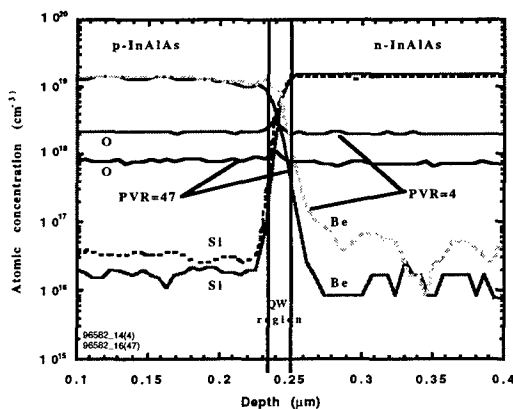
Figure 2. SIMS analysis of two different samples grown within a few days of each other. An oxygen concentration increase of 2.5 times decreases the PVR by an order of magnitude.

Collecting SIMS data from several samples with different oxygen content we obtain the plot of PVR versus oxygen concentration shown in Fig. 3. We find a clear exponential dependence of PVR on O concentration.

The presence of oxygen is attributed to the well-known high reactivities of Al containing materials (InAlAs) and Be[8] which is the p-dopant used in these structures. Another source of oxygen was found to be the hot PBN crucible. Polaron measurements of free carrier profiles agree with the SIMS measurements of atomic concentration by adjusting Si or Be profiles with the oxygen concentration.
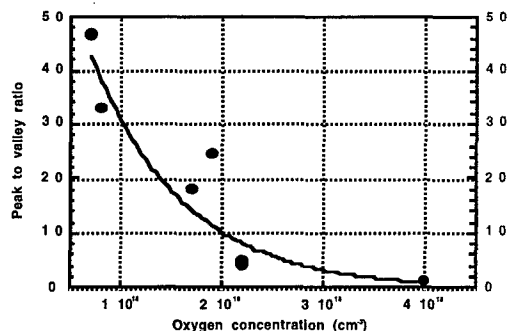
Figure 3. Plot of PVR versus O concentration. Curve fitting gives us a clear exponential dependence.

Using SIMS, Polaron and TEM analysis we also show the effect of impurity diffusion on the PVR and peak current density (Jp). Fig. 4 shows the SIMS analysis of a stack of two back to back HITDs (npn). Essentially the heterostructure stack is the same as the one described above except that after the 2000Å p+ InAlAs layer another DQW is grown, followed by a 2000Å n+ InAlAs layer, which is capped by a 200Å n+ InGaAs layer for contact purposes.

Be is known to have high diffusivity in III-V semiconductors. It introduces impurities into the DQW region, and "smears" the interfaces between the InGaAs wells and InAlAs barriers.
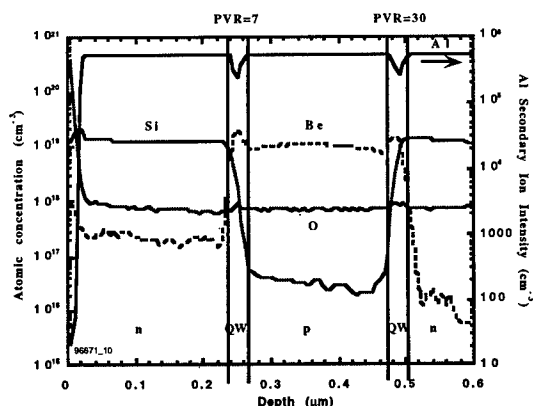
Figure 4. SIMS analysis of an n-p-n HITD. We can clearly see that the level of Be diffusion in the top diode. The Be level in that n-layer is around $5 \times 10^{17} cm^{-3}$, as compared to the bottom n-layer where it is at detection level.

The bottom diode (p on n) has a high PVR = 30 and a Jp = 7.64 A/cm², while the corresponding values for the top diode (n on p) are PVR = 6.8 and Jp = 0.56 A/cm². The Be signal in figure 4 clearly shows diffusion of Be in the top Si doped layer making that junction less abrupt and possibly smearing the quantum wells. TEM cross sections confirm this data by showing the bottom diode DQW interfaces to be very sharp, whereas the top diode DQW interfaces are very "hazy." The oxygen concentration, on the other hand, is constant throughout the structure. Therefore, in this case it the Be diffusion degrades the PVR (by carrier compensation and/or interface roughening). The presence of acceptors the QW region reduces the number of carriers available for conduction and thus the hole tunneling current and thus J_p. In addition to the presence of impurities in the wells - and as mentioned in ref. 5 - interface abruptness greatly affects the PVR because it results in high valley currents due to scattering mechanisms.

Simulations run on these structures, show that both compensation of dopants and impurities in the DQW region play an important role. The simulation trends show that the impurities in the well have a large on the PVR degradation. The exponential dependence seems to be related more to impurities rather than oxygen compensation. The dependence of PVR on oxygen seems to be linear or a second order polynomial at the most. The dependence of PVR on the presence of acceptors in the well (we observe that Si is not diffusing appreciably) has a clear exponential dependence. This implies that figure 3 might be showing the combined effect of both mechanisms. We are conducting further detailed SIMS analysis and correlating it with simulation results to try to decouple the effects in order to determine their relative effects.

Conclusion

In conclusion, experimental data (SIMS, TEM and Polaron) shows that compensation of carriers due to the presence of oxygen and dopants in the DQW of the HITDs have a large effect on the performance of these devices. Basically they degrade the PVR and Jp of the HITDs. Simulation tends to confirm this data. The challenge is to decouple these effects to determine the magnitude of PVR degradation.

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SUBSTRATE CRYSTALLINITY AND THE PERFORMANCE OF INP-BASED PSEUDOMORPHIC HIGH ELECTRON MOBILITY TRANSISTORS

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I. Abstract

We demonstrate a novel technique by which to measure the degree of crystalline perfection across semi-insulating InP substrates and show that the substrate perfection influences the crystallographic perfection and the electrical properties of subsequently deposited epitaxial layers. The substrate characterization technique is based on triple axis diffraction omega scans which are performed across the entire wafer area. Substrates with localized defective spots as well as overall substrate perfection are quantitatively measured. Pseudomorphic high electron mobility-type structures with strained $In_{0.60}Ga_{0.40}As$ channels and nominally lattice-matched $In_{0.52}Ga_{0.48}As$ buffer and supply layers were grown by molecular beam epitaxy and characterized by double and triple axis diffraction, Hall effect, and x-ray topography. Structures grown on high quality regions of the substrate exhibit sharper diffraction features and higher mobilities than those grown on low quality regions and we observe that there is a strong correlation between the level of diffuse scattering determined by triple axis diffraction and the channel mobility.

II. Introduction

The influence of substrate perfection on epitaxial layer material or electrical quality has not been widely studied in InP-based systems. In GaAs structures, Barnett et al., [1] demonstrated that misfit dislocations with specific Burger's vectors are nucleated from individual substrate threading dislocations. We recently showed [2] that the perfection of GaAs substrates strongly influences the mechanical stability of strained pseudomorphic $In_{0.2}Ga_{0.8}As$ channels grown on the substrates as part of a pseudomorphic high electron mobility transistor (pHEMT). More importantly, the channel conductivity of the structures grown on high quality substrates was consistently higher than for low quality substrate structures.

InP crystal growth is usually considered to be at a less advanced stage than GaAs. The low stacking fault energy, low heat conductivity, low mechanical strength, and higher group V equilibrium vapor pressure (all relative to GaAs) [3] can make high quality InP substrates more difficult to grow. This study was initiated to study the relationship between substrate perfection and the electrical properties of pseudomorphic structures grown on semi-insulating InP.

Several non-destructive characterization techniques were employed to determine the crystalline quality of the as-grown substrates. One rather novel technique which proved to be very

useful for the characterization of GaAs substrates is referred to as "omega (ω) mapping"[4]. This measurement involves triple axis diffraction (TAD) rocking curves taken from different locations on the wafer. Similar measurements can be performed using more widely utilized double axis diffraction (DAD) measurements, but DAD widths are intrinsically wider, especially in the tails of the Bragg reflections. These tails can obscure important structural information such as subsurface damage. For example, the TAD full width at half maximum (FWHM) from the highest quality GaAs substrate is about 4.0 arcsec and the width at 0.001 of the maximum is 17.9 arcsec. For comparison, the double axis measurements provide a FWHM of about 15 arcsec and 212 arcsec at the 0.001 maximum. By plotting the TAD full width as some maximum as a function of wafer position, one clearly maps out regions of high and low quality across the substrate. Similar measurements were performed across subsequently deposited epitaxial layers to study the relationship between substrate and epitaxial layer structural quality. We also performed x-ray topography, double axis diffraction (with simulations) and Hall measurements.

III. Experimental Procedure

Both 50 mm and 75 mm commercially available semi-insulating InP substrates were employed. Molecular beam epitaxy was used to grow pHEMT structures with lattice matched ($In_{0.52}Al_{0.48}As$) buffer and barrier layers and a strained $\approx$ 20 nm $In_{0.60}Ga_{0.40}As$ channel and top contact layer. Silicon delta doping in the barrier was employed to introduce carriers into the channel.[5]. The InP substrates were characterized by the TAD ω-maps and x-ray topography. For the TAD measurements, a modified Bede D^3 diffractometer was used with an effective beam size of 2x5 mm^2. For the 50 mm diameter substrates, (004) reflections were taken at 5 mm increments across the surface in both the "x" and "y" directions. For the 75 mm diameter wafers, measurements were taken at 7.5 mm increments; the wafer map typically consisted of 70-85 scans. The x-ray topography measurements used a Bede 150 diffractometer with a curved crystal collimator which was miscut to provide a 1.5° incidence angle of the slit collimated x-ray beam and the

collimator surface and diffracted from (224) planes.

IV. Results and Discussions

Examples of substrate ω-maps (FWHM) from 50 mm substrates are shown in Fig. 1. Fig. 1(a) represents a map from a high quality substrate. On this gray-scale map, light colors represent a lower FWHM and darker colors represent a higher FWHM. The scale for these figures ranges from 2 to 8 arcsec.
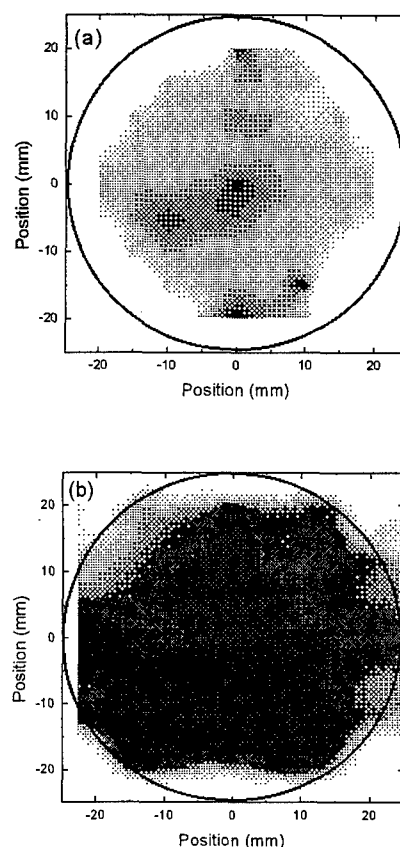
Figure 1. ω -maps from (a) high quality and (b) low quality InP substrates.

Higher FWHM values are set to the 8 arcsec limit. Fig. 1(a) shows an average FWHM of 5.1 arcsec which compares to the best semi-insulating GaAs of 4.0 arcsec.[6] Fig. 1(b) is from another substrate and the obvious dark areas here show that there are extensive regions of poor crystalline quality. The average FWHM from this substrate is 6.8 arcsec. The overall trend shows that nearly identical wafer maps are obtained from substrates of the same boule and

that wafers from different boules grown by the same manufacturer are very similar, too. It needs to be mentioned here that crystal quality is only one parameter which must be satisfied for development of wafers suitable for electronics applications. Semi-insulating behavior and reasonable surface finish are other requirements.

The properties of the pHEMT structures grown on the different substrates is also rather revealing. Figure 2 shows (004) double axis diffraction scans from pHEMT structures grown on the different substrates. The structure grown on the high quality substrate show much sharper peaks and fringes. By contrast, the structure grown on the low quality substrate exhibits a diffraction scan with less pronounced features.
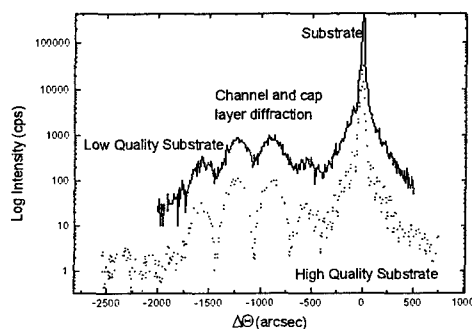
Figure 2. (004) double axis diffraction scans of pHEMT structures.

Figure 3 shows the first experimental diffraction scan and a scan generated from a dynamical x-ray diffraction model. The acceptable match between the two scans shows that these structures can be grown with a crystallographic perfection to the resolution of double crystal diffraction techniques.
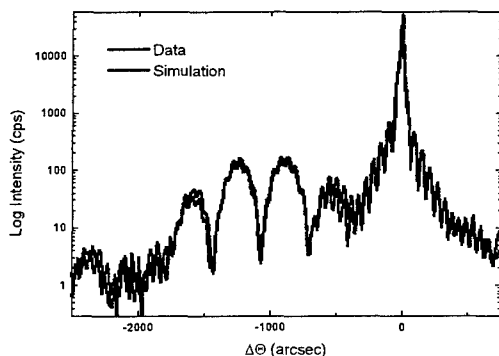
Figure 3. Double axis experimental scan and simulated scan from structure grown on the high quality substrate.

To better establish the crystalline perfection of the individual layers, TAD rocking curves were performed across the ≈ 20 nm $In_{0.60}Ga_{0.40}As$ channel diffraction peaks as shown in Fig.4.
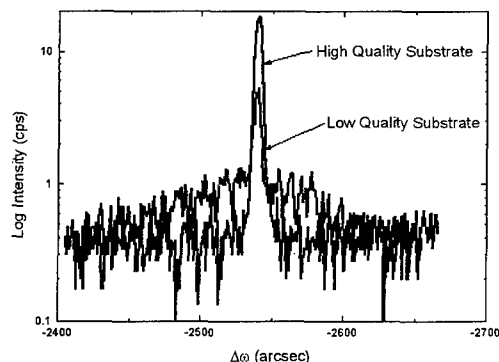
Figure 4. ω scans taken across the $In_{0.6}Ga_{0.4}As$ channel (004) diffraction peaks.

Again, there is a clear difference between the diffraction scans from the two samples. The layer(s) grown on the low quality substrates show two superimposed peaks. There is a sharp specular peak and a broad diffuse peak. Kaganer. et al. [7] modeled this behavior and demonstrated that the specular peak is from coherently diffracting material and the diffuse peak stems from regions of the layer which are distorted by, for example, misfit dislocations. For epitaxial structures grown on GaAs substrates, we have determined that such broadening is due to either misfit dislocations [8] or stacking faults [9]. In the present case, we have not yet positively identified the origin of the diffuse scattering, but we clearly observe that pseudomorphic structures grown on substrates with high ω-map levels always exhibit broadened TAD peaks. We also occasionally notice that broad TAD scans are observed on substrates which show good crystalline quality. We suspect that the surface of these wafers may be rough, contaminated, or otherwise act as the origin for crystallographic defects in the layers.

The electrical properties of layers grown on the low and high crystalline quality substrates also tend to exhibit different electrical properties. For example, structures grown on high quality substrates typically exhibit channel mobilities on the order of 10,000 $cm^2/V·s$ whereas the mobility of layers which exhibit the broadened layer dif-

266

fraction peaks can exhibit mobilities as low as 1,000 cm²/V·s.

V. Summary

TAD ω-maps provide an useful means to non-destructively characterize InP substrates for subsequent epitaxial growth. Substrates which show low and uniform FWHM values provide an appropriate template for growth of pseudomorphic epitaxial device structures. Substrates which show high values have defective epitaxial layers both in terms of crystalline properties and electrical behavior. Further work elucidating the origin of the diffraction peak broadening is underway.

VI. Acknowledgments

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STRUCTURAL CHARACTERIZATION OF DISTRIBUTED FEEDBACK LASER DIODES WITH UNDULATION OF STRAINED - LAYER MQW

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Abstract

The InGaAsP/InGaAs strained-layer multiple quantum well (SL-MQW) structures for 1.55 µm distributed feedback laser diodes have been grown by low-pressure metalorganic vapor phase epitaxy (LP-MOVPE). The undulation or deformation of SL-MQW layers grown on the corrugated InP substrates has been observed, and it was dependent upon AsH₃ partial pressure and heat-up time prior to the 1st active layer growth. The structural qualities of SL-MQW are discussed in-depth using DCXRC, PL, TEM, and SEM.

I. Introduction

The 1.3 µm or 1.55 µm InGaAsP/InP strained-layer multiple quantum well (SL-MQW) distributed feedback laser diodes (DFB-LD) have been extensively studied as light sources for long-haul, high-speed optical telecommunication systems [1]. Much work has been performed on thermal deformation of surface corrugations on substrates [2,3]. Recently, lateral thickness modulations have been observed in the strain-compensated InGaAsP/InGaAsP MQW [4-6], the strained-compensated GaInAs/GaInAs MQW [7], and InGaAs/GaAs superlattices structures [8], grown on no corrugated substrates. One may observe the undulation or deformation of SL-MQW layers in the growth of 1st active layers on the corrugated substrates prior to the fabrication of DFB-LD. Such phenomenon deteriorates the device performances, such as reliability and thermal stability of DFB-LD. In our study, we observed that this undulation or deformation of the layer grown on the corrugated substrate was dependent upon AsH₃ partial pressure and heat-up time prior to the 1st active

layer growth. We found the optimum initial growth conditions for removing such an undulation or deformation of SL-MQW layers, and will discuss the influence of undulation or deformation on the device performance.

II. Experiments

The epitaxial layers were grown on (100) InP substrates with 1st-order corrugation grating, formed by conventional holographic interference exposure method, using LP-MOVPE. The layer structure consists of compressively strained MQW (InGaAs(well)/ InGaAsP(barrier), 10 periods) as an active layer emitting at 1.55 µm, and 1.24-µm InGaAsP waveguide layers. The structural qualities of SL-MQW layers were analyzed in-depth using DXRD, PL, TEM, and SEM. We fabricated the high speed DFB-LD in order to see the influence of such an undulation.
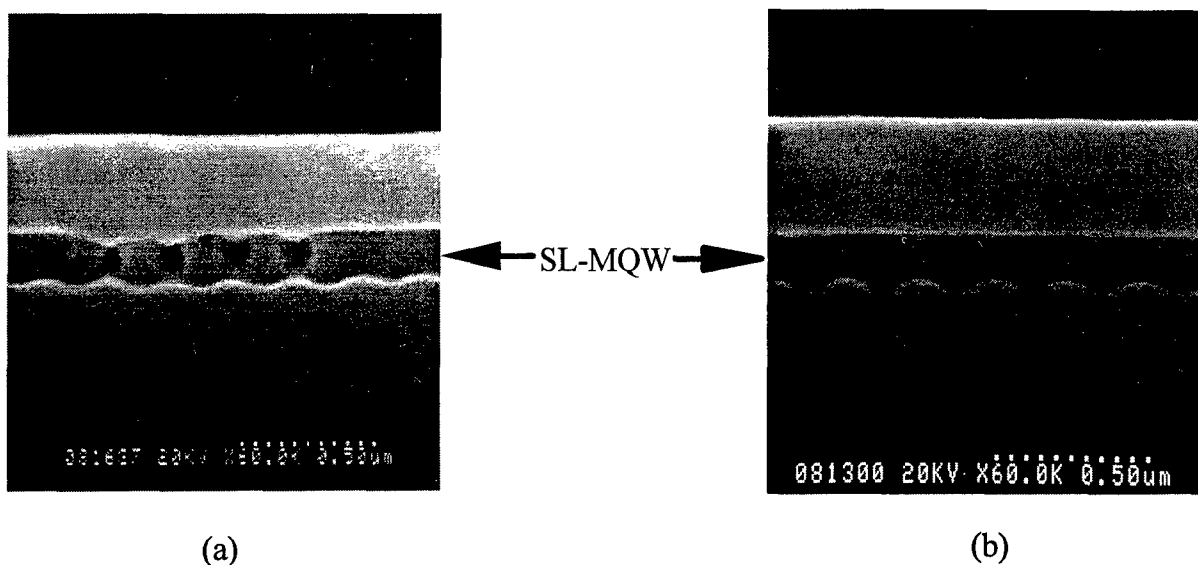
Fig. 1 SEM cross-section view of (a) undulation and (b) no undulation of SL-MQW layers.

III. Results and Discussion

We observed the undulation or deformation of SL-MQW DFB-LD structure grown on the corrugated substrates with the initial growth conditions of both AsH₃ partial pressure of 1.5×10^{-3} Torr and heat-up time of 5 min, as seen in a cross-sectional photograph (Fig. 1(a)).

Double crystal X-ray rocking curves (DCXRC) were obtained a high resolution double-crystal diffractometer (Bede DCC 300) equipped with a rotating-anode CuKα radiation and a Si(220) channel-cut collimator. Symmetric (004) reflection rocking curves were recorded in the Bragg case. From the experimental rocking curve in Fig. 2(a), satellite peaks of SL-MQW layers around InP substrate peak are very broad and not clear, indicating the very poor epitaxial quality of MQW, due to the dislocations indicated by arrows in the TEM bright field image (Fig.3). In the TEM image, we observed the dislocations generated at the concave of MQW, as reported by Jang et al.[9]. Dislocations appear as early as the fifth period of MQW as seen on the cross-sectional view. This is mainly due to the excess accumulation of strain in a

given growth condition.

We could not observe PL signal for the sample of layer undulation due to the poor layer quality. However, this undulation was removed by controlling the AsH₃ partial pressure and heat-up time, as observed by SEM photograph (Fig. 1 (b)). We found the optimum initial growth conditions, such as AsH₃ partial pressure of 9×10^{-4} Torr and 3 min heat-up time. In the DCXRC of sample with no layer undulation in the Fig. 2(b), several satellite peaks are sharp and comparable to the peaks of Fabry-Perot structure without first-order corrugation grating. Unlike the layer undulation, the clear and sharp PL spectrum were observed, showing good layer quality.

Figure 4 shows typical static characteristics, such as current - voltage (I-V), current - power (I-L), and differential quantum efficiency (i.e., slope efficiency, SE), of DFB-LD fabricated with undulation or without undulation of SL-MQW layers. The differential quantum efficiency was 8% for the layer with undulation (Fig. 4(a)), but for the layer without undulation in Fig. 4(b), quantum efficiency increased to 16%, indicating better device properties.

269
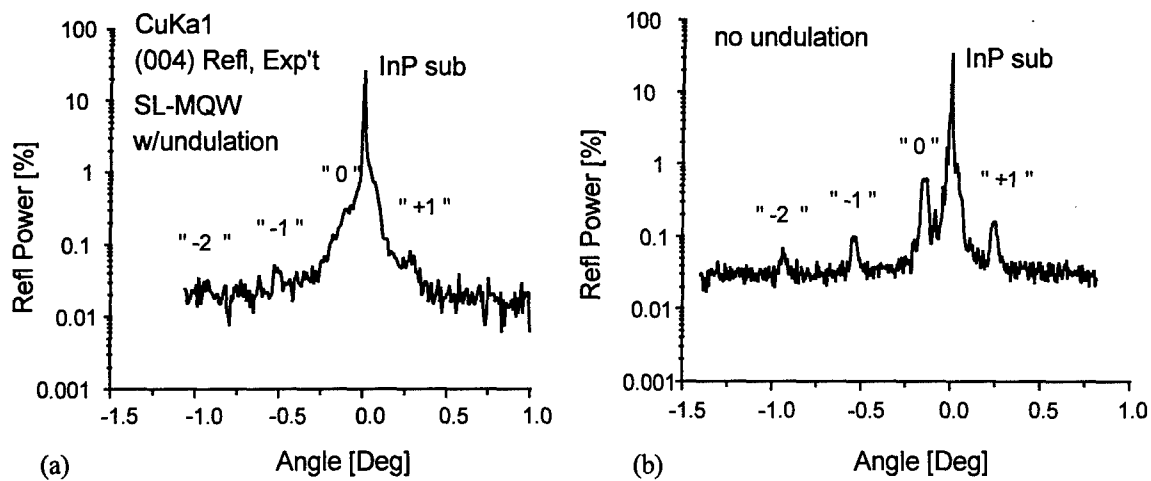
Fig. 2 Double Crystal X-ray Rocking Curves : (a) undulation and (b) no undulation of SL-MQW layers. Satellite peaks of SL-MQW layers with undulation are very weak due to the dislocations.

Fig. 3 TEM bright field image of the DFB - LD structure showing undulation of SL-MQW layers.
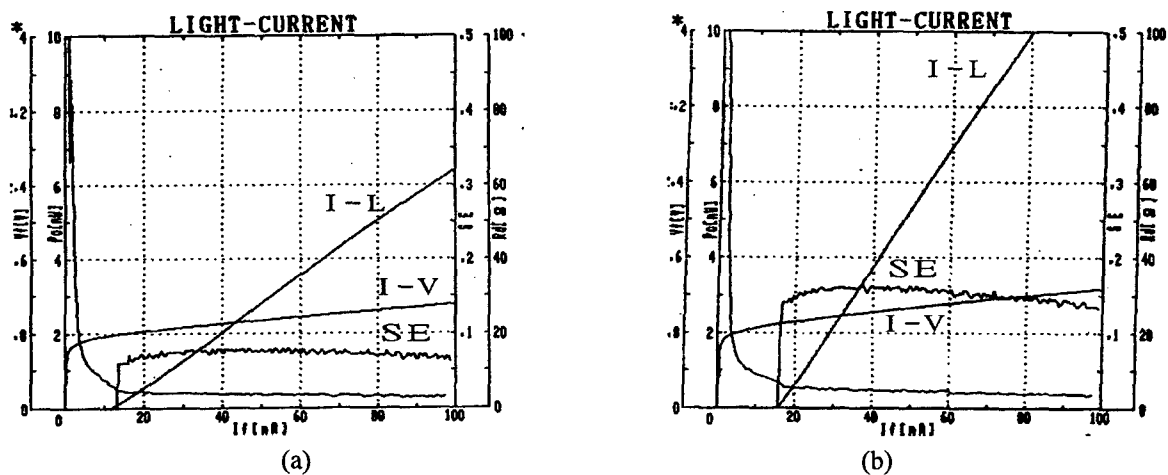
Fig. 4 Static Characteristics (I-L and I-V) of DFB-LD : (a) undulation and (b) no undulation of SL-MQW layers.

IV. Conclusion

The InGaAsP/InGaAs SL-MQW structures for 1.55 μm distributed feedback laser diodes have been grown by LP-MOVPE. The undulation or deformation of SL-MQW layers grown on the corrugated InP substrates has been observed, and it was dependent upon AsH_3 partial pressure and heat-up time prior to the 1st active layer growth. Based upon our results, the optimum initial growth conditions,prior to the 1st active layer growth, in order to remove such an undulation or deformation of SL-MQW layers, were AsH_3 partial pressure of 9×10^{-4} Torr and 3 min heat-up time. The differential quantum efficiency was 8% for the layer with undulation, while for the layer without undulation, quantum efficiency increased to 16%, indicating better device properties.

Acknowledgments

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WARPAGE OF InP WAFERS

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Introduction

InP wafer warpage induced during its processing has been investigated. Magnitude and shape of wafer warpage caused by surface damage, which is presumed to give tensile stress to wafer, was influenced by its dopant. After MOCVD growth some wafer warpage changed but only a little and smooth surfaces of epi-layer were achieved.

I . Origins of Wafer Warpage

There are several origins of wafer warpage which can be induced during its processing as shown in Fig. 1 as follows ;

① Inner stress of crystal which is released after slicing makes wafer bend.

② During slicing the course of the slicing blade through the cystal is not straight due to its displacement.

③ Stress by mechanical damage on the wafer surfaces causes wafers to bend. (Twymann effect)

④ Stress by heat treatment causes wafers to bend.

To reduce wafer warpage, it is necesarry to eliminate each of these origins.

Fig. 1. InP wafer processing. Figure in a circle corresponds to warpage origins ①~④.

II . Experimental

Sn, S, Fe and Zn doped ϕ 2" (100) InP LEC single crystals were used. Their properties are as folows ;

Sn doped ; carrier concentration is $(0.8\sim3)\times10^{18}cm^{-3}$, EPD is $<5\times10^{4}cm^{-2}$.

S doped ; carrier concentration is $(3\sim6)\times10^{18}cm^{-3}$, EPD is $<5\times10^{3}cm^{-2}$.

Fe doped ; resistivity is $>10^{7}\,\Omega cm$, EPD is $<5\times10^{4}cm^{-2}$.

Zn doped ; carrier concentration is $(1\sim2)\times10^{18}cm^{-3}$, EPD is $<5\times10^{4}cm^{-2}$.

These crystals were processed as shown in Fig. 1, where slicing was done by I.D. saw, #1200 Al2O3 abrasives were used in lapping.

Epitaxial growth conditions were as follows ;
method ; MOCVD
substrate ; Sn doped InP
growth temperature ; 715℃

growth rate ; 1.0 μ m /hr

$\mathrm{I\!I\!I}$/V ratio ; 96

growth thickness ; 1.0~2.0 μ m

An interferometer and a stylus surface profiler was used to measure wafer warpage after each stage of the processing.

To measure mechanical properties of these InP wafers a Vickers hardness tester was used, where 50~500g was loaded.

$\mathrm{I\!I\!I}$. Results and Discussion

As sliced or lapped wafers, both surfaces of which were mechanically damaged, were saddle-shaped as shown in Fig. 2, which is similar to in the case of GaAs wafers.[1] After removing wafer surface layers by H_3PO_4-H_2O_2 etchant as much as 2 μ m, the saddle-shaped warpage has vanished.

Then several doped as cut and etched wafers with 520 μ m thickness and less than 5 μ m warpage were processed as follows ;

① Front surface (100) lapped ; 30 μ m surface layer removed.

② Back surface (-100) lapped ; 30 μ m surface layer removed.

③ Etched ; 20 μ m thickness reduced.

The following results were found (Fig.3) ;

(1) after (100) lapped all wafers were deformed

Fig. 3. Warpage of several doped InP wafers ; ① as cut and etched, ② after (100) lapped, ③ after (-100) lapped, ④ after etched
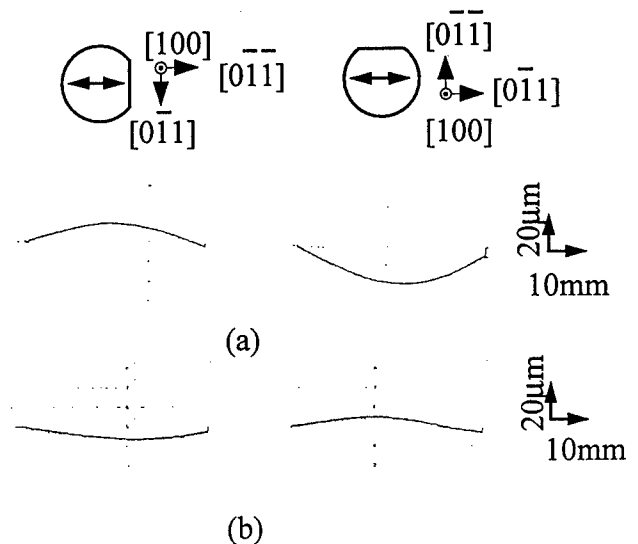
Fig. 4. Warpage of (100) and (-100) lapped InP wafers ; (a) S doped, (b) Zn doped

Fig. 2. Saddle-shaped InP wafer

(as lapped, 2 μ m/fringe)

273

convex, (2) magnitude of (100) lapped wafer warpage depended on its dopant such as Fe>Zn>S~Sn, (3) after (-100) lapped all wafers were saddle-shaped deformed, where Sn, S or Fe doped wafers are convex in the (011) direction and (0-11) concave, on the contrary Zn doped was (011) concave and (0-11) convex (Fig.4), (4) after etching all wafers' warpage recovered approximately their initial states.

The mechanism of processing brittle materials, for example quartz, Si, GaAs, InP and so on, by means of fixed or free abrasives such as slicing or lapping is presumed to be crack and fracture induced by indentation of abrasives. (Fig.5)
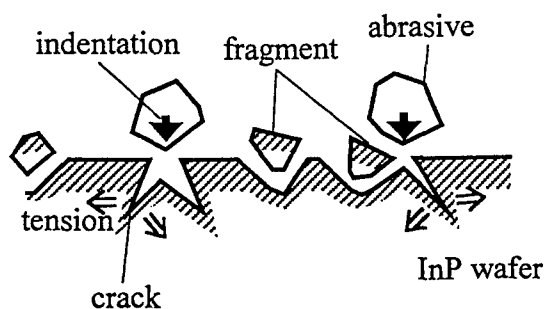
Fig. 5. Mechanism of processing by abrasive indentation.

So Vickers-indented InP wafers which were prepared to measure their hardness were etched by Huber etchant (20sec., at R.T.) to reveal micro cracks or propagated dislocations near the indentation mark. Two examples of optical micrographs of them are shown in Fig.6. Many of indentation marks were accompanied with cracks from the corners of them along $\langle 110 \rangle$ or $\langle 1\text{-}10 \rangle$ which are perpendicular to cleavage surfaces of zinc blende crystals. As for S, Sn, or Fe doped crystal $\langle 110 \rangle$ cracks tended to be longer than $\langle 1\text{-}10 \rangle$ ones as shown in Fig.6 (a). The length of the latter were largely scattered or even zero on

some samples, tendency of which is similar to in the case of GaAs.[2]

On the contrary, as for Zn doped $\langle 1\text{-}10 \rangle$ cracks tended to be longer than $\langle 110 \rangle$ ones, and accumulation of slip lines pararell to $\langle 1\text{-}10 \rangle$ spreaded X-shaped around the indentation mark as shown in Fig.6 (b).

(a)   (b)
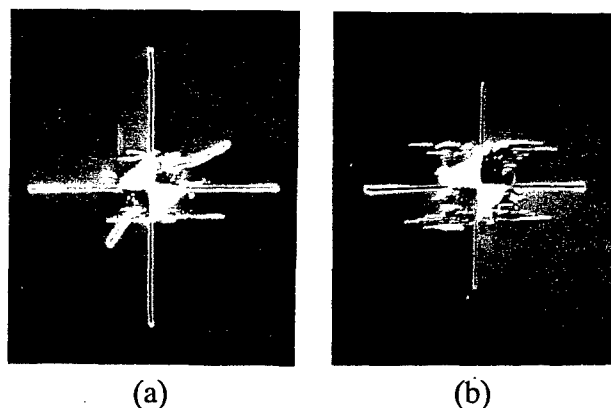
Fig. 6. Vickers indentation mark on InP polished wafers ; (a) S doped, (b) Zn doped, (load 100g, magnification ×400, crystalographic orientation ; vertical $\langle 110 \rangle$, hirizontal $\langle 1\text{-}10 \rangle$)

From these results asymmetry of plasticity along (100) surface and its dopant dependence could be presumed. As for S, Sn, or Fe doped crystal tensile deformation along (100) surface could be easier along $\langle 110 \rangle$ direction than $\langle 1\text{-}10 \rangle$.

When tensile stress is applied, the behavior of material to releave it is classified into two types ; One is plastic deformation, and the other is brittle fracture.

So if the stress is applied along (100) surface of S, Sn, or Fe doped crystal by indentation of abrasives, plastic tensile deformation along $\langle 110 \rangle$ could occur preferably to along $\langle 1\text{-}10 \rangle$. Then wafer warpage along $\langle 110 \rangle$ is bigger than $\langle 1\text{-}10 \rangle$.

And so if the stress is applied along both of (100) and (-100) surfaces, wafer shape is convex in $\langle 110 \rangle$ direction because plastic tensile

274

deformation along ⟨110⟩ is bigger on (100) surface than on (-100), while wafer is concave in the ⟨1-10⟩ direction because of on (-100)>on (100) along ⟨1-10⟩. Then the wafer is deformed saddle-shaped.

On the other hand, brittle fracture along ⟨110⟩ could occur preferably to along ⟨1-10⟩. So more ⟨110⟩ cracks could be formed on (100) surface.

But in the case of Zn doped crystal the deformation dependence on crystal orientation would be contrary, so tendency of wafer shape or crack occurrence should turn to be in reverse.

As for dopant dependence of warpage magnitude it could be presumed to have relation to plasticity of crystal. Vickers Hardness results are shown in Fig.7. The harder crystal would be, the less plastic deformation should become. The hardness order, S~Sn>Zn>Fe, is contrary to the warpage order, Fe>Zn>S~Sn.

To make clear the dopant dependence of plastic deformation or crack occurrence behavior of dislocations in InP crystal should be investigated. Further study is needed, such as in the case of GaAs.[3]

Warp before and after MOCVD growth is shown in Fig.8. All wafers were from the same crystal.

Some of wafer warp were changed, but only a little, and no dependence of wafer position in the crystal was found.

After epitaxial growth no irregularity on InP wafers such as cross-hatch pattern was found and smooth surfaces were achieved.
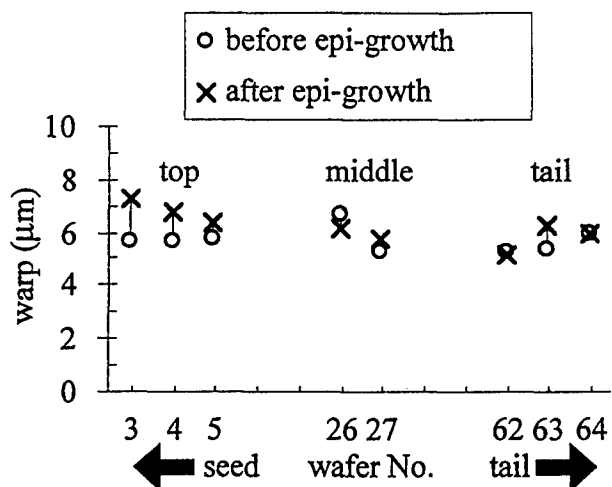
Fig. 8. InP wafer warpage before and after MOCVD growth.

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Fig. 7. Vickers Hardness of InP wafers   275

EFFECT OF GROWTH CONDITIONS ON THERMAL STRESS DEVELOPMENT IN HIGH PRESSURE LEC GROWN InP CRYSTALS

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I. INTRODUCTION

One of the critical issues associated with high pressure liquid-encapsulated Czochralski (HPLEC) growth of InP crystals is the high dislocation density, that is believed to be related to the thermal stress in the crystal. After Jordan's work on thermal stresses in GaAs and InP crystals (1), decreasing axial temperature gradient at the melt/crystal interface is considered to be important to control and reduce the dislocation desity in the crystal. Various measures have been suggested to accomplish this task, e.g., by making the B_2O_3 layer thicker or using the multizone heating (2). Recently, Kohiro et al. (3) have pulled low dislocation density InP crystals by employing a phosphorous-vapor-controlled (PC-LEC) method. In the PC-LEC method, a heat shield is used to decrease the axial temperature gradient, and an excess phosphorous vapor pressure (0.1-4 atm) is used to prevent the phosphorous dissociation from the crystal surface. The high pressure environement (about 40 atm) induces a highly turbulent gas flow in the furnace and thereby greatly influences the crystal cooling or heating. Bliss et al. (4) have also grown InP crystals with low dislocation denstiy using the liquid-encapsulated Kyropoulos method. Both Kohiro et al. (3) and Bliss et al. (4) have found that a heat shield is very useful in suppressing the gas convection and decreasing the dislocation generation in the crystal.

The generation and development of the thermal stress is particularly complicated in a HPLEC system where strong gas convection exists due to high pressure gas environment and the gas and melt flows are coupled through a low thermal diffusivity encapsulant layer. Zhang and Prasad has developed an advanced numerical model (MASTRAPP[1]) to simulate the HPLEC growth of InP crystals (5, 6). The MASTRAPP-based model accounts for the complex thermal interaction between the gas and melt flow. It also includes a sophisticated radiation formulation that is critical to simulate accurately the heat transfer conditions of the growing crystal (7). The HPLEC model has been further extended by Zou et al. (8) to incorporate segregation and thermal elastic stress calculations. They have studied the

[1]Multizone Adaptive Scheme for Transport and Phase-Change Processes

development of thermal stress in a HPLEC system, and have predicted two maximum stress spots, one at the periphery of the crystal when it just emerges out from the encapsulant, and the other at the melt/crystal interface. The calculated maximum Von Misses stress reaches about 29 MPa on the edge of the crystal and about 9.5 MPa at the melt/crystal interface. It is also found that as the crystal grows, the peak stresses at both locations are reduced with the values being largest when the crystal height is low, or at the beginning of the growth.

In this work, the MASTRAPP model has been used to investigate the effect of growth conditions on the development of thermal stress in a HPLEC grown InP crystal. In particular, it examines the variation of the resulting thermal stress under the conditions of both high and low axial temperature gradients. The effect of melt flow on stress development has also been examined.

II. PROBLEM DEFINITION

The MASTRAPP model was presented in brief in the last conference (9) and a detailed description of the model can be found elsewhere (5, 6, 7, 8). The present calculations have been carried out based on the HPLEC furnace operating at the USAF Rome Laboratory. The calculation domain is limited to the region inside the heat shield. The crucible wall temperature is assumed to be uniform and kept constant during the growth. Two different temperature conditions (Fig. 1) along the heat shield wall have been used to investigate the effect of the temperature boundary condition on thermal stress development in the crystal. In practice, the heat shield wall temperature can be controlled to a certain extent by varying the geometry or changing the fluid flow outside the heat shield. Case 1 represents a high axial temperature gradient along the heat shield while the Case 2 is for a lower temperature gradient. In Case 1, we assume that the axial temperature drops significantly in a short distance just above the crucible and then slowly decreases along the heat shield. In Case 2, the axial temperature decreases uniformly with a much lower gradient. In addition, the calculations are carried out without natural convection in the melt to study the effect of buoyancy-induced melt flows on stress development.
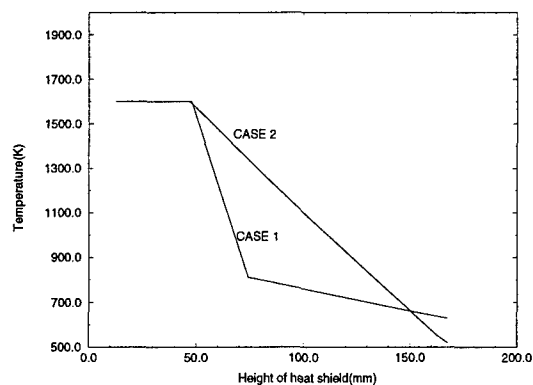
Figure 1: Temperature boundary conditions along the side wall of crucible and heat shield.
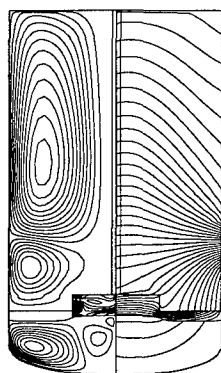
Figure 2: Temperature, stream function and thermal stress distributions for Case 1 with large temperature gradient ($Gr_g = 10^7$, $Gr_m = 10^6$, $Re_s = 10^3$, $Re_c = -5 \times 10^2$, Crystal height = 9 mm).
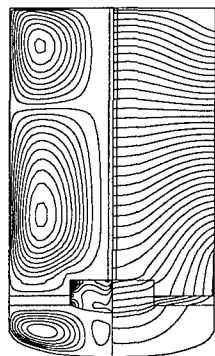
Figure 3: Temperature, stream function and thermal stress distributions for Case 2 with low temperature gradient ($Gr_g = 10^7$, $Gr_m = 10^6$, $Re_s = 10^3$, $Re_c = -5 \times 10^2$, Crystal height = 9 mm).
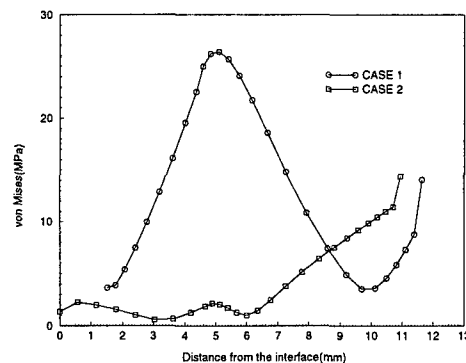
Figure 4: Comparison of the von Mises stress along the crystal surface for two cases.

III. RESULTS AND DISCUSSIONS

A. Effect of Axial Temperature Gradient

Numerical results for the above two cases are shown in Figs. 2 and 3. The results include the flow field (shown by streamlines on the left) in both the gas and the melt, the temperature fields (shown by isotherms on the right), and the von Misses stress (iso-stress lines on left side of the crystal). A comparison between Figs. 2 and 3 shows that the change in temperature condition along the heat shield has a dramatic effect on flow and temperature fields in the gas, as well as on the shape of the interface. The variation of the gas flow, from a small cell in the region between the crystal and the heat shield to a big cell as the temperature gradient along the heat shield is lowered down, leads to a very different heat transfer conditions for the crystal. This results in a much lower axial temperature gradient in the crystal for Case 2. This variation of the temperature field in the crystal leads to a significant decrease in the thermal stress at the edge of the crystal except near the top.

Figure 4 shows the predicted von Misses stresses at the edge of the crystal. In Case 1 with a large temperature gradient along the heat shield, a maximum stress spot is developed at the distance of about 5 mm from the interface, where the crystal emerges out from the encapsulant layer. This maximum value reaches about 26.4 MPa. By reducing the temperature gradient condition on the heat shield (Case 2), a much lower thermal stress is predicted below the encapsulant layer. Above the encapsulant layer, the thermal stress gradually increases to a larger value at the top of the crystal. For Case 2, a local maximum is still predicted at a location 5 mm from the interface where the crystal emerges out from the encapsulant, but the value is one order of magnitude smaller than that in Case 1 (2.1 vs 26.4 MPa). A local maximum stress with about 2.3 MPa also exists near the melt/ crystal interface for Case 2.

A careful examination of the temperature fields indicates that this reduction in thermal stress for Case 2 has resulted from the variation in heat transfer conditions. In Case 1, the rapid drop of temperature along the heat shield above

the crucible leads to a large temperature gradient in the encapsulant layer in both axial and radial directions. This large radial temperature gradient in the encapsulant leads to crystal cooling and therefore a large local radial gradient near the crystal surface in the region embedded in the encapsulant layer, where crystal loses heat to the encapsulant almost immediately above the melt/crystal interface. When the crystal emerges from the encapsulant layer, a quite different cooling condition is imposed on the crystal surface, the crystal is cooled by the recirculating gas. A local axial temperature is then developed near the surface in this area because of the sudden change of the crystal cooling conditions. A radial temperature gradient is also produced in the same area because of a strong cooling effect of the cold gas. This results in a large thermal stress in this region. A large thermal stress also develops near the top of the crystal due to a non uniform heat transfer condition along the top surface - a good cooling condition in the center where the seed is held by a cooled shaft, a reduced rate of cooling along the top surface away from the center, and heating at the cornor of the crystal due to the warm gas moving up.

In Case 2, on the other hand, a high temperature is maintained on the heat shield above the crucible, leading to higher temperatures for both the encapsulant and the gas. Much smaller axial and raidal temperature gradients than that in Case 1 are therefore developed in the encapsulant layer. In particular, because both the encapsulant and the gas above the encapsulant layer are at high temperatures, heat is not lost from the crystal to the encapsulant and gas in the nearby region, instead, heat is transferred through the crystal. When the crystal emerges from the encapsulant, although a change in heat transfer condition is introduced due to the variation of the heating media (from encapsulant to gas) which produces a local maximumm, no large temperature gradient is introduced in the crystal. Because of the dominant axial heat trasnfer along the crystal, a small thermal stress is developed in the region below the encapsulant layer as shown in Fig. 4 for Case 2. Away from the encapsulant, the crystal has a similar heat transfer condition as that in Case 1, so does the variation of the thermal stress, i.e., an increasing thermal stress to the top of the crystal.

The temperature conditions along the heat shield also affect the shape of the melt/crystal interface. As shown in Figs. 2 and 3, a concave interface towards the melt in Case 1 with a high temperature gradient is changed to a convex shape in Case 2 with a lower temperature gradient. This change in the interface profile leads to a dramatic reduction in maximum thermal stress developed at the melt/crystal interface (Fig. 5). As can be seen, a maximum stress (about 7.7 MPa) is developed at the center of the crystal for Case 1, which is reduced to about 1.6 Mpa for Case 2. This decrease in stress may be explained by the variation in heat transfer conditions along the interface and the assoociated low temperature gradients in the crystal. The isotherms show a large positive axial temperature gradient and a *negative*
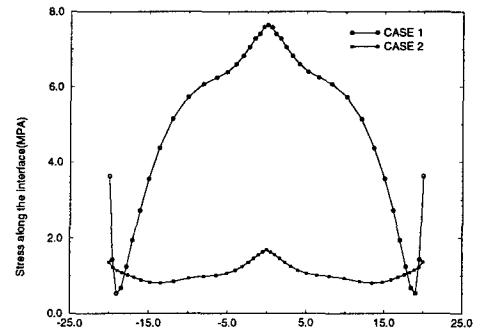
Figure 5: Comparison of the von Mises stress along the melt/crystal interface for two cases.
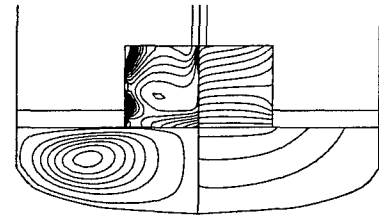
Figure 6: Flow, temperature and stress field calculated for the case without natural convection in the melt, i.e. $Gr_m = 0$ at crystal height $H = 17$ mm. ($Re_s = 10^3$, $Re_c = 0$, $Gr_g = 10^7$, $Sch = 16.2$, and $V_p = 10$ mm/hr)

radial temperature gradient near the interface for Case 1. However, a smaller axial tempertaure gradient and a *positive* radial temperature gradient is developed in the same area for Case 2. In the former case, the heat is lost from the crystal to the encapsulant, and in the latter case, the heat is transferred into the crystal from the encapsulant. This variation of the heat transfer condition of the growing crystal may result in the different thermal stresses shown in Fig. 5.
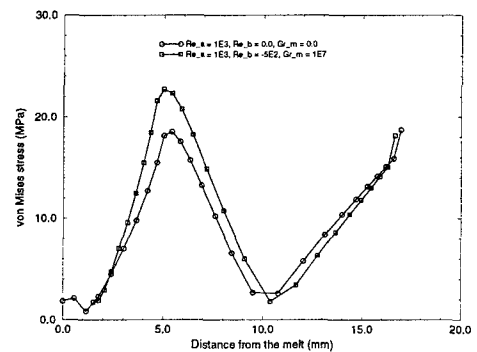
Figure 7: Comparison of the calculated Von Misess Stress along the edge of the crystal, with and without natrual convection in the melt.

B. Effect of Melt Flow

Most of the previous models that simulate the thermal stress development in LEC processes have generally ignored

278
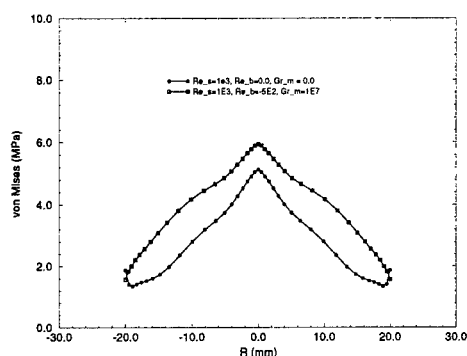
Figure 8: Comparison of the calculated Von Misess Stress along the melt/crystal interface, with and without natrual convection in the melt.

the effect of the melt flow. Recent study on Czochralski Si growth by MASTRAPP indicates that the melt flow may have a strong impact on both the calculated value of the thermal stress and the distribution of the stress along the melt/crystal interface (8). In the case of HPLEC growth, the effect of the melt flow is expected to be weaker because the critical thermal stress developed in the crystal is located above the melt/crystal interface, as shown in the previous paragraphs. Nevertheless, the effect of the melt flow on thermal stress in HPLEC grown crystals is important. This is demonstrated here by eliminating the buoyancy-driven flow in the melt. However, a low crystal rotation is still applied to maintain the thermal symmetry of the growth system. A large temperature gradient as in Case 1 above is used since this condition is prone to high thermal stresses.

Figure 6 shows the melt flow, temperature, and stress distributions when the flow in the melt is induced by pure crystal rotation, i.e., the melt Grashof number is set to zero while the gas Grashof number and other conditions are the same as in the previous case. The crystal height is about 15.0 *mm*. As in the case of Fig.2 with strong natrual convection, a large thermal stress is developed in the crystal, especially along the edge of the crystal. This is clearly shown in Fig. 7 which presents the stress distributions along the crystal surface for both cases, with $(Gr_m = 10^7)$ and without $(Gr_m = 0)$ natrual convection. A maximum thermal stress is developed at the same location, i.e., 5 mm from the interface where the crystal emerges from the encapsulant. Eliminating the melt flow, however, reduces the maximum value from about 23 MPa to about 18.5 MPa, a reduction of about 24 percent. This moderate effect of the melt flow on stress may be understood considering the strong effect of the stress by the gas flow and heat transfer between the crystal and the gas and the encapsulant.

The effect of the melt flow on stress along the melt/crystal interface is shown in Fig. 8. Under the present temperature condition, the melt flow shows only moderate effect on the stress at the interface. The maximum stress in both cases is at the center of the crystal. Eliminating the natrual convec-

tion will reduce the maximum value by about 15 percent, however.

III. CONCLUSIONS

A numerical investigation has been conducted to study the effect of the temperature boundary conditions, in particular the axial temperature profile along the heat shield wall, on thermal stress development in the HPLEC grown InP crystals. The results indicate that the thermal boundary condition on the heat shield has a significant effect on the development of the thermal stresses in HPLEC grown InP crystals. Under the conditions used here, one order of magnitude reduction in maximum stress at both the crystal surface and the melt/crystal interface is predicted by decreasing the axial temperature gradient along the heat shield. This dramatic effect of the temperature boundary condition on stress is caused by the variation of the heat transfer conditions of the crystal. The effect of melt flow on stress development is also investigated, and only moderate reduction in thermal stress is predicted by eliminating the natrual convection in the melt.

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INFLUENCE OF DOPANT SPECIES ON ELECTRON MOBILITY IN InP

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Introduction

We present a theoretical reassessment of electron mobility in doped InP with respect to different doping species. Using Thomas-Fermi theory in the energy functional formulation we describe the charge density of the individual impurity ion. Analytical expressions for the scattering rate are calculated based on a variational expression of Schwinger. Employing these results in a Monte Carlo calculation we find no significant dependence of mobility on doping species up to 10^{18} cm^{-3}. For higher concentrations an increasing difference is observed which reaches 25% at 10^{19} cm^{-3} for Si and Te doping.

I. Background

The dependence of the electron mobility μ on impurity concentration has been investigated for a long time by many theoretical approaches and experimental work mostly in n-InP. Many corrections to the simple Brooks-Herring (BH) model have been introduced improving the overall agreement with experiments [8]. All attempts in the past failed to explain the influence of the different dopant species characterized by the atomic number Z and electron number N. One usually assumes a delta-like impurity charge concentrated in the origin of the dopant ion neglecting the spatial extension of the electron charge distribution of the dopant. This is equivalent to neglecting the dependence of the atomic form factor $F(q)$ on the momentum transfer $q = |\mathbf{k}' - \mathbf{k}|$. We show that consideration of a spherically symmetric charge density of the electrons explains the different mobilities for majority and minority electrons for various dopants at high concentration.

II. Thomas-Fermi atomic model

Assuming a hydrogen-like electron charge distribution consisting of N valence electrons

$$\rho_e(r) = \frac{N\,\alpha^3}{8\,\pi}\,e^{-\alpha\,r} \qquad (1)$$

$$N = \int \rho_e(r)\,dV$$

and a point-like nucleus with charge Z, the total charge distribution of an impurity ion (in units of the elementary charge e_0) is

$$\rho_{ion}(r) = Z\,\delta(r) - \rho_e(r)\,. \qquad (2)$$

The atomic form factor $F(q)$ which is the fourier transform of ρ_e [11],

$$F(q) = \int \rho_e(r)\,e^{-i\,\mathbf{q}\cdot\mathbf{r}}\,dV = \frac{N\,\alpha^4}{(q^2 + \alpha^2)^2}\,, \qquad (3)$$

directly enters the effective scattering potential in momentum space $U(q)$

$$U(q) = V_0\,\frac{Z - F(q)}{q^2 + \beta^2} \qquad (4)$$

$$V_0 = \frac{2\,e_0^2\,m^*}{\hbar^2\,\varepsilon}\,.$$

β is the inverse Thomas-Fermi screening length. The reason for different scattering rates for different dopants lies in the different radial extension of their charge density expressed by the variational parameter α. To obtain numerical values for α as function of the doping species determined by Z and N we minimize the semiclassical Thomas-Fermi energy functional [2, 4, 15]. It should be noted that the form factor can also explain the difference between majority and minority electron mobility since, besides the completely different functional form, $Z - F(q)$ is larger than unity in the first and smaller in the second case. Only in the limit of small-angle scattering ($q \to 0$) the form factor equals the number of electrons, $F(0) = N$, and the BH Model is retained.

III. Scattering rates

In addition to the first scattering amplitude of the Born approximation

$$f_1(q) = U(q), \qquad (5)$$

an analytical expression for the second scattering amplitude $f_2(q)$ of the Born series can be obtained if we use the approximation $F(q) \approx F(0) = N$,

$$
\begin{aligned}
f_2(q) &= \frac{U_0{}^2}{q\,A(q)}\left(\mathrm{atan}\left(\frac{\beta\,q}{2\,A(q)}\right) + \frac{i}{2}\log\frac{A(q)+k\,q}{A(q)-k\,q}\right) \\
A(q) &= \sqrt{\beta^4 + 4\,\beta^2\,k^2 + k^2\,q^2} \\
U_0 &= \frac{2\,e_0^2\,m^*\,(Z-N)}{\hbar^2\,\varepsilon}.
\end{aligned}
\qquad (6)
$$

The squared total scattering amplitude gives the differential scattering cross section

$$\frac{d\sigma}{d\Omega}(q) = |f(q)|^2, \qquad (7)$$

the total scattering cross section for electrons in state k is

$$\sigma(k) = \frac{2\,\pi}{k^2}\int_0^{2k} |f(q)|^2\, q\, dq. \qquad (8)$$

In the usual first Born approximation (B1), which is valid for low doping concentrations, the total amplitude simply is the first term $f_{B1}(q) = f_1(q)$. In the second Born approximation (B2) the series is truncated at the second term and $f_{B2}(q) = f_1(q) + f_2(q)$. However, the series does not converge for small energies. Therefore we calculate the total scattering amplitude by employing the variational method of Schwinger [6, 12]. The scattering amplitude denoted by $f_S(q)$ can be expressed as

$$f_S(q) = \frac{f_1(q)}{1 - \dfrac{f_2(q)}{f_1(q)}}. \qquad (9)$$

It can be shown that using (9) the divergence of the second Born approximation for the cross section σ_{B2} that occurs at small energies at low concentration is avoided while with increasing concentration σ_S exceeds σ_{B2}, which is in agreement with numerical phase-shift results [7].

As the Friedel sum rule [13] has to be obeyed by the effective scattering potential, a correction for the screening parameter β has to be introduced which now also depends on Z and N.

The behavior of the Schwinger formula is shown for example in the calculated momentum scattering rate for low (Fig. 1) and high doping concentrations (Fig. 2), respectively. While the scattering rate for weakly n-doped material using the Schwinger model is about three orders of magnitude below B2 and even smaller

than the BH value, it lies above BH for highly n-doped but below for heavily p-doped material. Throughout the figures "Schwinger" denotes the use of Schwinger formula with $F(q) = N$ while the chemical symbols for the dopant elements in Figs. 4-6 imply the usage of the Schwinger model including $F(q)$.
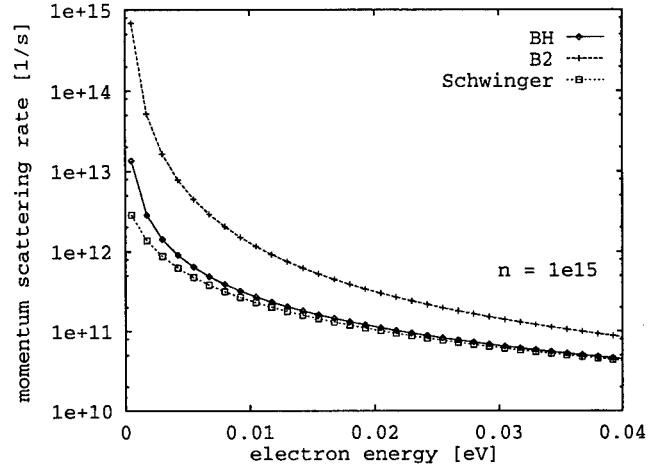
Figure 1. Momentum scattering rate for a carrier concentration of 10^{15} cm^{-3} in InP with $F = F(0)$.
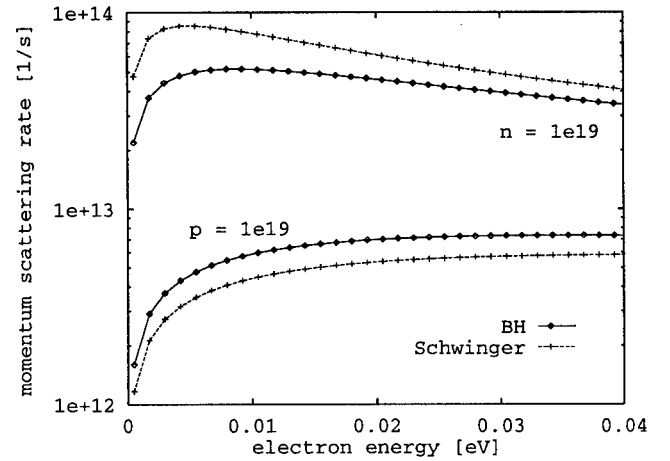
Figure 2. Momentum scattering rate for a carrier concentration of 10^{19} cm^{-3} in InP with $F = F(0)$.

IV. Monte Carlo Results

We employ the derived formulas in a single-particle Monte Carlo procedure to calculate the electron drift mobility at 300K using an analytic three-valley band dispersion and include phonon and plasmon scattering. At high concentrations many-body effects cause a distortion of the conduction band. The resulting concentration dependent change of the density of states

281

is incorporated via an increase of the effective electron mass. This mass enhancement is an increase of the band edge curvature mass and is not to be confused with the usual mass increase due to nonparabolicity. In analogy to [14] we model the effective mass by a polynomial in n,

$$\frac{m^*}{m_0}(n) = 0.075 + A\frac{n}{n_{ref}} + B\left(\frac{n}{n_{ref}}\right)^2 \quad (10)$$

$$A = 3.49 \times 10^{-3}$$

$$B = -2.37 \times 10^{-5}$$

$$n_{ref} = 10^{18}\,\mathrm{cm}^{-3}.$$

The coefficients have been obtained by a fit to experimental data summarized in [9]. Equation (10) is valid for $n < 3 \times 10^{19}$ cm^{-3}. The Pauli exclusion principle is accounted for by a rejection technique [3].

Fig. 3 compares the calculated majority mobility using the Brooks-Herring (BH) and "Schwinger" model with published experimental Hall data [1, 5, 9]. The Schwinger model reduces the overestimation of the mobility of BH at degenerate conditions significantly.
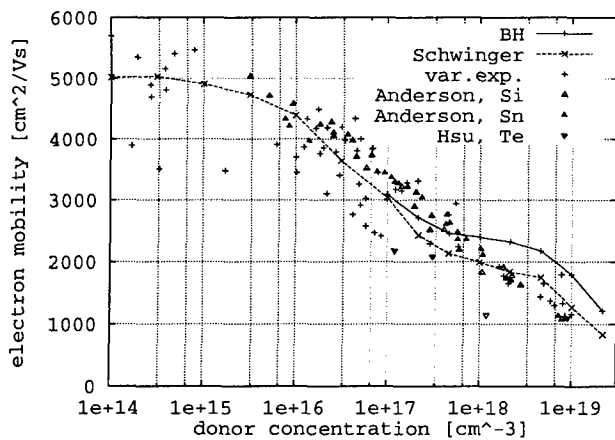
Figure 3. Majority electron mobility in InP with $F = F(0)$.

In Fig. 4 the mobility for different donors in InP is shown. We find no significant influence on Z up to $n \approx 10^{18}$ which is in agreement with experiments. With increasing concentration the different behavior becomes significant, heavier ions lead to lower values of μ. At 10^{19} cm^{-3} the mobility differs by 25% for ^{14}Si and ^{52}Te doping, which are the lightest respectively heaviest donors used. Unfortunately, the uncertainty and scattering of the available experimental data is of the same order of magnitude as the difference of the mobilities for various dopants. Hence, we are unable to assess the simulation results quantitatively at that time. In case of n-Si (Fig. 5), however, a systematic decrease of μ with increasing Z is observed experimentally, too [10].
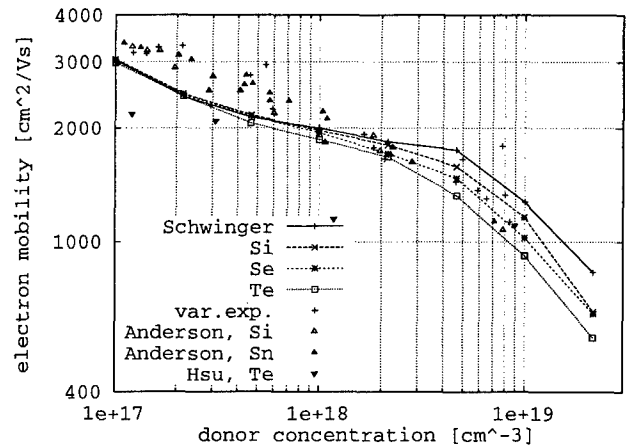
Figure 4. Majority electron mobility in InP with $F = F(q)$.
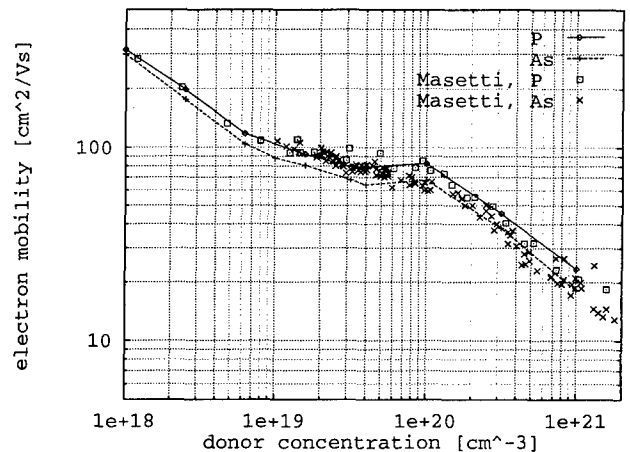
Figure 5. Majority electron mobility in Si with $F = F(q)$.

Finally, Fig. 6 shows the well-known dip in μ in p-type material due to the plasmon interaction and a weaker dependence on Z compared to n-type material. Only for $p > 2 \times 10^{19}$ cm^{-3} a small difference is observed, μ again decreases with atomic number from ^{4}Be, ^{30}Zn to ^{48}Cd.

V. Conclusions

The proposed theoretical approach to our knowledge is the first physically based model to date which explains the dependence of the majority and minority electron mobility on various dopant species through the atomic number. Corrections to the first Born approximation are important for doping concentrations beyond 10^{17} cm^{-3}. The dependence on the donor species be-
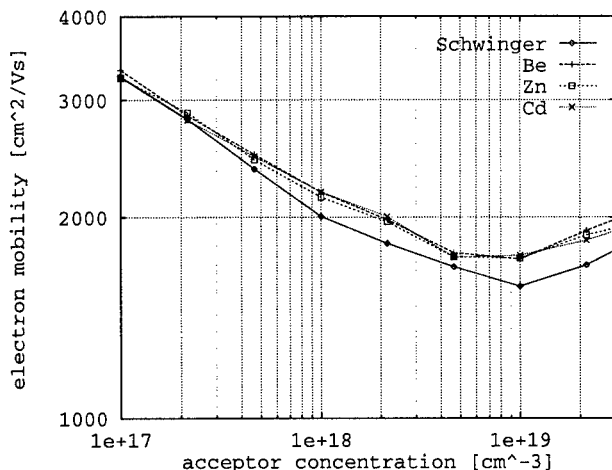
Figure 6. Minority electron mobility in InP with $F = F(q)$.

comes significant for concentrations beyond 10^{18} cm^{-3}. Neither compensation nor autocompensation is necessary to obtain a close agreement with experiment in highly n-degenerate material. In case of minority electron transport no species dependence is observed in the practical doping range.

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Acknowledgments

283

Inverted, Substrate-Removed Vertical Schottky Diode Optical Detectors

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Introduction

The InGaAs metal-semiconductor-metal (MSM) photodetector has great potential as a high-performance component for future lightwave communication systems and opto-electronic integrated circuits (OEICs). Low capacitance, dictated by finger spacing, and high carrier drift velocity should result in GHz operating bandwidths.[1] Efficient optical absorption to 1.7 μm results in high responsivity at the wavelengths preferred for optical fiber communications, 1.3 and 1.55 μm. Although significant efforts have been devoted to the realization of InGaAs MSM photodetectors, few devices have found their way into commercial or military products. Among the technical problems still hindering the practical incorporation of InGaAs MSMs into optical systems and networks are their high dark current and the slow response of photo-generated holes. High dark current results from low Schottky barrier heights and poor surface passivation. The problem is compounded for devices with submicron finger spacing since the surface electric fields are very high. Analysis of carrier dynamics shows holes generated deep in the depletion region can significantly degrade the high-frequency response. For these reasons we have chosen to investigate new designs for vertical Schottky diode detectors.

I. Background

An alternative to the lateral MSM photodetector is the vertical Schottky diode (VSD). The classical fabrication method for front-illuminated Schottky diode optical detectors requires the Schottky contact to be made with either a transparent conductor, a thin semi-transparent metal, or a metal with a grid-style layout. Engineering the Schottky junction for transparency usually involves compromises in barrier height. Schottky diode detectors can also be illuminated through the substrate. The fabrication of such back-illuminated detectors is hampered by the fact that the InP substrate is opaque to visible light, making alignment of the source and detector difficult. Our new design improves the performance and manufacturability of back-illuminated InGaAs Schottky diode optical detectors. A substrate removal process is used to expose a buried InGaAs ohmic contact layer. Ohmic contacts are made with the same techniques as front-illuminated Schottky contacts: either a transparent conductor, a thin semi-transparent metal, or a thicker metal with a grid-style layout. The Schottky contact in our design is made with a standard TiAu process, which results in better detector performance. Alignment of the optical input to the detector is made easily after removal of the opaque substrate. In addition, carrier transport is vertical, circumventing the need for the submicron lithography required in high-speed lateral structures. Device performance can then be optimized by precise epitaxial growth techniques.

II. Experimental Results and Discussion

Photomicrographs of completed vertical Schottky diode detectors are shown in Fig. 1. After TiAu Schottky metalization, the wafer is secured to a surrogate substrate and the InP bulk is selectively removed, leaving only the epitaxial layers (InAlAs/InGaAs/n^+-InGaAs). For the detectors of Fig. 1, indium tin oxide (ITO) is deposited over the newly exposed n^+-InGaAs by RF sputtering. Mesas are formed by etching the ITO with HCl and the epitaxial layers with a

10:1:1 solution of H_2O:H_3PO_4:H_2O_2. CrAu pads are placed in a ground-signal-ground configuration with a liftoff process to facilitate microwave probing.

Performance was studied as a function of physical design and processing. Two detector designs were investigated; in the first design the Schottky contact extends past three mesa edges (extended gate), in the second design the ohmic contact pad extends over three edges (extended ohmic). An air bridge is not required for either design. To reduce the series resistance of the back contact, CrAu fingers are used for the extended gate design and a grid pattern is used with the extended ohmic design. Detectors were processed with and without the ITO transparent conducting layer. Mesa areas were varied to determine the dominant reverse leakage current path (edge or surface) and to distinguish whether performance is limited by RC time constant or transit-time effects. The InGaAs absorber thickness and InAlAs barrier layer thickness and composition were varied to determine optimum electrical and optical design. Table 1 lists the lattice-matched epitaxial layers used in this study. Different InAlAs surface treatments, prior to Schottky contact evaporation were also studied.

CrAu Ohmic metal

TiAu Schottky contact
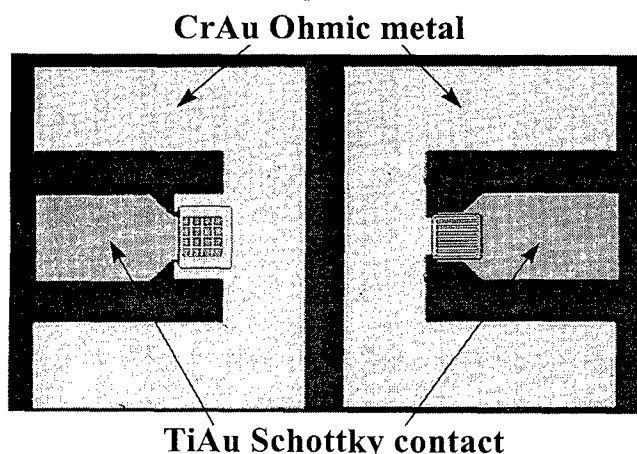
Figure 1. Photomicrographs of 50x50 μm² VSD detectors. Extended ohmic is shown on the left and the extended gate on the right.

Wafer	SBE (nm)	Junction	Absorber (μm) InGaAs	Ohmic Contact (nm) $n+$ -InGaAs
A	25	abrupt	1.0	10
B	25	graded	1.0	10
C	50	abrupt	1.0	10
D	50	graded	1.0	10
E	50	abrupt	0.5	none

A. I-V and C-V Characteristics

The InAlAs Schottky barrier enhancement (SBE) layer affects both dark-current level and high-frequency response.[2] We fabricated diodes with abrupt InAlAs/ InGaAs and graded InAlAs/InAlGaAs/InGaAs junctions. For a given SBE layer thickness, the abrupt junctions consistently yield lower dark current. I-V characteristics of 20×20 μm^2 extended gate detectors fabricated from wafer C are shown in Fig. 2

Etching the exposed InAlAs surface with a 6:1 succinic acid (1.7 M, adjusted to a pH of 5.5 with NH$_4$OH):H$_2$O$_2$ solution[3] prior to e-beam evaporation of TiAu Schottky contacts results in lower leakage current than treating the surface with buffered oxide etch (BOE). The reduced leakage is unexpected since the 8-minute succinic acid etch removes approximately 20 nm of InAlAs from the 50 nm abrupt SBE layer. A similar result was observed after removing 10 nm of InAlAs from the 25 nm abrupt SBE layer. The succinic acid solution may form a beneficial native oxide layer, but this is

unlikely since treating the succinic acid-etched surface with BOE did not substantially change the leakage characteristics, as shown in Fig. 2. Plots of 1/C^2 vs. bias indicate the succinic acid-etched sample has a slightly larger barrier height.

The Schottky diodes are of high quality for both mesa designs; the best diodes display dark currents below 10 pA/μm^2 at 5 V reverse bias and breakdown voltages above 12 V. The extended ohmic design leaves fewer mesa edges exposed but no systematic differences in leakage currents or breakdown voltages are observed. At low reverse bias (-5 V) a linear increase in dark current with mesa area is observed in both detector designs, suggesting injection over the barrier and bulk recombination are the dominant paths for leakage, even though mesa edges are not passivated. Equivalent levels of leakage are observed for samples with and without ITO layers, implying the sputtering process used does not cause substantial damage to the Schottky contact.

The knee in the I-V curve at approximately V = -0.5 V is interpreted as the bias required to fully deplete the InGaAs absorber. Using $n = 2\ \varepsilon_s\ \varepsilon_o(|V| + V_{bi})/(q\ d^2_{epi})$, $\varepsilon_s = 11.3$, and $V_{bi} = 0.5$ V we calculate a background carrier concentration of $n = 1.2 \times 10^{15}$ cm^{-3}. C-V data of Fig. 3 approaches a minimum around V = -1.0 V, suggesting the depletion layer extends into the n^+-InGaAs contact layer. Plotting C_{min} vs. area and extrapolating to zero area gives a stray capacitance under 40 fF. Stray capacitance is mainly due to probes and cables. The corrected values of minimum capacitance (C_{min}) for the
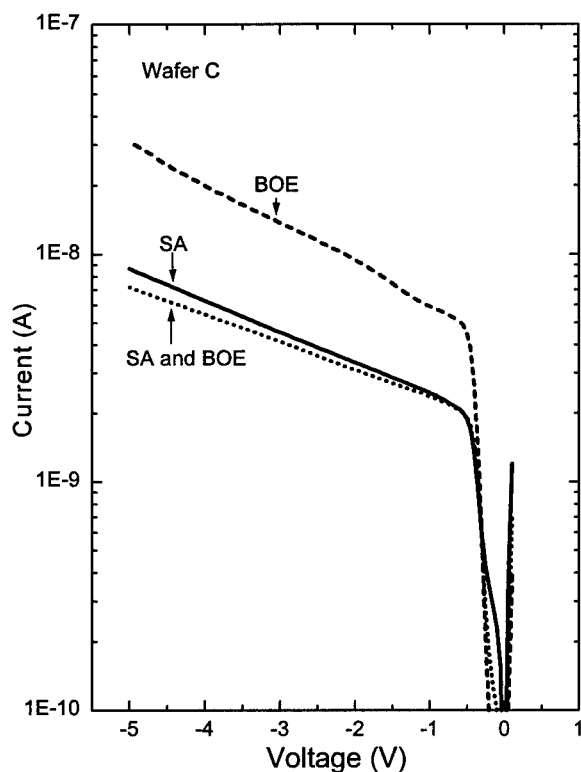
Figure 2. I-V characteristics for 20×20 μm^2 Schottky diodes fabricated from wafer C. Lowest dark currents are observed for abrupt InAlAs/InGaAs heterojunctions after succinic acid (SA) etching.

Figure 3. C-V characteristics for Schottky diodes fabricated from wafer C. 20×20 μm^2 detectors have a capacitance below 50 fF after correcting for probes and cables.

20×20, 30×30, 40×40, and 50×50 μm² detectors are 47, 104, 181, and 248 fF, respectively. Maximum performance is observed for a reverse bias beyond -3 V, corresponding to E = 30 KV/cm for an InGaAs absorber of 1 μm. Bias levels above $|V|$ = 3 V insure full depletion and photo-generated carriers will travel at their saturation velocities.
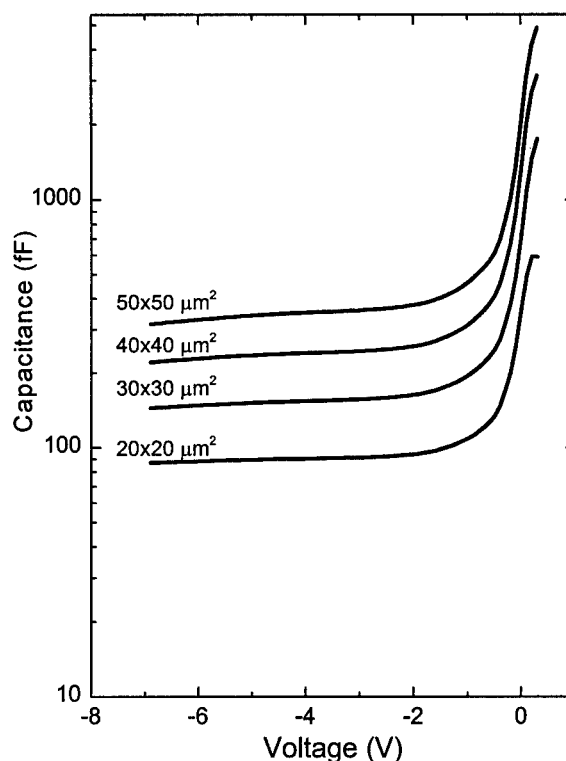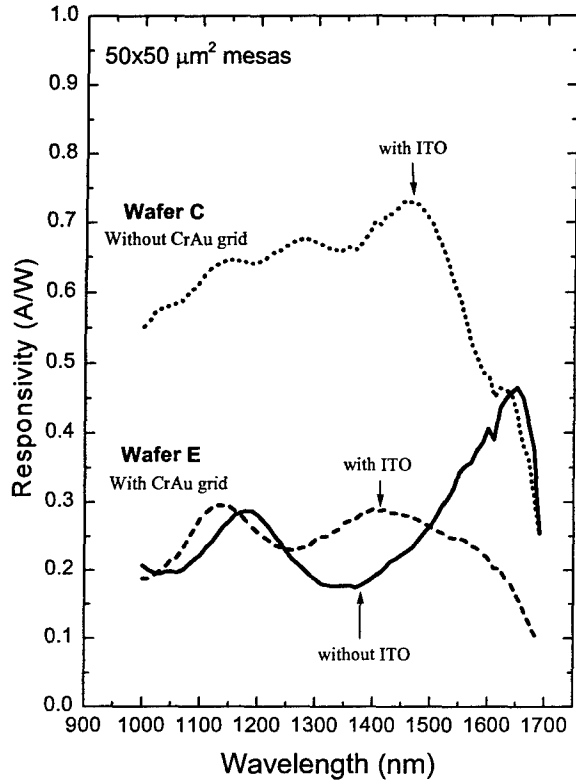

Figure 4. Responsivity results from wafer E and wafer C show the beneficial effects of ITO. The CrAu ohmic grid covers approximately 35% of the mesa area.

B. Responsivity

Responsivity is measured between 1.0 and 1.7 μm using a 0.15 meter monochromator and lock-in amplifier. Light from the monochromator is coupled into a fiber (50 μm core) positioned over the detector. Calibration is performed by measuring the output power of the fiber with a large-area Newport Ge detector. Figure 4 shows the responsivity of a 50×50 μm² detector fabricated from wafer C with a 150 nm ITO coating (upper trace). Responsivities over 0.7 A/W are obtained for 1μm thick InGaAs absorbers. The ITO layer acts as an anti-reflection (AR) coating, maximizing the response near 1.5 μm. Responsivity is also shown in Fig. 4 for the 50×50 μm² extended ohmic detectors fabricated from wafer E (lower traces).

The data from wafer E in Fig. 4 was taken after depositing the grid metal over samples with and without an ITO layer. The grid pattern covers approximately 35% of the surface area. Accounting for the fraction of power blocked by the grid metal and the fraction of power reflected at the

semiconductor surface, we calculate an internal quantum efficiency of 60%. Absorption in the TiAu and power lost to incident light falling outside the device area partially account for the low experimentally observed internal quantum efficiency. Conversely, the absorbing power of the 0.5 μm InGaAs layer is enhanced for specific wavelengths by using the Schottky contact as a reflector. We account for the beneficial effects of the optical cavity by modeling the layered structure and determining the reflection coefficient as a function of wavelength before calculating the internal quantum efficiency. Detector responsivity is optimized for specific wavelengths by choosing an InGaAs absorber thickness and using an ITO layer as the AR coating.

C. Pulse Response

A 35 ps FWHM Tektronix OIG 502 (λ = 1.3 μm) optical impulse generator was used as the input. The dc voltage was supplied through a 40 GHz bias tee and detectors were contacted with a 50 GHz microwave probe in a ground-signal-ground configuration. The optically generated signal is fed to the input of a high speed digitizing oscilloscope with a 50 ohm input impedance. Figure 5 shows pulse responses for VSD and MSM detectors processed from wafer E for different active detector areas and ohmic contact schemes.

There is very little observed change in pulse width or shape for VSD detectors with ITO having areas less than 40×40 μm². Rise and fall times of 25 ps and a FWHM of 35 ps are mainly limited by the optical source. Transient response of the VSD can be limited by the RC time constant or carrier transit-time effects. For the smallest area detector, C = 100 fF and R = 50 ohms gives τ_{RC} = 5 ps. Using a 0.5 μm absorber thickness and a hole saturation velocity of v_s = 5×10⁶ cm/s gives a transit-time of τ_t = 10 ps, which is of the same order of magnitude as the predicted RC time constant. Additional series and contact resistance likely raises τ_{RC} above τ_t for devices fabricated from wafer E. The pulse response of the 20×20 μm² vertical detector with only a CrAu grid is degraded from the 20x20 μm² detector with ITO since the series resistance is significantly higher.

Transit time-limited response is not likely observed for detectors fabricated with 0.5 μm InGaAs absorbers. Performance is more likely limited by the transit time for 1.0 μm absorber detectors since the transit-time is increased by a factor of 2, while capacitance per unit area is reduced by a factor of 2 compared to detectors fabricated with 0.5 μm absorbers.

The inverted, substrate-removed MSM detector of Fig. 5 is fabricated in the same manner as our VSD detectors, although it does not require a back ohmic contact. The MSM mesa area is 50×50 μm² and the finger width and spacing are 1 and 2 μm, respectively. The commonly observed tail in the pulse response of the MSM detector is evident. Failure of the pulse response to return to zero significantly reduces the useable bandwidth of MSM detectors. The vertical structures ensure uniform electric field and high carrier collection efficiency compared to lateral MSMs.
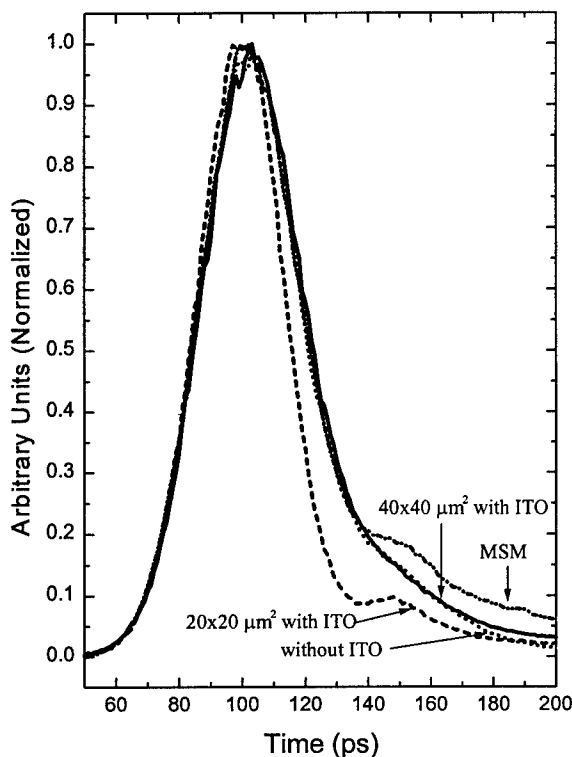
Figure 5. Pulse response from wafer E in both VSD and MSM configurations. Different active areas are shown along with the effects of an ITO AR coating. All VSD detectors have an CrAu ohmic grid metal.

Figure 6. Frequency response measurement indicate a greater bandwidth with both ITO and ohmic grids for small area detectors.

Small area detectors consistently show a small shoulder shifted from the center of the primary peak by approximately 40 ps. The n^+ layer was eliminated in wafer E to avoid the generation of holes in a semiconductor with low electric field, which would extend the transit time, but the shoulder is still present. Holes generated near the back surface would require the longest time to drift to the Schottky electrode. The shoulder did not depend on the InAlAs SBE layer thickness or composition, InGaAs absorber thickness, or the contact geometry. We eliminated the possibility of a round-trip reflection in the single mode 9 μm-core optical fiber used to illuminate the sample by using significantly different fiber lengths. We also eliminated possible problems in the electrical measurement system by varying cable lengths, bias tees, and probe tips. The shoulder may be an artifact of the optical source, electrical ringing due to inductance, or the result of surface defects.

D. Frequency Response

An HP 83420A lightwave test set with a 1.55 μm laser was used for frequency domain measurements. Calibration of the apparatus was performed with an internal system detector and an amplifier of known response. The only component not included in the calibration is the microwave probe tip. Responsivity as a function of modulation frequency is shown in Fig. 6 for VSD detectors fabricated from wafer E. The 20×20 μm² detector with a CrAu ohmic grid, curve (a),

demonstrates a responsivity of 0.35 A/W and a 3dB bandwidth of 10 GHz. Using an ITO back contact instead of CrAu, curve (b), increases responsivity to 0.5 A/W and the 3dB bandwidth to 13.8 GHz. Placing a CrAu grid pattern over the ITO layer reduces the responsivity by 30% to 0.35 A/W but increases the bandwidth to 18 GHz, curve (c).

Responsivities obtained with the monochromator (nW of optical power) correspond well with the values of obtained with the lightwave analyzer (mW of optical power), suggesting a linear dependence on optical power and the absence of the low frequency gain often observed in MSM detectors.

III. Summary

High performance vertical Schottky diode photodetectors were demonstrated. Low dark current densities (10 pA/μm²) and high responsivities (0.7A/W) are readily obtained. Using ITO to reduce the series resistance of the back contact allowed fast response and good sensitivity. The highest bandwidth obtained with frequency domain measurements is 18GHz.

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EXTENDED CAVITY LASERS FABRICATED USING PHOTO-ABSORPTION INDUCED DISORDERING

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Introduction

Photo-absorption induced disordering (PAID) has emerged as a laser induced quantum well intermixing technique of particular applicability to the GaInAsP/InP material system. Blue shifts in the bandgap of >100 meV in standard MQW laser structures are typically obtainable. The spatial selectivity of the technique is, however, limited by lateral heat flow. Here we show that extended cavity lasers can be fabricated by the PAID process, provided the graded interface region is pumped. The PAID process is modelled, and the ultimate spatial resolution is deduced.

I. Background

Photo-absorption induced disordering (PAID) has emerged as a laser induced quantum well intermixing (QWI) technique of particular applicability to the GaInAsP/InP material system. The technique takes advantage of the poor thermal stability of this material system, by using illumination from a Nd:YAG laser operating cw at 1.064 μm to heat the sample[1]. Intermixing takes place entirely in the solid state and requires a power density of only ~1 to 10 W mm^{-2}. The process involves band-to-band and free carrier absorption of the incident laser photons. Subsequent carrier cooling and non-radiative recombination results in the generation of heat causing the temperature of the material to rise to a level at which thermal intermixing will occur. Blue shifts in the bandgap of >100 meV in standard MQW laser structures are typically obtainable. The resulting processed material is of high optical and electrical quality, as evidenced by the production of band-gap shifted lasers[2], bandgap tuned modulators[3] and low-loss waveguides[4]. The spatial selectivity of the technique is, however, limited by lateral heat flow[4]. Here we show that extended cavity lasers can be fabricated by the PAID process, provided the graded interface region is pumped. The PAID process is modelled, and the ultimate spatial resolution is deduced.

II. Material Structure

The laser structure investigated was grown by metal organic vapour phase epitaxy (MOVPE) on an (100)-oriented n$^+$-type InP substrate and consisted of five 85 Å InGaAs wells with 120 Å InGaAsP (λ_g=1.26 μm, where λ_g is the wavelength corresponding to the bandgap) barriers. The active region was bounded by a stepped graded index (GRIN) waveguide core consisting of InGaAsP confining layers. The thicknesses and compositions of these layers (from the QWs outward) were 500 Å of λ_g=1.18 μm and 800 Å of λ_g=1.05 μm. The structure, which was lattice matched to InP throughout, was completed by an InP upper cladding layer and an InGaAs contact layer. The first 0.2 μm of the upper cladding layer was doped with Zn to a concentration of 5×10^{17} cm^{-3} and the remaining 1.2 μm to 2×10^{18} cm^{-3}. The lower cladding layer was Si doped to a concentration of 1×10^{18} cm^{-3}. The waveguide core was undoped, thus forming a pin structure with the intrinsic region restricted to the QWs and the GRIN layers.

III. PAID Intermixing

The experimental set-up used to intermix the material is shown in Fig. 1. During the disordering process, half of the Gaussian profiled laser beam was shielded using a metal mask suspended approximately 200 μm above the material surface. This mask effectively stops any heat being generated within certain regions of the material, thereby generating an interface between disordered and undisordered regions. The beam size was approximately 2 mm (FWHM) and the material was disordered by moving the laser along the mask edge in steps of approximately 1.5 mm.

The position of the metal mask does not determine the precise position of the interface because of the diffusion of heat away from the regions of high temperature i.e. the heat generated by the laser tends

to diffuse under the mask. In order to examine the spatial profile of the bandgap and determine where the active region and passive region of the ECL should be, photoluminescence measurements were carried out perpendicular to the mask edge in steps of 50 μm. Figure 2 shows the spatial PL plot of the sample, indicating shifts of up to 140 nm in the disordered section, with a transition region width of around 200 μm.

IV. Lasers with Unpumped Interface

Fig. 3 shows light-current (P-I) characteristics from ridge waveguide lasers with integrated extended cavities, in which current was injected only into the masked (non-disordered) region. At threshold, these devices show a near vertical jump (snap-on) in the P-I characteristics but then a more typical linear regime, with no kinks, takes over at higher currents. This sort of P-I relationship is typical of a Q-switched laser, which contains a saturable absorber in the cavity. This effect can also occur in broad area lasers with bad metal contacts, which cause inhomogeneous current injection, leading to gain switching[5]. By extrapolating the curves back to the x-axis, it is possible to define an effective threshold current for the
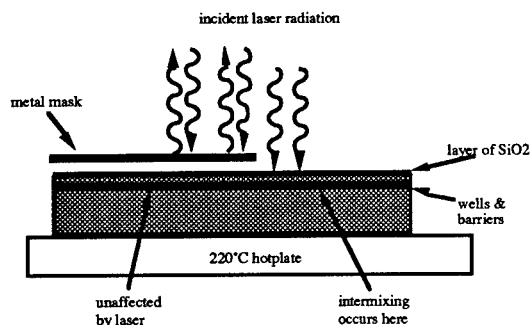
Fig. 1: Experimental set-up used to intermix the ECL samples
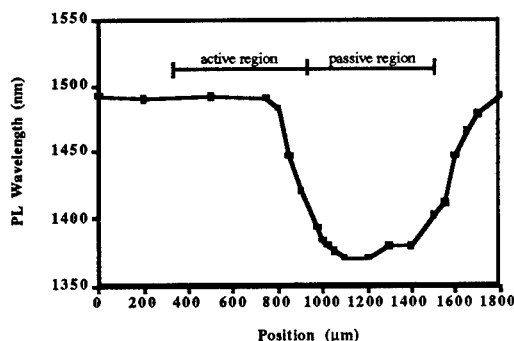
Fig. 2: Spatial PL plot of extended cavity laser sample
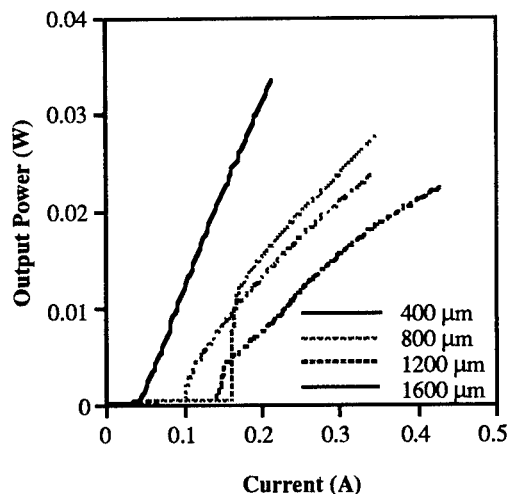
Fig. 3: Light-current characteristics of extended cavity ridge laser with unpumped interface region. The extended cavity lengths are as indicated.

devices, and hence infer the loss in the passive section. This procedure gives a value of 28.7 cm⁻¹.

V. Lasers with Pumped Interface Region

A second batch of devices was fabricated in which part of the graded interface region was pumped. The positions of the pumped and unpumped sections are indicated in Fig. 2. The interface between the active region and the passive region of the devices was chosen to be the mid-point between the zero intermixing and maximum intermixing regions. The sample was cleaved in such a way as to produce broad area OSLs next to the extended cavity devices, making direct device performance comparison possible.

The oxide stripe lasers were tested under pulsed operation (400 ns @ 1 kHz rep. rate). Fig. 4 shows the P-I curves of a bar of 600 μm lasers situated immediately beside the (active region of the) ECLs. The threshold current of these lasers was around 500 mA (1.1 kA cm⁻²).

Fig. 5 shows the P-I curves of the bar of EC lasers with 600 μm passive regions and 600 μm active regions. The best threshold current was around 1.2 A which is a factor of 2.4 greater than that of the 600 μm long oxide stripe lasers. The increase in threshold current is due both to the absorption in the passive waveguide region, and to the divergence of the light from the active region due to the lack of optical confinement in the passive slab waveguide region. It seems likely that the main loss is due to the lack of optical confinement in the transverse direction of the passive section, leading to poor coupling back into the active section.
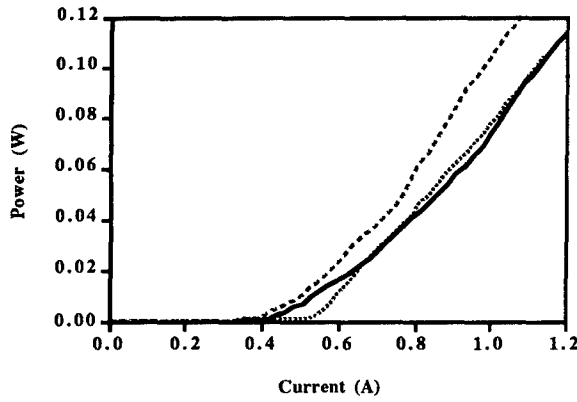
Fig. 4: Light-current characteristics of oxide stripe lasers without extended cavity.
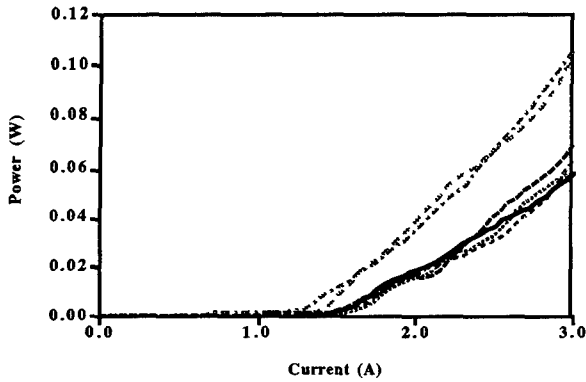
Fig. 5: Light-current characteristics of extended cavity oxide stripe lasers with pumped interface region.

It is not possible to determine the propagation losses from the change in threshold current as there is no transverse confinement in the passive section. The losses can, however, be determined by measuring the sub-threshold luminescence from both facets of the device and using the equation[6]:

$$\alpha(\lambda_o) = -\frac{1}{L_{pass}} \ln\left(\frac{J_{pass}(\lambda_o)}{J_{act}(\lambda_o)} \right) \qquad (1)$$

where $\alpha(\lambda_o)$ is the wavelength dependent absorption coefficient (in cm⁻¹), $J_{pass(\lambda o)}$ is the luminescence power from the passive waveguide (in mW), and $J_{act(\lambda o)}$ is the power from the active laser side. The losses were calculated in this manner for all the lasers in the bar and the average was found to be 16 cm⁻¹. This value represents the average loss of the entire passive waveguide section over the lasing wavelength range. It is expected that the losses are higher close to the interface (where the bandgap is narrower) and lower in regions away from the active section. The optical scattering loss in the gain section for this particular laser wafer was found to be 28 cm⁻¹, found by fabricating OSLs of different lengths and measuring

their *P-I* characteristics. It is therefore evident that the propagation losses have been reduced by the intermixing process.

The passive loss of 16 cm⁻¹ for the extended cavity broad area devices should also be compared with the value of 28.7 cm⁻¹, being the effective passive section propagation loss for the ridge waveguide lasers in which the interface region was unpumped (Section IV). Despite the lack of transverse guiding in the broad area devices, the effective propagation loss is lower confirming the benefits of pumping the graded interface.

VI. Laser Spectra

The lasing spectrum of a 600 μm OSL is shown in Fig. 6, taken at a drive current of I_th + 500 mA, indicating a peak lasing wavelength of around 1500 nm. The lasing spectrum of an ECL is shown in Fig. 7, which indicates that the peak lasing wavelength has blue shifted by around 25 nm to 1475 nm. The shift in lasing wavelength to higher energy is due to the large increase in current density in the active region of the device. This shift in lasing wavelength will cause the propagation losses to increase slightly, since the energy of the photons is closer to the bandgap of the passive waveguide section. Thus, the loss of 16 cm⁻¹ is influenced by
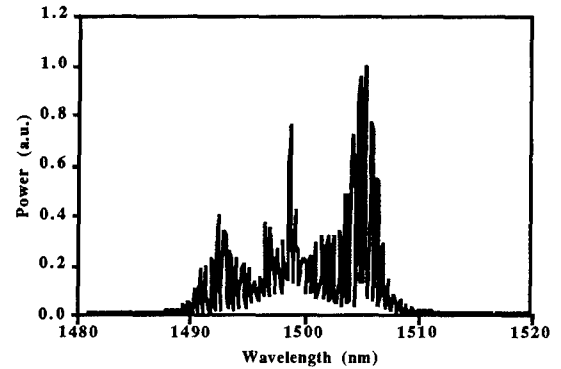
Fig. 6: Lasing spectrum of oxide stripe laser
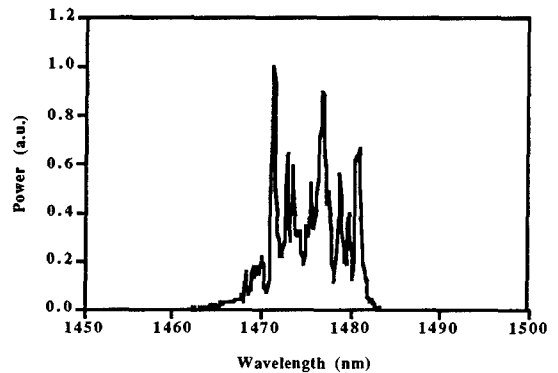
Fig. 7: Lasing spectrum of extended cavity oxide stripe laser

290
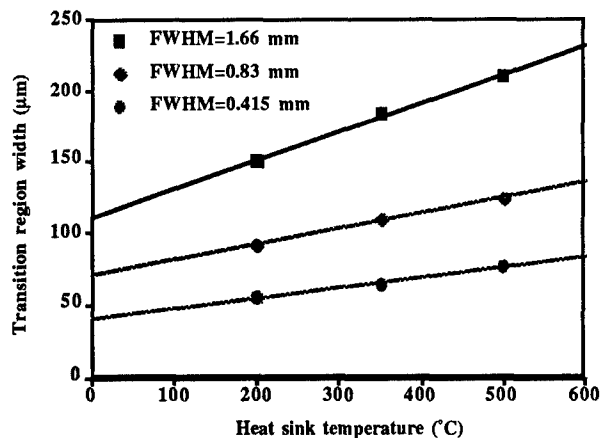
Fig. 8: Thermal modelling of transition region width for different heatsink temperatures and laser spot sizes.

the blue shift in lasing wavelength.

VII. Spatial Resolution

Modelling of the temperature distribution within a sample subjected to the PAID process has also been carried out. Because the thermal conductivity is strongly temperature dependent, a commercial nonlinear finite element package (ABAQUS) was used. The model confirmed that, for the condition used in fabricating the extended cavity device, the length of the graded region was ~100 to 200 μm. For a laser spot size with FWHM = 0.415 mm and a heatsink temperature of 200 °C, however, the transition width is 54.5 μm, which compares favourably with other forms of integration process such as selective area epitaxy.

Very much improved spatial resolution (<25 μm) can be achieved using a pulsed variation of the PAID technique[7], and it anticipated that use of the pulsed technique will lead to improved integrated devices.

VIII. Conclusions

Photo-Absorption Induced Disordering (PAID) has been used to widen selectively the bandgap in regions of a GRIN QW laser straucture. The bandgap widened regions have been used as the passive sections of extended cavity lasers, with non-bandgap widened sections being used as the gain sections. The spatial resolution of the process is ~100 to 200 μm, sufficiently large that it is necessary to pump part of the interface region to obtain a low average optical propagation loss in the passive section. Devices without the pumped interface section exhibit Q-switching behaviour, but no Q-switching effects are seen when the interface is pumped. The lowest passive section loss obtained here was 16 cm[-1], but

this figure was obtained from a slab device with poor coupling from the passive section into the gain section. It is, however, known that the propagation loss can be as low as 5 dB cm[-1] in PAID intermixed material[4], and ridge waveguide devices are expected to have very much superior characteristics.

IX. Acknowledgements

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291

COMPARISON OF InGaAs ABSORPTIVE GRATING STRUCTURES IN 1.55μm InGaAsP/InP STRAINED MQW GAIN-COUPLED DFB LASERS

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Abstract

In gain-coupled (GC) distributed-feedback (DFB) lasers of absorptive grating type, the device characteristics depend very much on the absorptive grating configuration such as duty cycle, layer thickness, conduction type, and material composition. We have fabricated 1.55μm InGaAsP/InP strained multiple quantum well (MQW) DFB lasers having different absorptive grating thickness and different conduction type. Lasing characteristics of these lasers were compared in view of coupling coefficients and absorption saturation. Through net gain measurement, information useful for designing and optimizing the absorptive grating was obtained.

I. Introduction

Gain-coupled DFB lasers have many advantages over conventional index-coupled (IC) DFB lasers such as high longitudinal single-mode yield [1], immunity to facet reflection [2]. Furthermore, these advantages can be obtained without using complicated phase-shifting structures like quarter wave phase shift or multiple phase shift.

In GC DFB lasers of absorptive grating type, the device characteristics depend very much on the absorptive grating configuration such as duty cycle, layer thickness, conduction type, and material composition. However, guideline for designing or optimizing absorptive grating has not been established. This is partly because there has been no easy and reliable method to evaluate coupling coefficients of DFB lasers precisely. Recently, automatic laser parameter extraction from subthreshold spectra has been made possible. It is applicable to both index- and gain-coupled DFB lasers even without facet anti-reflection (AR) coating. By using this method, most of DFB laser parameters such as coupling coefficients, grating phases at facets, effective refractive index, and its wavelength dispersion can be determined simultaneously [3, 4].

We have fabricated 1.55 μm InGaAsP/InP strained multiple quantum well (MQW) DFB lasers having different absorptive grating thickness and conduction type. Since some of the laser parameters might vary above threshold, we demonstrate net gain measurement in order to understand how the absorptive grating behaves with output optical power. Then, we compare lasing characteristics of these lasers in view of coupling coefficients and absorption saturation in the absorptive grating.

II. Device Structure and Fabrication

Figures 1 and 2 illustrate the bird's-eye view and the
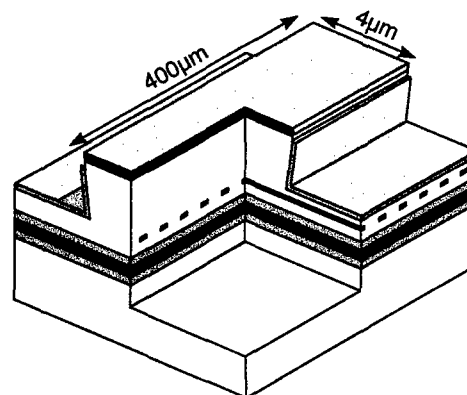
Fig. 1. Schematic drawing of the ridge-waveguide absorptive-grating gain-coupled DFB laser.
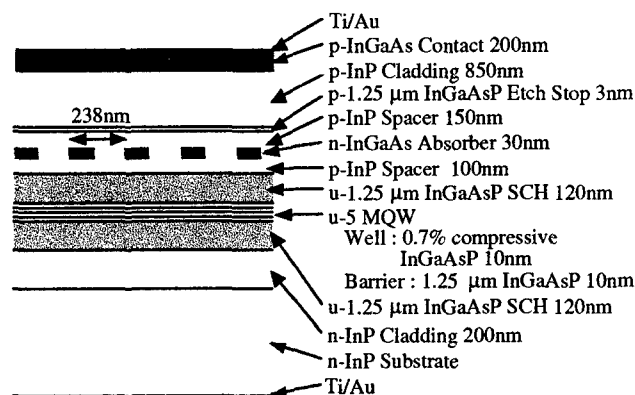
Fig. 2. Schematic longitudinal cross-section of the gain-coupled DFB laser with 30nm-thick n-InGaAs absorptive grating.

longitudinal cross section of the laser structure. The layers were grown by two-step metal-organic vapor phase epitaxy (MOVPE, AIX200/4) with TBP and TBAs as group V precursors. The growth temperature was 610°C and the pressure was 10kPa. The doping levels of the cladding, absorptive, and contact layers were about 5×10^{17} (Zn and S), 5×10^{17} (Zn or S), 1×10^{19} (Zn) cm^{-3}, respectively. The active layer is composed of five compressively strained (0.7%) InGaAsP wells and 1.25 μm barriers (10 nm thick each). The absorptive grating with 238 nm period was formed by holographic exposure and wet chemical etching of the InGaAs layer. Here, two different values were used for the thickness of the InGaAs absorptive grating, namely, 10 nm and 30 nm. For 30nm-thick absorber, both p-doped and n-doped InGaAs were tried whereas the 10nm InGaAs was undoped. Duty cycle of the grating was ~30 %. After the second step MOVPE on the grating, the wafer was made into ridge waveguide configuration (400 μm-long and 4μm-wide) by utilizing the 3 nm-thick quaternary etch stop layer. For the sake of comparison, conventional index-coupled DFB lasers were fabricated at the same time. Facets of the lasers were left as-cleaved. Laser chips were bonded on heatsinks with tin solder.

III. Characteristics

Typical cw threshold currents at 20°C were 18, 20, and 25 mA for IC and GC with 10 and 30 nm-thick gratings, respectively. Slight threshold increase is attributed to excess absorption by the grating. Index and gain coupling coefficients, κ_i and κ_g, were extracted from subthreshold spectra [3, 4]. Figure 3 shows a typical fitting result in the GC DFB laser with the 30nm-thick n-InGaAs absorber. Measured and calculated spectra are almost completely matched, and extracted κ_i and κ_g of this laser are 62cm^{-1} and -13cm^{-1}, respectively.

Bias dependence of index- and gain-coupling coefficients in different grating configurations are plotted in Figs. 4 (a) and (b). Since both real and imaginary parts of the refractive index of the InGaAs absorptive grating are different from those of surrounding InP, not only gain coupling but also index coupling is incorporated. The 30 nm-thick grating resulted in larger κ_i and κ_g (the minus sign of κ_g corresponds to loss coupling), which is reasonable.

In order to investigate saturation behavior of the absorptive grating, we measured net gain in the laser cavity by Hakki-Paoli method [5]. From peak to valley ratio r in measured spectra, cavity length L, and facet power reflectivity R, one can calculate net gain g_{net} by following equation,

$$g_{net} \equiv \Gamma g_{mat} - a_{loss} = \frac{1}{L}\ln\frac{\sqrt{r}-1}{\sqrt{r}+1} + \frac{1}{L}\ln\frac{1}{R} \qquad (1)$$

where Γ is optical confinement factor into active layer, g_{mat} is material gain, and α_{loss} is waveguide loss. Though equation (1) is for a Fabry-Perot cavity, we may apply this formulation to DFB lasers if wavelength is apart from the Bragg wavelength. R was assumed to be 0.3. Figure 5 shows bias
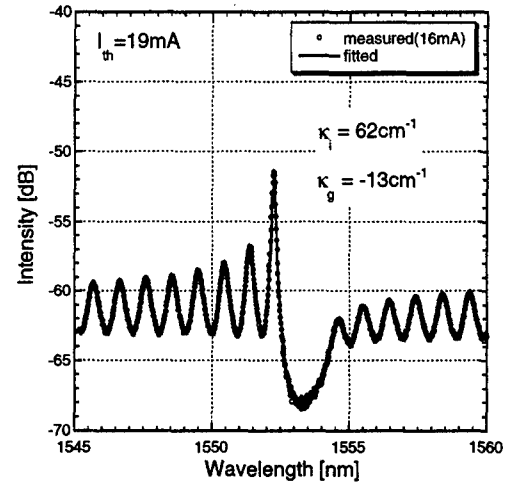
Fig. 3. Typical fitting result in the gain-coupled DFB LD with 30nm-thick n-InGaAs absorber.
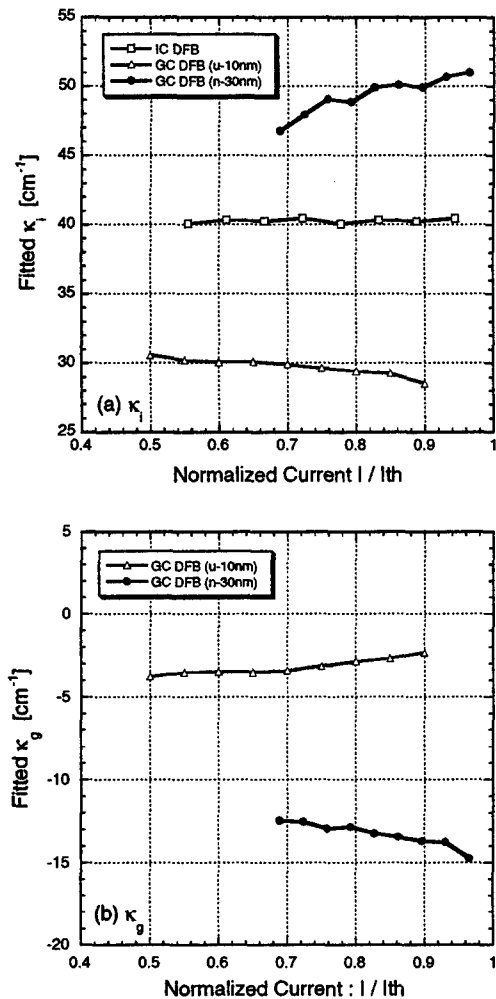
Fig. 4. Bias dependence of the index-coupling (a) and gain-coupling (b) coefficients extracted from subthreshold spectra.

293
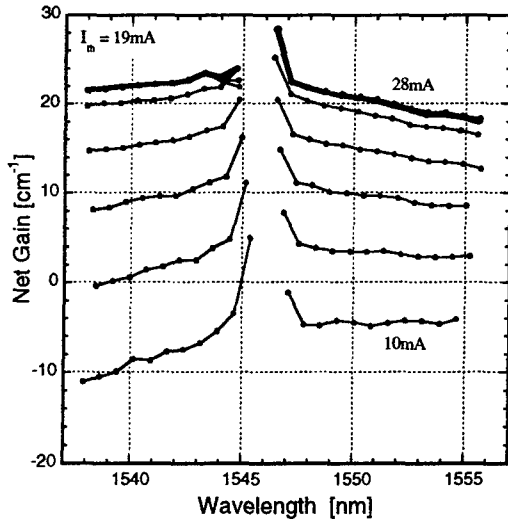
Fig. 5. Bias dependence of the net gain curve in the index-coupled DFB laser. Thick solid line represents threshold. Current step is 2mA.
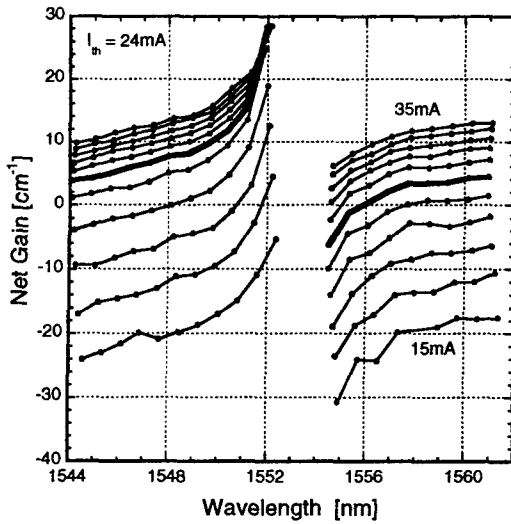
Fig. 6. Bias dependence of the net gain curve in the gain-coupled DFB laser with 30nm-thick n-InGaAs absorptive grating. Thick solid line represents threshold. Current step is 2mA.

Fig. 7. Net gain and output power versus normalized injection current.
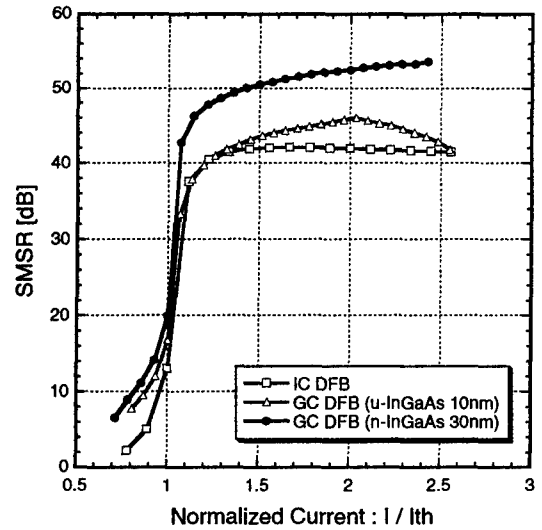
Fig. 8. Side mode suppression ratio versus normalized injection current.

dependence of the net gain curve in the index-coupled DFB laser. Due to the DFB modes, net gain cannot be evaluated correctly near the Bragg wavelength (around 1546nm in this laser). Thick solid line in the figure is at the threshold. Below threshold, net gain increases with bias current. However, when it reaches threshold, the gain stops increasing and remains constant. This is because carrier density in the active layer above threshold is fixed at the threshold value and therefore net gain is also unchanged.

In the GC DFB laser in Fig. 6, on the other hand, net gain

continues increasing even above threshold. This difference could be explained as follows. In GC DFB lasers, the modes whose standing wave antinodes overlap with the grating are absorbed, and thus side modes are suppressed. Above threshold, the main mode of the cavity is intensified, and absorption begins to saturate. This absorption decrease results in net gain increase through the reduction of the waveguide loss.

The large net gain discontinuity across the DFB mode in Fig. 6 is attributed to the absorption coupling; the modes on

294

the longer wavelength side have their antinodes overlapping on the absorptive grating while the modes on the shorter wavelength side have nodes on the grating, thus being free from the absorption. Such discontinuity is not observed in the index-coupled DFB laser in Fig. 5 as expected.

To make a comparison among different absorptive grating configurations, net gains at a certain wavelength (λ_{DFB} - 8 nm) are plotted against normalized injection current in Fig. 7, together with L-I characteristics. Above threshold, the gain in the IC DFB laser is flat and completely fixed. On the other hand, in the GC DFB lasers, the gains keep increasing. This tendency is more notable in the GC DFB laser with thicker grating. In 10nm-thick absorber, amount of the net gain change is very small and absorption saturation begins earlier than that in 30nm-thick n-InGaAs absorber. However, in 30nm-thick p-InGaAs grating, it is found that absorption saturation occurs rapidly right after threshold. Nonlinear behavior due to this rapid absorption saturation can also be seen in the L-I curve, which is similar to what was reported before in GaAlAs/GaAs material system [6]. In order to prevent the absorption saturation at relatively low output power level, conduction-type-inverted thick absorptive grating is effective.

Because of the absorption compression observed in Fig. 7, κ_g above threshold might be reduced. Since the parameter extraction is only applicable to subthreshold spectra, κ_g above threshold cannot be evaluated by fitting. Instead, we measured side mode suppression ratio (SMSR) of the lasers, the result of which is shown in Fig. 8. In the 10nm-grating GC DFB laser, the SMSR begins to decrease at twice threshold. This means that the absorptive grating doesn't work any more and the laser becomes like an index-coupled DFB laser as the output power increases.

However, the SMSR of the 30 nm n-InGaAs GC DFB laser is not much affected since the bleaching is not substantial as in the case of the 10 nm absorber GC DFB laser.

The above information helps understanding how the absorptive grating works above threshold, and is useful for designing the grating configuration.

IV. Conclusion

We have fabricated 1.55μm strained MQW ridge waveguide gain-coupled DFB lasers having different absorptive grating configuration. Both gain- and index-coupling coefficients of the lasers were extracted and determined successfully from the subthreshold spectra. By means of Hakki-Paoli net gain measurement, we compared absorption saturation behavior for different absorptive grating thickness and conduction type. Utilizing this information, design and optimization of the absorptive grating having desired coupling coefficients and saturation behavior would be possible.

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LOW-LOSS, LOW-THRESHOLD 0.98 μm WAVELENGTH InGaAsP/InGaP/GaAs BROADENED WAVEGUIDE LASERS GROWN BY GSMBE

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Abstract: We describe the design and experimental results for broadened waveguide (BW) high-power, low-loss, low threshold current 0.98μm aluminum-free InGaAsP/InGaP/GaAs lasers. The dramatic decrease in the internal losses with an increase in the width of the waveguide layer for a SCH-MQW structure, is attributed to lower free-carrier absorption due to the reduced overlap of the optical mode with the highly doped cladding regions. The BW lasers grown with both InGaAsP and GaAs waveguides show lower internal loss and threshold current than those designed for optimum optical confinement factor within the QW region. We report a record low internal loss of 2.2 cm^{-1} and highest CW output power of 6.8W for a InGaP/GaAs laser grown by GSMBE. We also report the highest quasi-continuous output power of 13.3 W measured for a single 100 μm aperture, 0.8-0.98 μm Al-free laser diode, grown by either MBE or MOCVD.

Introduction

The conventional designs for separate confinement heterostructure (SCH) lasers typically maximize the overlap of the optical mode with the gain in the quantum wells (QWs), resulting in a low threshold current density (J_{th}). While this design is appropriate for lasers operating near threshold current (I_{th}), in the case of high power lasers the operating current is greater than 10 x I_{th}, other laser parameters such as external differential and power conversion efficiency determine maximum output power. The broadened waveguide (BW) laser structures [1-2] represent a new approach in designing high efficiency high power lasers. By reducing the overlap between the optical mode and the highly-doped cladding layers (Γ_{CL}) the optical loss due to free-carrier absorption can be drastically reduced. The corresponding decrease in the confinement factor of the QWs (Γ_{QW}) is not as drastic and the threshold current density for long cavity lasers does not increase. Thus, long cavity lasers needed for high power operation can significantly benefit from the low-loss, high efficiency offered by the BW laser structure. Also the larger mode size results in reduced optical density and is critical for reducing COD and spatial hole burning. Recently, 0.98μm Al-free BW lasers grown by metal-organic chemical vapor deposition (MOCVD) have achieved powers in excess of 8 W [3].

We describe the experimental results for broadened waveguide high-power, low-loss, low threshold current 0.98μm aluminum-free InGaAsP/InGaP/GaAs lasers grown by gas-source molecular beam epitaxy (GSMBE). Internal losses decrease dramatically with an increase in the thickness of the waveguide layer for a SCH-MQW structure. The influence of waveguide thickness on threshold current density (J_{th}), internal loss (α_i) and differential efficiency (η_d) is studied for lasers fabricated on GaAs substrates with In$_{0.49}$Ga$_{0.51}$P cladding regions. The BW lasers grown with both InGaAsP and GaAs waveguides show lower internal loss and threshold current than those designed for optimum optical confinement factor within the QW region. We report a record low internal loss of 2.2 cm^{-1} for a InGaP/GaAs laser grown by GSMBE and CW output power of 6.8 W for a LR/HR coated, 3mm long device.

Device Structure

The BW lasers studied here (Fig. 1) consist of a separate confinement waveguide layer of thickness W, bound by 1.5-1.75 μm thick In$_{0.49}$Ga$_{0.51}$P cladding layers. The active region is comprised of two 80Å In$_{0.15}$Ga$_{0.85}$As well separated by 200Å barrier made of the waveguide material. Lasers designed to maximize

Γ_{QW} and minimize J_{th} typically use W = 0.15-0.3 μm, for a variety of waveguide materials. The BW lasers, on the other hand, are designed to minimize Γ_{CL} but must use W $\leq$ W$_{max}$, viz. the maximum waveguide thickness before the onset of the second even mode. For the InGaAsP(E_g=1.53eV) waveguide lasers, as the waveguide thickness increases from W=0.23μm to 0.95μm, the calculated cladding layer confinement factor decreases from 34% to about 3%, while the QW confinement factor only decreases from 4.3% to 2.6%. To study the corresponding decrease in internal loss with increase in waveguide thickness, three otherwise identical InGaAs/InGaAsP(E_g=1.53eV)/InGaP lasers were grown with various waveguide thicknesses of 0.23μm, 0.47μm and 0.75μm. For these lasers, the waveguide and active layers were undoped and a 800Å undoped InGaP buffer layer is grown before the top p-cladding InGaP layer. The Be-doping profile in the cladding region is abrupt with N_A~3x10^{18}cm^{-3}. The n-type Si-doped cladding layer is also doped to a constant level of 2x10^{18}cm^{-3}.
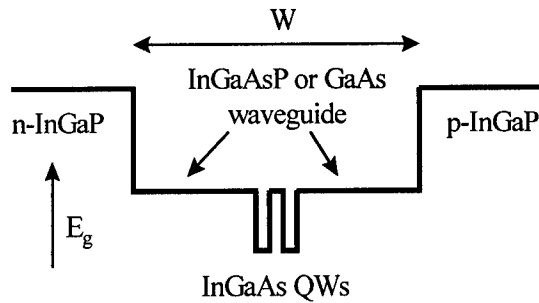
Figure 1. Schematic diagram of 0.98 μm InGaP/InGaAsP/ GaAs laser structure.

The internal loss for each structure is determined from the slope of inverse external efficiency versus cavity length for broad-area, uncoated 100μm stripe lasers. For comparing conventional and BW laser, another structure (D) was also grown with the same waveguide thickness as (A) but instead of abrupt high doping a graded doping profile is used in the cladding regions. The InGaP:Be layer is linearly graded from 5x10^{17}cm^{-3} at the edge of the waveguide region to 5x10^{18}cm^{-3} near the top contact, which resembles the standard doping profile for a conventional laser. The lasing wavelength for the lasers made from these structures was 0.97-0.99 μm.

Growth and Fabrication

One of the difficulties in growing these lasers by MBE is the different growth temperatures that must be used to achieve good optical quality material for the different layers. The highest quality GaAs is grown at ~600°C, whereas In$_{0.49}$Ga$_{0.51}$P and InGaAsP must be grown at a much lower temperature of ~480-510°C. This is attributed to the high vapor pressure of P at 600°C, as well as the rapid surface loss of In at elevated temperature. For the lasers in this study, we used growth interruptions to change substrate temperatures. In the case of lasers with GaAs waveguides, most of the waveguide region was grown at 600°C, while low temperature GaAs (510-525°C) was used near the active region and for the barrier between the InGaAs QWs.
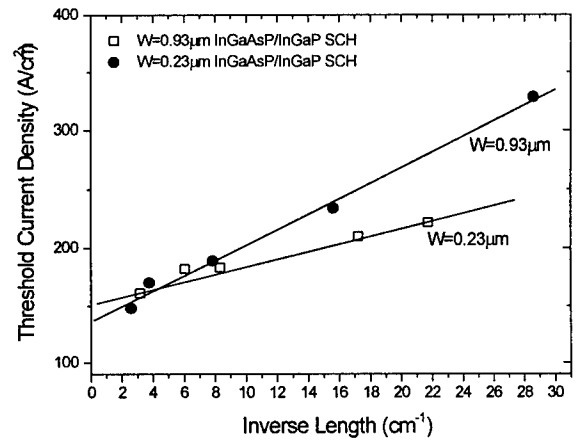
Figure 3. Threshold current density as a function of inverse cavity length for conventional and BW InGaAsP waveguide lasers.

Broad area lasers with 100 μm-wide stripes have been fabricated. Following a photolithography step the 100 μm wide stripes are exposed. Next, p-type metal (200 Å:Ti/500 Å:Pt/1000 Å:Au) is deposited. The top GaAs contact layer is etched between adjacent stripes. The wafer is thinned to ~ 100 μm and the back contact (270 Å:Ge/450 Å:Au/215 Å:Ni/1000 Å:Au) is deposited and annealed at 360°C for 15 seconds.

Results

Broad area lasers with uncoated facets were tested at room temperature using 1μs pulses at 10 KHz. The measured internal efficiencies are approximately the same for all three wafers (η_i = 82$\pm$2%), while internal optical losses (α_{in}) decrease almost six-fold with

a fourfold increase in W (see Table 1). Since the reduction in the optical confinement factor for cladding layers is greater than for the quantum wells, J_{th} for BW lasers is lower for long cavity length (L > 1.7mm) devices, as shown in Fig. 2. The threshold current for long cavity BW lasers ranges from 140-160 A/cm^2. Figure 3 shows the external quantum efficiency for these lasers. The internal loss for structure D (conventional laser with graded doping) is similar to the broadened waveguide laser B with W=0.47μm but is significantly lower than that for laser A (same W, but abrupt doping). This clearly shows that internal loss can be reduced by decreasing the overlap of the optical mode with the high doping density regions The lowest internal loss (3.2 cm^{-1}) is obtained for the BW laser with the widest waveguide (W=0.93μm, C). Further reduction in losses is possible by reducing the doping levels to ~1x10^{18} cm^{-3}.

3.3-9.1 cm^{-1} for a similar device grown by GSMBE [4-6].
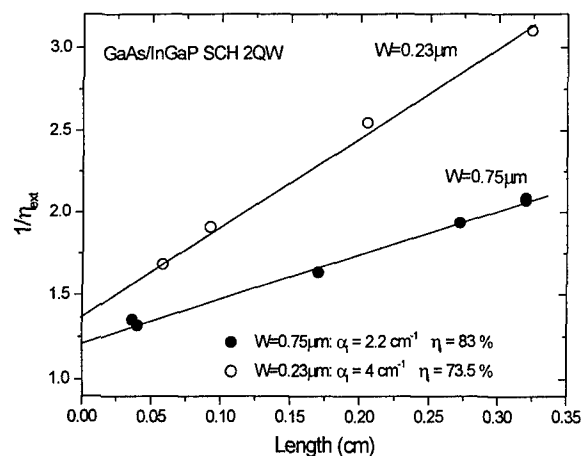
Figure 4. Reciprocal differential efficiency versus cavity length for GaAs waveguide of different thickness.

Figure 3: Reciprocal differential efficiency versus cavity length for InGaAsP waveguide of different thickness.

To eliminate any possible effect of alloy scattering in the waveguide material, BW lasers were also fabricated with GaAs as the waveguide material. These lasers were grown with graded doping(similar to structure D) in the cladding regions, thus resulting in lower internal losses. Figures 4 and 5 plot 1/η$_d$ versus L and J$_{th}$ versus 1/L, respectively. It is seen that increasing the waveguide width from 0.23 to 0.75μm decreases α$_{in}$ from 4.0 to 2.2 cm^{-1}. The α$_{in}$~2 cm^{-1} from Figure 4 is a record for GSMBE grown 0.98 μm wavelength InGaP/GaAs/InGaAs lasers and is significantly lower than the previous reported results of

Figure 5. Threshold current density as a function of inverse cavity length for conventional and BW GaAs waveguide lasers.

Low values of internal loss, threshold current density, and thermal and electrical series resistance are important factors for fabrication of high power, long cavity laser diodes. For the GaAs waveguide lasers a low resistance of 0.04 Ω was obtained for a 100μm stripe, 3.3 mm long laser, mounted p-side down on a Cu heat-sink. For uncoated devices CW powers of ~2 W were achieved. Figure 6 is a plot of CW output power as a function of current for a 3mm long (W=0.75μm) LR(5%)/HR(95%) coated. The output power of 6.8 W is the highest power ever reported [4-6] for a Al-free

298

980nm laser grown by MBE and is second only to the 8.1 W obtained for a MOCVD-grown InGaAs/InGaAsP/ GaAs 0.98 µm laser [3]. We also measured the output power from the same laser (Fig. 6) in a quasicontinuous (QCW) mode using 100 µs wide pulses at 100 Hz. The QCW power of 13.3 W, shown in Fig. 6, is the highest reported value for any 0.98 µm laser diode. The COD value at the output facet for a QCW power of 13.3 W is calculated to exceed 20 MW/cm².

Conclusion

In summary, we have tested the validity of the broadened waveguide concept as applied to 0.98 µm wavelength InGaAsP/GaAs/InGaP based high power lasers. By simply reducing the optical overlap with highly doped regions, internal losses have been improved to record low values, with no degradation in J_{th} for long cavity devices. We demonstrated a record low internal loss of 2.2 cm⁻¹ for a InGaP/GaAs laser grown by GSMBE and CW output power of 6.8 W for an LR/HR coated, 3 mm long device. Also the QCW power of 13.3 W obtained is the highest reported value from a single laser in the 0.8-1.0 µm range.

Acknowledgments

Figure 6. CW and QCW output power versus current for 3-mm cavity length GaAs broadened waveguide laser.

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Waveguide Material	Doping Profile	W (µm)	Γ_{CL} (%)	Γ_{QW} (%)	α_{in} (cm⁻¹)	η_i (%)
A:InGaAsP	abrupt	0.23	34.3	4.36	18.5	80.6
B:InGaAsP	abrupt	0.47	12.3	3.66	4.6	83.3
C:InGaAsP	abrupt	0.93	3.0	2.5	3.0	83.3
D:InGaAsP	graded	0.23	34.3	4.36	4.3	83.3
GaAs	graded	0.23	26.2	5.04	4.0	73.5
GaAs	graded	0.75	3.3	2.9	2.2	83.0

TABLE 1. Summary of output loss and internal efficiency for various waveguide widths and waveguide materials.

HIGH TEMPERATURE STABILITY AND ELECTROSTATIC DISCHARGE SENSIBILITY OF InGaAs/InP AVALANCHE PHOTODETECTORS

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Introduction

Temperature dependent dark current-voltage measurements performed on four different types of Separate Absorption Grading Multiplication avalanche photodiodes showe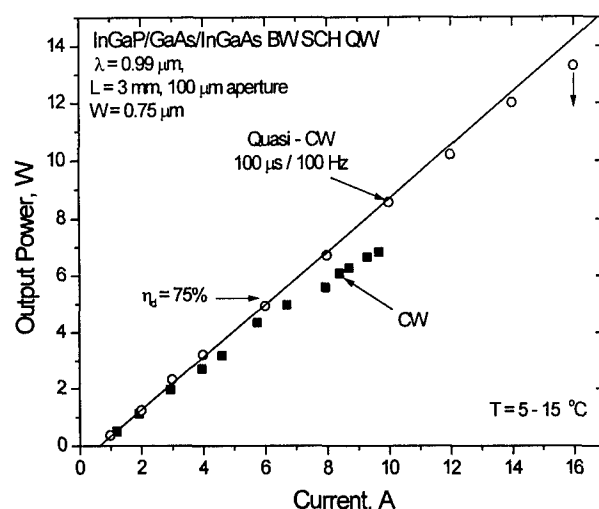d that the increase of the dark current can be described for all devices by a single activation energy and that the breakdown voltage increases strictly linearly with temperature, both in a wide temperature range between 25°C and 150°C. Three types of avalanche photodiodes showed no performance degradation during 5000h of a temperature step-stress test at temperatures up to 150°C, while for another device type with active layer inhomogeneities already at low temperatures a continuous lowering of the breakdown voltage, followed by a rapid increase of the dark current has been observed. During electrostatic discharge tests the avalanche diodes failed at pulse amplitudes between 700V and 1400V.

I. Background

Avalanche photodiodes (APDs) have the advantage of inherent photocurrent gain and better noise performance at high modulation bandwidths (1) but suffer from poorer photoresponse homogeneity (2) with respect to pin photodiodes.

In the existing literature regarding the reliability of InGaAs/InP APDs, an increase of the unmultiplied surface current has been often observed after bias stressing at elevated temperatures (3,4,5), related to positive charge buildup in the dielectric surface passivation layer. Inhomogeneities have been reported on the failed devices, and in most cases local avalanche breakdown close to the guard-ring has been observed by light beam induced current measurements (3,4).

We performed a constant current stress test at stepwise increasing temperatures and showed that also active layer inhomogeneities - identified by electroluminescence imaging - can induce device degradation.

II. Device structures

In this work we report on measurements performed on devices of four different families (labelled A,B,C,D) of commercially available avalanche photodiodes, all from the top illuminated Separate Absorption Grading Multiplication

(SAGM) type. For a description of the different types of InP based APDs the reader is referred to (6).

The main difference among the investigated APD families is the definition of the lateral electrical confinement. The photodetectors from the family A exhibit a rather simple structure with a single guard-ring and with a multiplication layer defined by the p$^+$ diffusion into an n$^-$-InP layer. The guard ring is created by ion implantation. In the family B the multiplication region is defined by a n-InP mesa buried into the n$^-$-InP layer and a guard-ring at the junction edges. Devices from family C have two guard-rings with a PLEG structure (Preferential Lateral Extended Guard-ring). For the APDs from family D the multiplication area is obtained by silicon implantation; the p$^+$ region is larger than the Si implanted area in order to prevent edge breakdown at the curved junction. It is the only type investigated here without guard-ring structure. A detailed description of the investigated APD types can be found in (2).

III. Results and discussion

A. Temperature dependence of the dark current - voltage characteristics

In order to verify that no change in the conduction mechanisms occurs within the temperature
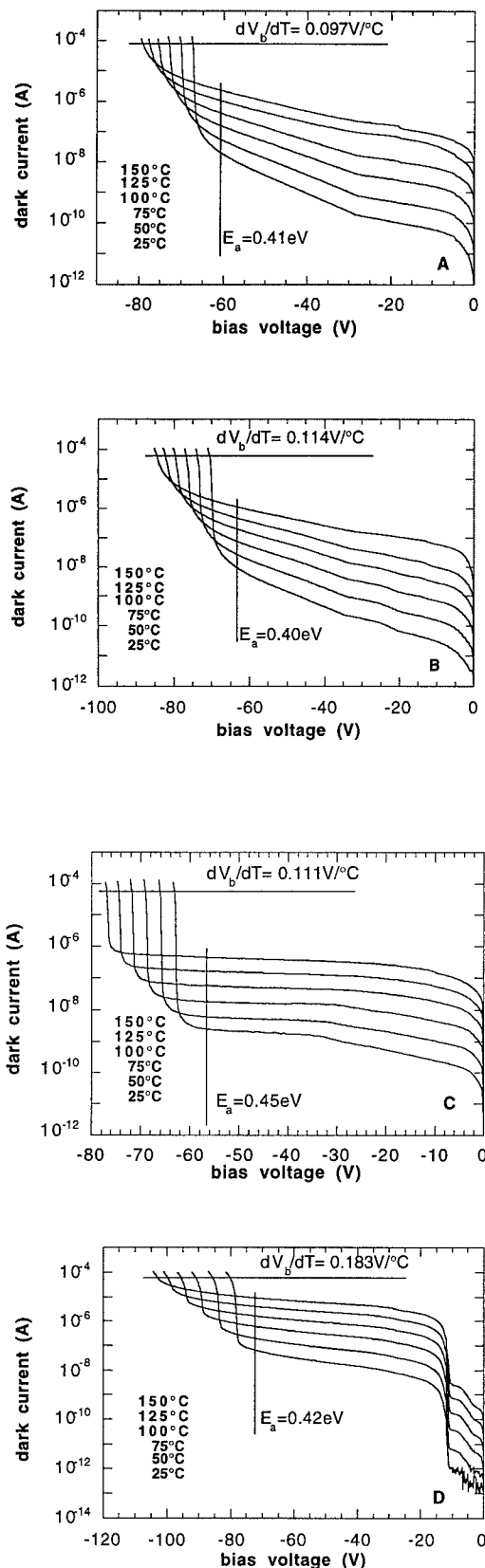
range of the step-stress test, we measured the temperature dependence of the dark current - voltage (IV) characteristics of the four avalanche photodiodes in steps of 25°C between 25°C and 150°C.

An Arrhenius plot of the dark current at a given reverse bias voltage (here at 90% of the room temperature breakdown voltage value) shows that this current can be described by a single activation energy (E_a) in the whole investigated temperature range. The values for the different APD families varieing between 0.40eV and 0.45eV are indicated in Fig.1. We defined the breakdown voltage (V_b) as the value of the bias voltage, where the reverse dark current reaches a value of 100μA. For all four APDs the breakdown voltage increased linearly with increasing temperature and temperature coefficients between 0.097V/°C (family A) and 0.183V/°C (family D) have been determined in agreement with literature data on similar devices (7).

The devices from family D exhibited additionally rather high dark current values for reverse bias voltages exceeding -11V and in the breakdown regime an ohmic behaviour with a series resistance exceeding 20kΩ.
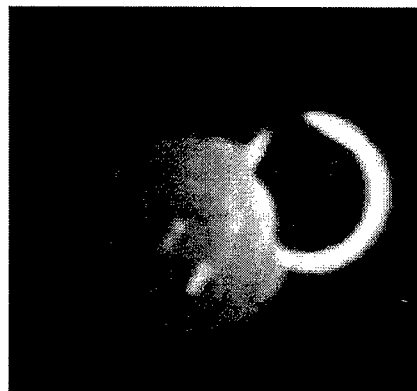
Fig.2 *Electroluminescence image of an APD from family D with a reverse bias current of 200μA. The image has been superposed to the homogeneaous forward bias image in order to identity the position of the bright spots on the active area.*

In Fig.2 an electroluminescence image of this APD taken with a reverse bias current of 200μA shows that the current in the breakdown regime is localized to small spots of the photodiode active area. The same inhomogeneity has also been observed in the photoresponse map, indicating an inhomogeneous charge carrier multiplication. This can be due to inhomogeneous doping or due to layer thickness fluctuations. The high series resistance in the breakdown regime is reflecting the

Fig.1 *Reverse bias dark IV characteristics of the four different APDs measured at different temperatures.*

301

space charge limitation of the current, when microplasma formation is observed.

B. Temperature step-stress test

After characterization at 25°C, for two devices from each APD family a long term stability test at successively increasing temperatures (25°C, 100°C, 150°C) has been performed under constant current conditions (100µA) in the reverse bias breakdown regime. During this test the dark current - voltage (IV) characteristics of the APDs have been measured at short intervals at the respective test temperature. In addition, at longer intervals the APDs have been cooled down to 25°C and a complete characterization of the electrooptic properties has been performed at that reference temperature.
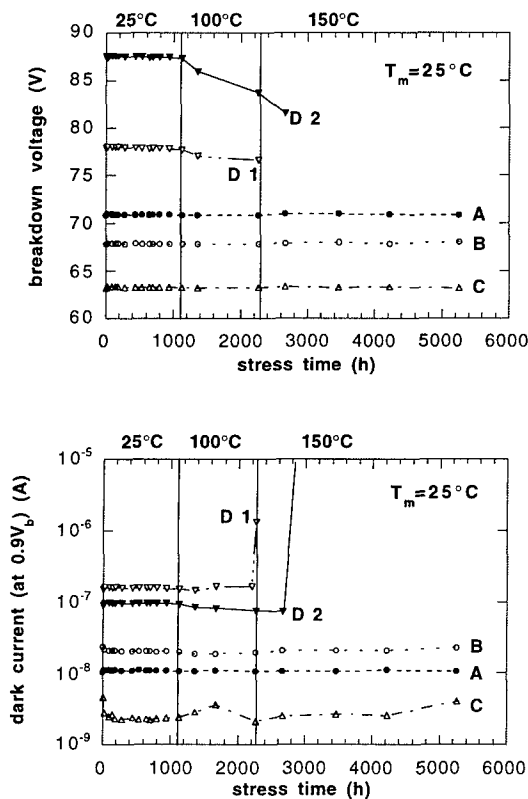
Fig.3 *Monitoring of: A) the breakdown voltage and B) the dark current at an applied reverse bias voltage corresponding to 90% of the breakdown voltage, measured at 25°C during a constant current step stress test with successively increasing temperatures*

The development of the breakdown voltage and of the reverse dark current at a bias voltage corresponding to 90% of the breakdown voltage, both measured at 25°C, have been plotted in Fig.3 as a function of the stress time. The two devices

each from the A,B and C APD families exhibited very similar behaviour, so that for simplicity only one curve each is shown. The APDs from the three APD families with guard ring structure did not show any variation of the breakdown voltage during the single steps for a complete stressing time of more than 5000h, while both devices from the APD family - with ion implanted active layer - exhibit a typical degradation during bias stress at 100°C and 150°C respectively. At first the breakdown voltage shifted to lower voltages, then a rapid increase of the dark current has been observed. In the case of the APD D1 a minor diminution of the breakdown voltage has been already observed during the 1100h bias stress at 25°C and during the 100°C step the breakdown voltage shift accelerates. The dark current remains stable during the first 2200h of bias stress and increases sharply after 1200h stress time at 100°C. The breakdown voltage shift at this time accumulates to a value of -2V.

The degradation of the APD D2 is in detail seen in Fig.4 and Fig.5. The IV reverse bias characteristics measured at 25°C before stress and after the 100°C step (Fig.4) reveals that the initial degradation results also in this case only in a decrease of the reverse bias breakdown voltage. Already during this step a shift of -6V has been observed and no dark current increase is observed. Furthermore the breakdown characteristics becomes less sharp for high current values. The final degradation of the APD D2 can be seen in Fig.5 where the development of the IV characteristics during the 150°C step is shown. After 600h of current stress at this temperature a 3V decrease of the breakdown voltage can be observed with no further changes of the IV characteristics in the whole bias voltage range. After 800h the breakdown voltage remained fairly stable and for bias voltages below -11V an increase of the dark current for about two orders of magnitude can be observed. After 895h, an increase of the dark current in the whole temperature range is observed and the sharp step in the IV characteristics at -11V disappeared. Since this step is related to a heterojunction barrier in the bulk of the device, we can conclude that after about 800h current stress at 150°C a surface current path is created and the reverse bias current even at 150°C is no more dominated by the bulk current. A possible explication is that the electric field near the microplasma range becomes high enough to allow injection of charge carriers into the top isolation layer. The captured charge carriers can then induce a highly conductive surface

302

current channel in the underlying semiconductor layer.
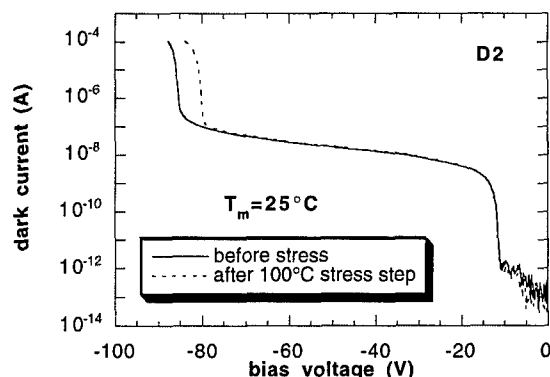
Fig.4 *Dark IV characteristics of device D2 measured at 25°C before and after bias current stressing at 100°C.*
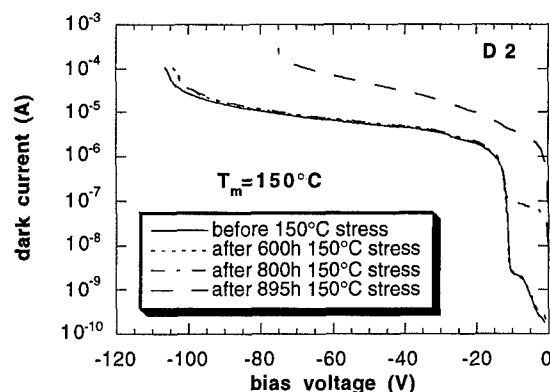
Fig.5 *Dark IV characteristics of device D2 measured at different times during the bias stressing at 150°C.*

C. Electrostatic discharge sensibility

Table 1 *Failure voltage range of the different APD families during ESD-testing*

device family	voltage range (V)
A	1300-1500
B	700-1100
C	1200-1400
D	700-900

Electrostatic discharge tests have been performed, applying one positive and subsequently one negative ESD pulse each - conforming to the human body model - with successively increasing amplitudes to 6 devices of each APD family, starting from 100V until 400V in steps of 50V and subsequently in steps of 100V. The dark current-

voltage characteristics of the APDs have been monitored after each ESD pulse.

Device destruction occured in all but one case during the negative pulse application within the voltage ranges indicated in Table 1.

IV.Conclusions

For three InGaAs/InP SAGM avalanche photodiodes families with different guard-ring structures we found no performance degradation during a constant current stress test of complessively more than 5000h at succesively increasing temperatures up to 150°C, while the only APD family without guard-ring structure showed already at 100°C a derivation of the dark current-voltage characteristics. The degradation started with a decrease of the breakdown voltage, followed by the formation of a surface leakage current path and was strongly related to inhomogeneities in the current distribution as revealed by electroluminescence imaging.

V.References

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InAlAs/InGaAs/InP field effect transistor with carbon-doped InAlAs buffer layers

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Introduction

InGaAs/InP composite channel transistors have potential applications in high speed optoelectronic integrated circuits due to their dynamic and DC performances [1] [2]. Indeed, the high mobility of InGaAs combined with the high breakdown field and high electron velocity of InP are favorable parameters to obtain high cutoff frequency and low leakage current, and so, make it a good candidate for such application. In this paper we investigate MOVPE structures, in particular HFETs on InAlAs buffer layers, and the influence of the InGaAs channel parameters -thickness and doping- on both gate leakage current and breakdown voltage. Furthermore, the reverse doped structure has been optimized for highest Hall mobility.

I-Device structure

The InAlAs/InGaAs/InP heterostructures were grown by MOVPE at 650 °C. A cross section of the epitaxial layers and the associated band diagram are shown fig.1 and 2. The buffer consists of InAlAs grown at low temperature directly onto the Fe-doped InP substrate, which yields high resistivity layers [3]. In our study, the buffer is composed of a 100 Å undoped $In_{0.52}Al_{0.48}As$ layer grown at 500 °C, followed by a 300 Å $In_{0.52}Al_{0.48}As$ growth at 650°C. The upper part of the structure, grown at 650 °C, consists of a 250 Å homogeneously or δ-doped n-type InP donor/channel layer, followed by an undoped InP layer which acts as a spacer, a $In_{0.53}Ga_{0.47}As$ channel layer and a 500 Å $In_{0.52}Al_{0.48}As$ barrier layer. Finally a 400 Å $In_{0.53}Ga_{0.47}As$ doped layer was grown as a cap layer.

We have investigated the DC characteristics of such a transistor for two structures with homogeneously doped InP sub-channel layer with a 20 Å spacer layer: the InGaAs channel thickness of the first one is 40 Å and it contains a sheet carrier concentration of 4.1×10^{12} /cm^2, the second is 100 Å thick with a carrier concentration of 2.4×10^{12} /cm^2. The measured mobilities are respectively 2910 cm^2/V.s and 2180 cm^2/V.s. Theses values are typical of InP, although, the C-V curves indicate that carriers are in the InGaAs channel. Moreover high mobilities obtained in direct doped HEMT MOVPE structures (~ 9000 cm^2/V.s) do not allow to incriminate the InAlAs/InGaAs interface quality.

II-Electrical influence of InAlAs buffer

The Id (Vds) curves (Fig.4-a,Fig.6-a) show good pinch-off characteristics. The InAlAs thickness must be well adjusted : on the one hand, too strong a compensation by deep acceptors [4] of the InP donor layer can localise the essential of the conduction in the InP channel (see Fig. 2). On the other hand, a good buffer isolation must be insured while avoiding pertubations connected with kink and drain lag effect. A 100 Å layer is sufficient to satisfy these two constraints ; sheet resistivities of 10 MΩ have been measured with perfect reproducibility. In this configuration, we found hysteresis and other slow trap relaxation effects to be less pronounced than with InP[Fe] buffer FETs [5].

Fig. 1: device structures
left: uniform doping, right: delta doping
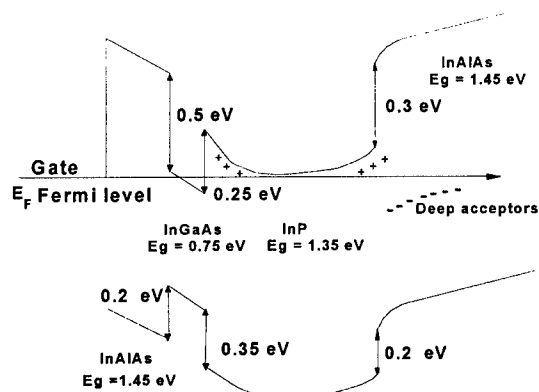
Fig. 2: band diagram of InGaAs/InP composite
channel FET heterostructure

The gate tunnel current (at low electric fields) is due to the filling of the InGaAs channel associated with both doping concentration and thickness. These parameters have a large influence on the position of the Fermi level of the channel and so condition the effective thickness of the InAlAs barrier layer. This hypothesis is confirmed by device simulation (CNET-QUASAR) of two stuctures with the same homogeneous doping concentration in the InP channel but with different InGaAs channel thicknesses (40 Å, 100 Å) (Fig. 5). This simulation explains the larger gate tunnel current observed with the 40Å channel devices.

We observe the good localisation of free carriers using Cgs(Vgs) measurements. Fig. 3 shows the depletion width as a function of Vgs bias and confirms that 2/3 of the conduction takes place in the InGaAs channel.
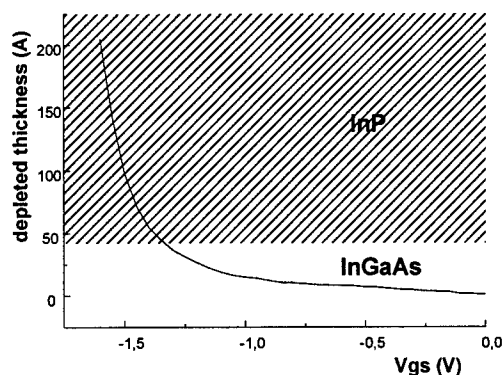
Fig. 3: depleted thickness versus Vgs bias voltage
($V_{pinch-off}$=-1.6 V)

III-leakage current analysis

The comparison of the DC characteristics of the two structures (fig.4-a,b, fig. 6-a,b) clearly indicates an improvement of the gate leakage current by simultaneously decreasing the doping concentration and increasing the channel thickness. The maximum current is reduced by a decade at Vds=2 V and reaches a value as low as 400 nA/mm for the common bias conditions Vds= 2 V, Vgs=0 V which is small enough to avoid sensitivity degradation of PIN-FET circuits by gate current shot noise. This effect is strongly dependent on carrier concentration: at increased doping, electric fields become stronger in the InGaAs channel with the higher charge (40 Å-4.1×10^{12} /cm²) and consequently, for the same bias conditions the ratio Ig(impact ionization)/Id is higher in the first structure.

4.a)

4.b)

Fig. 4-a,b : FET DC characteristics with a 40 Å
InGaAs channel thickness (W=50 μm, Lg=0.8μm)

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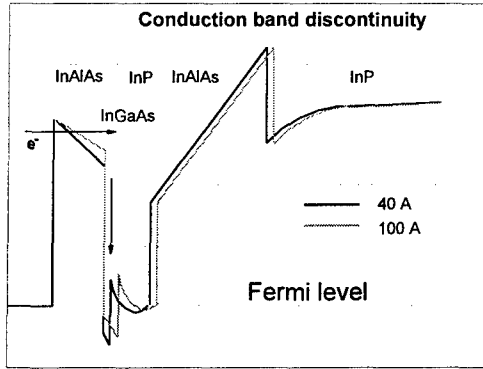
Fig. 5: conduction band diagram for two channel thicknesses 40 Å and 100 Å

IV- Breakdown voltage analysis

The structures show a significant difference of the breakdown voltage: 7 V against 9 V. The better behavior at high electric fields is obtained for a 40 Å channel layer in spite of the larger gate leakage current. This is in agreement with recent publications of similar structures grown by MBE used for power applications [6]. The reduction of the thickness of the InGaAs induces an effective increase of the bandgap of the channel due to energy quantisation and therefore improves breakdown voltages [7] (with and whithout pinch-off).

6.a)
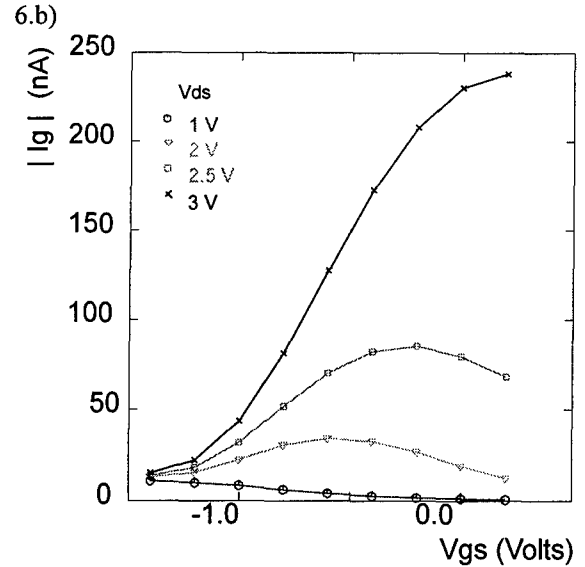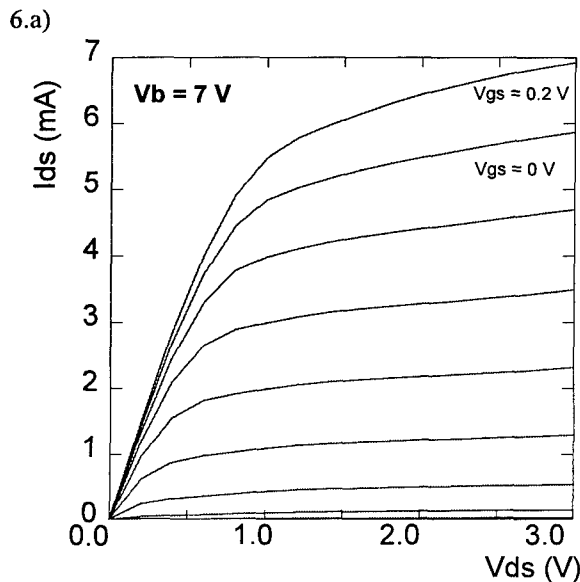
Fig 6-a,b : FET DC characteristics with a 100 Å InGaAs channel thickness (W=50 μm, Lg=0.8 μm)

IV-Mobility measurements

We have carried out Hall measurements on structures with different doping profiles - homogeneously or δ-doped- for two InGaAs channel thicknesses: 40 Å and 100 Å. The results are shown in table 1 and table 2.

e_{ch} (Å)	40				100
Ns (10^{12}/cm²)	2	2.4	6	11	4.1
μ (cm²/V.s)	3000	2910	2000	1600	2180

Table 1: uniform doping of InP layer

e_{ch} (Å)	100 Å				
Ns (10^{12}/cm²)	1.6	1.9	3.6	4	5
μ (cm²/V.s)	3070	2570	2880	2300	1300

Table 2:Si δ-doped InP layer

All these combinations show low Hall mobility. This limitation of mobility has already been observed on inversed doped structures grown by MBE and has first been attributed by Brown [8] to Si surface segragation. This hypothesis is supported in our case by the improvement of mobilities when increasing the InP spacer layer. We have obtained a maximum value of approximately 5000 cm²/V.s with a 100 Å spacer layer. Such a spacer is too thick to insure a good electronic transfer to the InGaAs channel layer: our simulation (QUASAR) showed an optimum at a 20 Å spacer layer.

306

e$_{spacer}$ (Å)	20	40	100
Ns (10^{12}/cm^2)	1.6	1.3	1.7
μ (cm^2/V.s)	3070	3700	4760

Table 3: spacer influence with δ-doped InP layer

Therefore, the epitaxy of InGaAs/InP double channel FETs with delta-doping below the InGaAs layer involves a compromise between charge transfer efficiency and mobility.

The composite channel structure is promising for OEIC design : low gate leakage current, high breakdown voltage, perfectly isolated substrate/FET interface. A careful optmization of the InGaAs part of the channel is required: to improve breakdown voltage without increasing the tunnel leakage current and without deteriorating electronic confinement. Moreover, in the long gate FETs investigated, showing high f_{max} ,(~60 GHz for a 0.8 μm gate lengh), the conduction essentially takes place in InGaAs at low electric fields and in InP at high fields. Yet, the InGaAs/InP interface shows rather low Hall mobilities due to Si surface segregation, wich explains the moderate f_t (~20 GHz). Further work is under way to block this diffusion and therefore improve the mobility of the structure with thinner spacer layers.

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RAPID THERMAL MOCVD OF InGaAs/InP MULTILAYERS

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High quality InGaAs/InP multilayers have been grown by means of rapid thermal low pressure metalorganic chemical vapor deposition (RT-LPMOCVD), using tertiarybutylphosphine (TBP) as phosphorous source and tertiarybutylarsine (TBA) as arsenic source. The undoped featureless films exhibited an excellent morphology with a narrow x-ray peak of 30 arcsec for InGaAs layer on RT-LPMOCVD grown InP, reflecting a lattice mismatch of 0.02%. A test structure of three Quantum Wells lattice matched InGaAs/InP structure ($\approx$50 Å width of each layer) were grown following determination of the optimum growth parameters for InGaAs and InP layers.

I. Background

The growth of III-V semiconductors by means of RT-LPMOCVD, earlier realized successfully for GaAs and AlGaAs on GaAs substrates [1-3] and for InP and InGaAs on InP substrates [4,5] uses rapid and precise changes in the substrate temperature driven by switching of halogen-tungsten lamps, to control layer growth rather than applying the gas phase switching technique normally used in the standard MOCVD technique.

The ability to control the growth of abrupt interfaces is advantageous for currently used InP based devices for optical communication systems. In view of this need, the RT LPMOCVD technique looks attractive, carrying the potential of a control to the monolayer level for InP based compounds, as a result of the rapid elevation and reduction of the wafer temperature above and below the reactive temperature.

The RT-LPMOCVD technique combines rapid thermal annealing and chemical deposition processes. Figure 1 contrast the process cycles for the RT-LPMOCVD and LPMOCVD. From this scheme one can see that the major advantage of the RT-LPMOCVD technique is the elimination of the pre-processing high temperature wafer exposure step. This step is particularly critical in the deposition of conductive layer or in second growth process, in order to eliminate interfacial reactions. Thus in a conventional LPMOCVD process, the III-V semiconductor substrate is heated until it stabilizes at the reaction temperature, after which the deposition reaction temperature is initiated. Long high temperature exposure generally could lead to some level of surface degradation and interface reactions.

In this work we provide demonstration of the epitaxial growth of a undoped heterostructure layers of InP/InGaAs by means of RT-LPMOCVD.

II. Experimental

InP layers were grown on Fe doped, semi-insulating (100) InP substrates by the RT-LPMOCVD technique, using A. G.
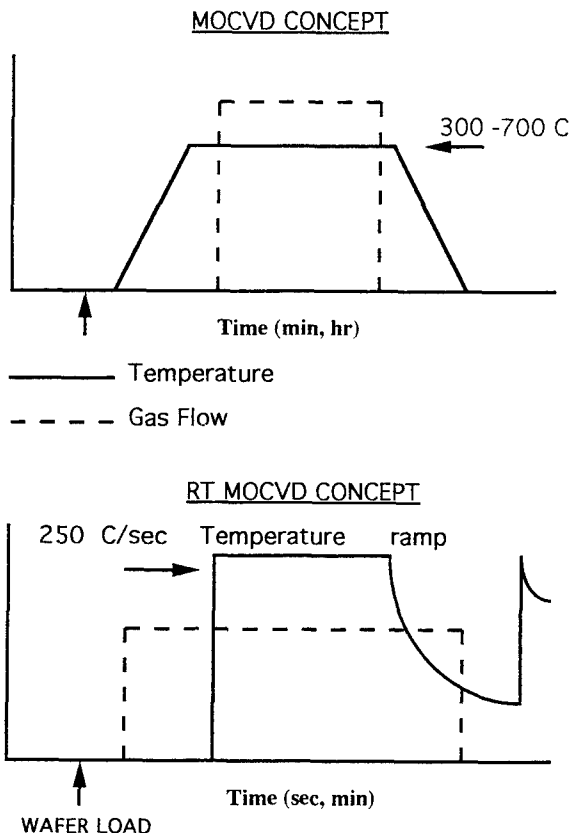
Fig. 1 Schematic presentation of the LPMOCVD and RT-LPMOCVD conceptual process schedule

Associates Heatpulse CVD 800 system. This is a low pressure, load lock, horizontal, and laminar flow reactor, heated by two sets of high power halogen tungsten lamps (20 lamps of 1.5 kW each) and is capable of processing a single wafer. The growth and load lock chambers were pumped by turbomolecular pumps to a vacuum of 10^{-6} Torr.

Prior to growth, The InP substrates were cleaned using a standard process, and immediately loaded into the reactor.

Trimethylindium (TMIn), triethylgallium (TEGa), tertiarybutylphosphine (TBP) and tertiarybutylarsine (TBA) have been used as indium, gallium phosphorous, and arsenic sources respectively. Hydrogen purified by Nanochem®, gas purifier was used as the carrier gas for the metalorganic precursors.

Four crystal x-ray difractometry, Photoluminescence (PL) and Auger electron spectroscopy (AES) were used to characterize the InP and InGaAs film quality. Room temperature Hall measurements (Hg-In alloyed contacts) were used to obtain the sample carrier concentration and mobility.

III. RT-LPMOCVD of InP and InGaAs layers

As a first step we investigated a range of values for the key growth parameters of InP. The optimum growth conditions in our system were found to be at temperatures of 525 °C, at a pressure of 1 Torr, for at a growh rate of up to 2μm/h. The optimum TBP flow rate was 70-80 sccm with TMIn flow rate of 0.15 sccm, with bubbler temperature of 30 °C. The undoped featureless films exhibited an excellent morphology .X ray diffraction showed a well defined, narrow peak as shown in Figure 2, confirming the high quality of the epitaxial layer. The full width at half maximum (FWHM) of the InP peak was measured to be 15 arcsec. Luminescence intensities similar to those that were measured at layers that grown by conventional MOCVD were found at these layers.
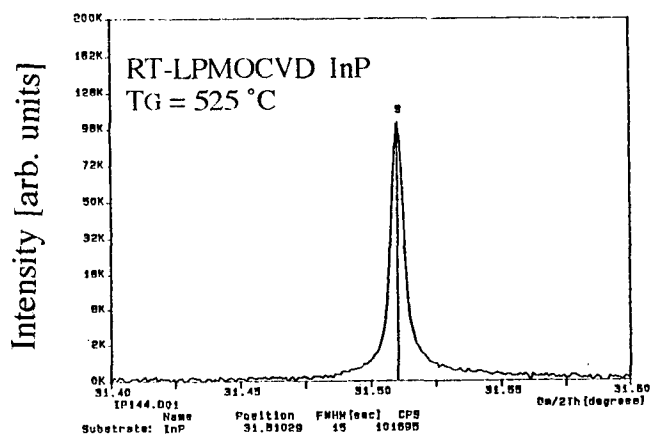
Fig. 2. Four crystal x-ray diffractometry of an undoped RT-LPMOCVD InP layer grown on SI-InP at 525 °C for 10 min.

The featureless layers were measured to have n type background doping levels of $Nd \approx 5*10^{16}$ cm^{-3}, and 300K mobility of 3500 $cm^2/V*s$. The AES data, provided in Fig. 3, shows good stoichiometry and a uniform distribution of the elements in the InP layer, with a negligible amount of oxigen and carbon contaminants incorporated in the film.

sputter time (min.)
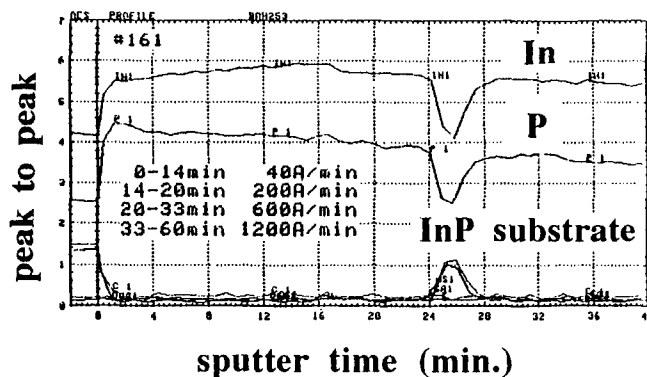
Fig. 3. AES depth profile of undoped RT-LPMOCVD InP layer grown on SI-InP at 525 °C (growth time 12 minutes).

The optimum growth conditions for lattice matched InGaAs on InP were identified through set of growth runs, through which the key growth parameters were modified. The temperature was varied in the range of 450-550 °C, pressure in the range of 0.5 to 5 Torr, growth duration in the range of 2 to 20 minutes and metalorganic flow rates in the range of 1 - 75 sccm. The best results were achieved at growth temperature of 550 °C, flowing 70 sccm of In, 5sccm of Ga and 32 sccm of As into the chamber, keeping the metalorganic bubblers at temperatures of 25, 30 and 5 °C respectively. The undoped featureless films exhibited narrow x-ray full width at half maximum, reflecting very small lattice mismatch.

IV. RT-LPMOCVD of InGaAs/InP heterostructures

In the next step of the study we used the special feature of the RT-LPMOCVD system to grow the different layers subsequently, but at different temperatures using gas switching steps at low temperatures below the deposition reaction.

The steps for heterostructure growth of InP/InGaAs are the following: First 10 minutes of InP growth at 525 °C as described before At the end of this step, the gas flow of TMIn was stopped and the wafer temperature was cooled down, in TBP atmospher, to 480 °C in two seconds, while the chamber was pumped down to vacuum of about 10^{-3} Torr. Subsequently TBA and TEGa flows were started and the TBP was closed. In the next step TMIn flow was started again, the temperature raised to 550 °C, and RT-LPMOCVD cycle of InGaAs was executed at the conditions mentioned in the former paragraph.

Figure 4 shows the four crystal x-ray diffractometry spectrum taken from a sample of 0.6 μm layer of InGaAs that was grown on 0.8 μm InP layer grown on SI-InP substrate.
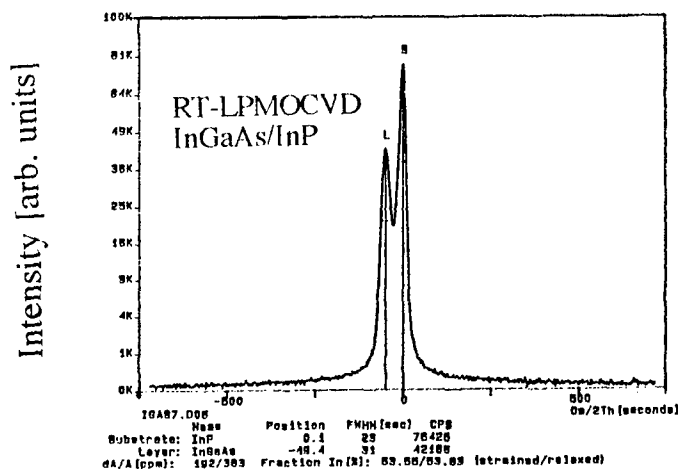
Fig. 4. Four crystal x-ray diffractometry of undoped RT-LPMOCVD InGaAs/InP heterostructure grown on SI-InP.

Fig. 5. Schematic growth process flow chart of RT-LPMOCVD of undoped InP/InGaAs/InP heterostructure.

The FWHM InGaAs peak was measured to be 30 arc sec, the peak splitting reveal in InGaAs lattice mismatch in the InP layer of about 0.02%, suggesting that a high quality InGaAs layer was grown

Multiple quantum wells structure were grown by RT-LPMOCVD using the similar growth process scheme. During growth interruptions and cooling times the reactor was purged with group V elements. At the InP/InGaAs interface a growth interruption of 3 sec was used. The TBA was switched on immediately with starting the heating stage and the TBP was switched off 2 sec before starting growth of InGaAs well. A similar sequence was used for the switching of the gas phase at the InGaAs to InP interface. The duration of interruptions was also 3 seconds at this interface. Fig. 5 and 6 show the gas switching procedure and the temperature profile used in our study of three quantum wells ($\approx$50 Å wells and barriers widths) deposited on 0.1μm thick InP buffer layer grown on (100) oriented SI-InP substrate.

The quantum wells sample was analyzed by PL measurement at 77K. An Argon laser was used for photopumping. The laser beam was focused on the sample surface yielding a pump density of 100mW/cm^2. The spectral distribution of the emitted signal was measured with 0.5 monochromator using liquid nitrogen cooled Ge detector, with conventional lock-in technique. The 77K PL spectra for the InGaAs/InP three quantum wells is shown in Figure 7. The luminescence of the 3 QW's structure is characterized by a single peak close to the theoretically expected energetic position.

Fig. 6. Growth temperature sequence scheme for InP/InGaAs/InP QW's deposition by RT-LPMOCVD.

310

InGaAs/InP 3QW, T=77K
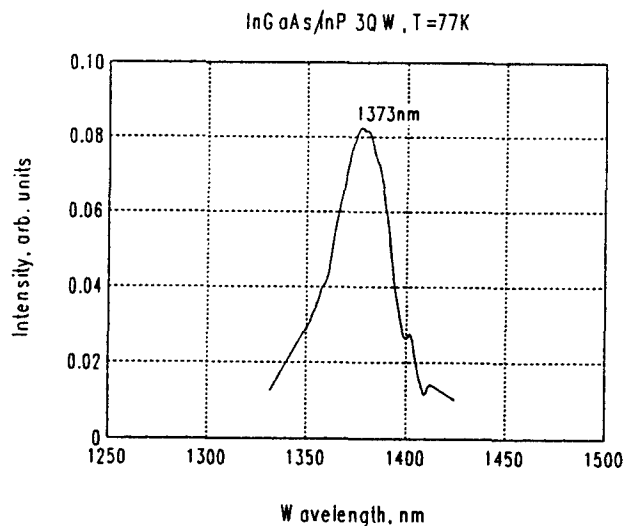
Fig. 7. 77K photoluminescence spectrum of 3 QW's
InP/InGaAs/InP grown by RT-LPMOCVD on InP

V. Conclusions

In conclusion, we have demonstrated the potential of the
RT-LPMOCVD technique for the growth of a good quality
epitaxial InGaAs/InP heterostructures and multiple quantum
well structues on InP substrates. Preliminary characterization
by electrical measurements, x-ray diffraction, Auger electrons
spectroscopy, and PL measurement provided promised results,
which are as good or similar to the widely reported
heterostructures properties grown by MOCVD. Further work
has to be done for optimizing the growth process and using the
special features of the RT-LPMOCVD technique.

Acknowledgment

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Effect of Gas Switching on InP/InGaAs Interfaces During CBE Growth

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INTRODUCTION

The InP/InGaAs material system has several beneficial material properties which enable the development of high performance optical and electrical devices. However, high quality epitaxial layers with abrupt interfaces are necessary to attain the performance predicted. Several growth techniques, including metalorganic vapor phase epitaxy (MOVPE), chemical beam epitaxy (CBE), and gas source molecular-beam epitaxy (GSMBE), have been used to grow high quality layers with varying success in achieving abrupt interfaces.[1,2,3] The difficulty in realizing abrupt interfaces arises from the As-to-P or P-to-As exchange process that occurs at heterointerfaces during the switching of the group V species. The presence of significant levels of residual As or P can degrade the interface due to the high incorporation efficiency of these molecules on the opposite terminated surface.[4] In order to reduce residual levels of As or P, high pumping speeds, close-coupled run/vent switching, and separate hydride crackers may be necessary.[5] An added concern during CBE growth is the presence of residual group III molecules which can form unwanted transition layers at interfaces during subsequent growth. Formation of the poor interfaces can lead to both an increased difficulty in the fabrication of devices, if thick interfacial layers are present, and degradation of device performance due to scattering from rough interfaces. With the use of an optimized switching scheme the formation of these interfacial layers can be minimized. Several researchers have investigated the effect of switching on interfaces. A combination of growth/group III pauses as well as group V pauses, followed by the introduction of the opposite group V source prior to growth have been used.[2,3,6] Researchers have shown varying degrees of success in reducing the extent of the interface layers, though interface layers on the order of 2-3 monolayers still remain. Tsang, *et. al.*, has reported the best results in terms of low-temperature photoluminescence data, however, no information is available on the switching scheme used.[1] In this paper, the effect of a simple gas switching sequence on interface abruptness during CBE growth is studied using double crystal x-ray diffraction (DCXRD), photoluminescence (PL), and scanning tunneling microscopy (STM). Optimization of the switching sequence produces monolayer abruptness for both the InP/InGaAs and the InGaAs/InP interfaces.

EXPERIMENTAL PROCEDURE

All of the structures investigated in this study were grown in a Perkin Elmer (PHI) model 430P MBE system which has been modified for GSMBE and CBE growth. The standard cryo-pump and diffusion pump have been replaced with a 2200 l/s turbomolecular pump and a 5000 l/s cryo-pump. Group V constituents were derived by the thermal cracking of AsH_3 and PH_3 using separate Ta-based "fast-switching" hydride crackers. Using pressure-based flow controllers downstream of the bubbler, undiluted trimethylindium (TMIn) and triethylgallium (TEGa) were injected using a common pryolytic boron nitride-based injector. Close-coupled run/vent switching was employed for all gases, in order to minimize source "memory effects".

All epitaxial structures were grown at a substrate temperature of 490 °C on semi-insulating Fe-doped InP (100) substrates which were In soldered to Mo blocks. Substrate

temperatures were measured using an infrared optical pyrometer which was calibrated by observing the melting point (525 °C) of InSb. The growth rates for InP and InGaAs were kept constant at 1.05 μm/hr and 2.25 μm/hr, respectively.

Quantum well (QW) structures were grown to investigate the effect of both PH_3 and AsH_3 anneal times on interface abruptness. The structures consisted of a 1800 Å InP buffer, 20 periods of 300 Å InP and 60 Å InGaAs wells followed by a 1800 Å InP cap layer. The annealing times, τ_1 and τ_3, were varied for the different growths with double crystal x-ray diffraction measurements used to determine the effects of these variations (Figure 1). During GSMBE growth using this system, the PH_3 and AsH_3 vent times, τ_2 and τ_4, were determined earlier as 7 seconds and 20 seconds and will be used here.[2] During this vent time, background levels of As and P are reduced by over two orders of magnitude.
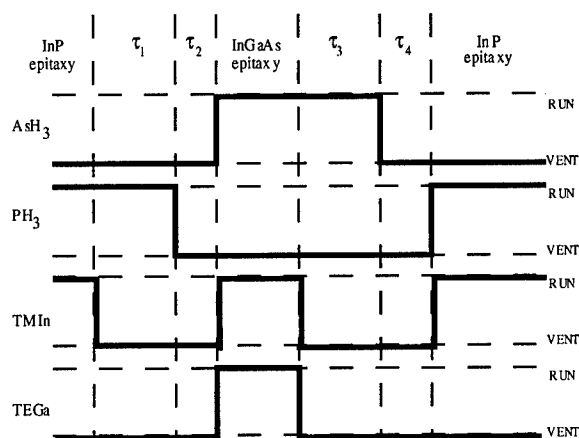
Figure 1 - Gas switching sequence for the CBE growth of InP/InGaAs. The switching sequence consists of an anneal and vent time for both PH_3 and AsH_3. The optimized switching sequence of τ_1, τ_2, τ_3 and τ_4 was determined to be 10 sec., 7 sec., 20 sec., and 20 sec.

Once an optimized switching scheme was determined, a structure consisting of 2500 Å InP buffer, 1000 Å InGaAs reference layer, and 100 Å, 75 Å, 50 Å, and 25 Å InGaAs QWs separated by 600 Å of InP barriers was grown. PL spectra at 5K were measured using an Ar+ laser with an optical power of 250 mW at 5145 Å. FWHM of

PL luminescence peaks were measured as well as energy shifts as a function of well thickness.

Finally, scanning tunneling microscopy measurements were made on samples with optimized and non-optimized switching schemes in order to directly examine the extent of the interfacial layer.

DATA and ANALYSIS

InGaAs quantum wells, 60 Å thick, with 300 Å InP barriers were grown with τ_1 values of 5, 10 and 20 seconds. τ_2, τ_3, and τ_4 were fixed at 7, 20 and 20 seconds, respectively. The double crystal x-ray diffraction FWHM of the 1st order satellite peak was compared for the different samples (Table I). A broadening of this peak indicates the presence of interfacial layers, implying that for times less than 10 s, there is insufficient time for residual group III molecules absorbed on the surface to be removed so that they are subsequently incorporated. Though very little difference exists as far as the FWHM of the satellite peak for the 10 and 20 s PH_3 anneal times, a slight surface roughness is observed in samples with 20 s anneals as observed by Nomarski microscopy. Additionally, the room temperature PL (RT-PL) peak shifts to longer wavelength. This shift maybe due to the incorporation of residual As from the chamber during the long delay. Though during the PH_3 anneal, background levels of As are typically about 3 orders-of-magnitude lower than the P levels, the long delay combined with the near unity incorporation efficiency of As lead to the formation of an interfacial layer that causes this shift. These results indicate that an anneal time of 10 s is sufficient to prevent the formation of an interfacial layer at the InP to InGaAs transition.

Table I - Summary of DCXD and room temperature PL as PH_3 anneal time is varied

τ_1	FWHM of Sat. Peak	RT-PL Wavelength
5 sec.	91.1 arc. sec.	1.558 μm
10 sec.	28.3 arc. sec.	1.549 μm
20 sec.	30.4 arc. sec.	1.564 μm

In order to optimize the AsH_3 anneal time, a similar set of samples were grown except that

the τ_3 values were chosen at 10, 20, and 40 s. τ_1, τ_2, and τ_4 values were fixed at 10, 7 and 20 s, respectively.(Table II) For times greater than 40 s, a broadening of the 1st order satellite peak is observed as well as a shift to longer wavelengths in the room temperature PL. This is most likely due to the incorporation of residual P at the surface with prolonged growth delays, thereby forming a strained interfacial layer. Though the exchange mechanism for P on a As terminated surface has been reported to be less than As on a P surface, the effect still needs to be considered when long growth pauses are used.[5] For times less than 20 s, a degradation of the surface is observed in the form of surface roughness. This degradation may be attributed to insufficient time for residual group III molecules that are absorbed on the surface to be removed. Their subsequent incorporation during the initial InP growth, leads to surface roughness. For this reason an anneal time of 20 s is chosen.

Table II - Summary of DCXD and room temperature PL as AsH₃ anneal time is varied

τ_3	FWHM of Sat. Peak	RT-PL Wavelength
10 sec.	28.7 arc. sec.	1.580 μm
20 sec.	28.3 arc. sec.	1.583 μm
40 sec.	51.5 arc. sec.	1.591 μm

X-ray diffraction results as well as simulation results using a commercially available dynamical simulation package from Bede Scientific are shown for 20 period QWs grown with the optimized switching scheme.(Figure 2) For the simulation, interface layers were included at both the P to As and As to P transitions, with the assumption that only InAs layers will be present. With this switching scheme, time is allowed for the removal of residual growth III molecules and group V molecules. The strong As/P exchange mechanism however is difficult to overcome at both the InP and InGaAs surfaces, therefore a thin InAs layers may be present. At the InP surface, this is due to the introduction of As during InGaAs growth, while at the InGaAs surface, InAs is formed due to introduction of In during InP growth. The thickness of the layer, however, can be minimized. For 20 periods of 60 Å InGaAs wells with 300 Å barriers, the best fit to

this data is obtained when 0.45 ML of InAs at the InP to InGaAs transition and 0.45 ML of InAs at the InGaAs to InP transition are assumed.
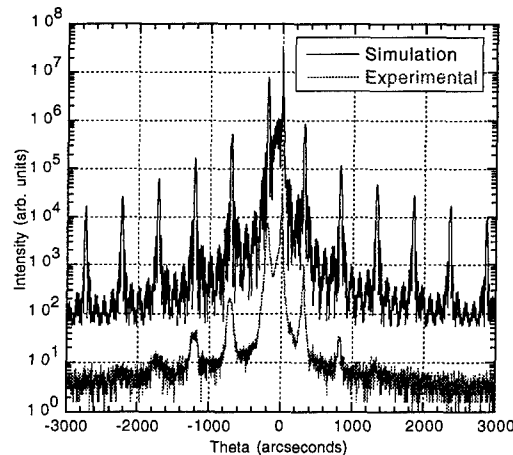
Figure 2 - Experimental and simulation results of 20 periods of 60 Å InGaAs wells with 300 Å InP barriers. The simulation was fit by including a 0.45 ML of InAs interfacial layer at both sides of the quantum well.

Low temperature PL measurements of a structure consisting of QWs with different thickness, grown using the optimized switching scheme, are shown in Figure 3 . The FWHM of the PL peak of the 25 Å QW is 15.8 meV, which is below the value calculated by Welch, et al.for 1 ML of thickness variations in 25 Å quantum wells.[7] This indicates that the interface layer is less than a total of 1 ML. Additionally, the energy shift of the PL to QW thickness is comparable to data reported by Tsang et. al., further indicating excellent interfaces.(Figure 4)[1]
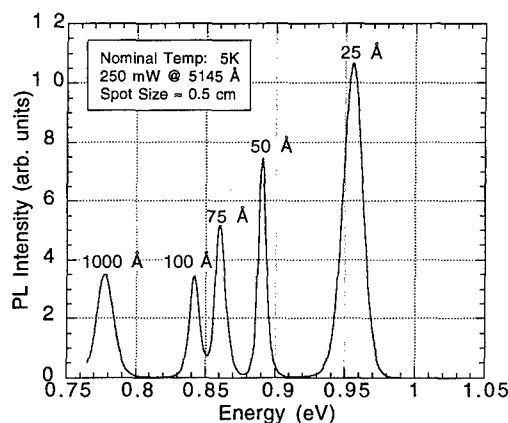
Figure 3 - 5 K PL spectra of 25 Å, 50 Å, 75 Å, and 100 Å InGaAs QW with 600 Å InP barriers. A 1000 Å marker layer is included as a energy reference.
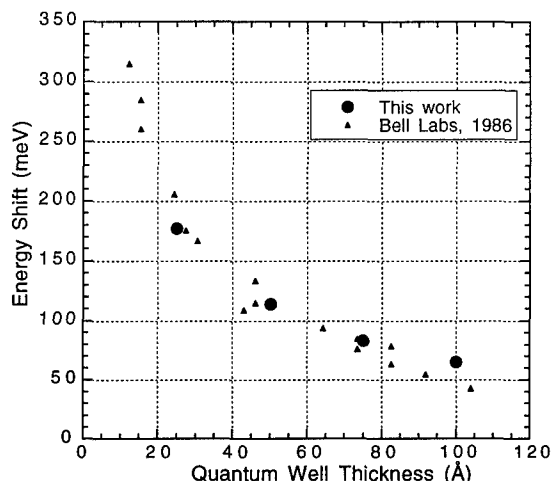
Figure 4 - Energy shifts of the luminescence from quantum wells with different thickness. Measured data is similar to that reported by Tsang et. al..[1]

Figure 6 - STM picture of a 60 Å InGaAs (light region) quantum well with InP barriers. The growth direction is from left to right. The optimized switching scheme was used. Fluctuations along both interfaces are on the order of 1 ML.

CONCLUSION

Finally, scanning tunneling microscopy measurements (STM) were conducted on a sample with a non-optimized switching scheme and one with an optimized scheme in order to directly observe the presence of interfacial layers. Figures 5 and 6 show a 60, 7, 60, 20 and 10, 7, 20, 20 s switching schemes, respectively. From figure 5, for the non-optimized switching scheme, we observe a 2-3 ML interface layer, as evidenced by the significant fluctuation in the intensity along the interfaces. In Figure 6, for a sample grown using the optimized switching scheme, fluctuations on the order of 1 ML are present. From this we conclude that by optimizing the switching scheme, 1 ML abruptness can be obtained for both interfaces

The effect of a simplified switching scheme on interface abruptness is investigated. By optimizing the anneal and vent time for both the As to P and P to As transition, near monolayer control can be obtained. This is evidenced by the x-ray rocking curve measurements, low-temperature PL measurements, and STM results. An optimized scheme of 10, 7, 20, and 20 seconds is determined to produce abrupt interfaces, with less than a monolayer of interfacial layer present.

Figure 5 - STM picture of a 60 Å InGaAs (light region) quantum well with InP barriers. The growth direction is from left to right. The non-optimized switching scheme of 60, 7, 60 and 20 seconds (τ_1, τ_2, τ_3, τ_4) was used. Fluctuations along interfaces are on the order of 2-3 ML.

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DEGRADATION OF CRYSTALLINE QUALITY DUE TO INTERFACIAL STRAIN IN SHORT PERIOD LATTICE-MATCHED GaInAs/InP SUPERLATTICES

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Introduction

Superlattices of $Ga_{0.47}In_{0.53}As/InP$ were grown by metalorganic molecular beam epitaxy. Abrupt interfaces were obtained when the total superlattice period was larger than about 85 Å. When the total period was less than 85 Å the onset of three-dimensional growth was observed. Since no group III atom intermixing was detected in our samples we attribute this effect to the intrinsic interface strain.

I. Background

Phenomena related to strain induced by the InP/ $Ga_{0.47}In_{0.53}As$ interface have been observed in many studies [1-11]. The strain is attributed to either the intrinsic strain due to the unavoidable presence of the InAs or $Ga_{0.47}In_{0.53}P$ monolayers at the interfaces [1,4], or to an "extrinsic" strain caused by intermixing of group V elements [3]. A third possibility for interface related strain is exchange of group III atoms across the interface [12], however, it has been argued that this effect is negligible in comparison to the intermixing at the group V sublattice [6, 9].

Here, we report on the growth of InP/$Ga_{0.47}In_{0.53}As$ superlattices (SLs) by the metalorganic molecular beam epitaxy (MOMBE) method. The period of the SLs was varied between 660 Å and 68 Å, and the ratio between well and barrier thickness was also varied. It was found that when the SL period was larger than 85 Å the interfaces were abrupt, as evident from the intense and narrow line width , (6 meV), in low-temperature photoluminescence (PL), and the presence of sharp strong satellite peaks in high resolution x-ray diffraction (HRXRD), Fig. 1 (a). Smooth interfaces were observed in dark field cross-section transmission electron microscopy, (TEM), images, Fig. 1 (c). However, when the SL period was less than 85 Å we observed a clear degradation of the crystalline quality in PL, HRXRD and by TEM. The degradation shows up as a broadening of the peaks in the PL and the HRXRD spectra, Fig. 2 (a), and as wavy interfaces
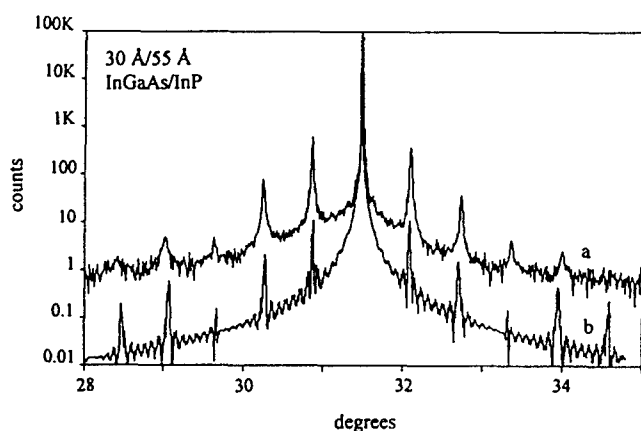
Figure 1. (a) X-ray diffraction plot of a 20 period $Ga_{0.47}In_{0.53}As$ superlattice with a period of 85 Å and well width of 30Å. (b) Simulated x-ray diffraction plot of the same structure.

Figure 1 (c) (200) dark field TEM image of a 20 period $Ga_{0.47}In_{0.53}As$ structure with a period of 600 Å and well width 60 Å.
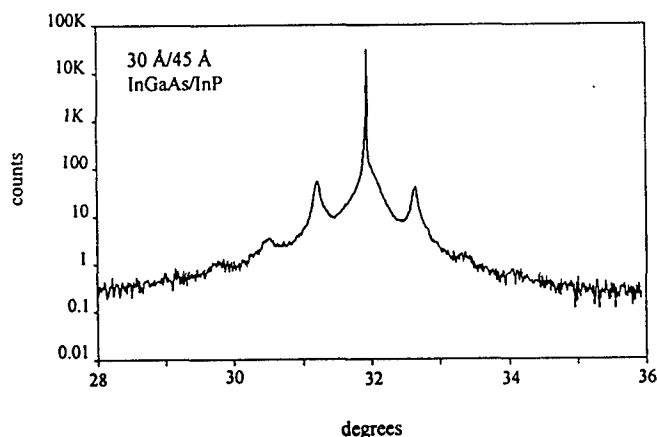
Figure 2 (a). X-ray diffraction plot of a 20 period $Ga_{0.47}In_{0.53}As$ superlattice with a period of 75 Å and well width of 30 Å.

Figure 2 (b) (200) dark field TEM image of a 20 period $Ga_{0.47}In_{0.53}As$ superlattice with a period of 80 Å and well width of 30 Å

in TEM images, Fig. 2 (b). Wavy interfaces have previously been observed in strained GaInAs/InP structures grown by MOCVD [13] at high temperature or low V-III ratio. It has also been observed in zero-net strain structures of quaternaries [14], where it was attributed to the tensily strained barrier layer growth. However, the period of the SL structures studied in both those cases were well above 85 Å. Since no compositional mixing was observed in our samples we conclude that the degradation of the crystalline of short period SLs is due to the intrinsic interface strain.

II. Experimental

The samples were grown using a compact MOMBE system [15] on exact (100)-InP:Fe substrates. Trimethylindium, triethylgallium, arsine and phosphine served as group III and V sources, respectively. The growth temperature was 500 °C, and the growth rate was about 1 monolayer/sec. A 0.2 μm buffer layer of InP preceded the SL structure and the capping layer was 500 Å. Growth interruptions between consecutive layers were of the order of 30 sec, to allow full stabilization of all gas flows. As described below, in spite of these relatively long growth interruptions no compositional intermixing was observed in the SLs. A summary of the samples grown is given in table 1.

The PL spectras were recorded at 77 K with a HeNe laser as excitation source, the PL was dispersed and focused onto a LN_2 cooled Ge-detector. HRXRD were obtained from the (004) reflection with the diffractometer scanning in the Θ–2Θ mode. The HRXRD spectra were compared to simulations based on the dynamical theory, (HRS program provided by Phillips). Furthermore, (110) cross-sectional dark field images were taken by TEM.

III. Analysis

The lack of compositional intermixing in our samples was verified by comparing HRXRD measurements to simulations. For example, the HRXRD rocking curve of a sample consisting of 10 periods of 490 Å $Ga_{0.47}In_{0.53}As$ / 45 Å InP layers is shown in Fig.3 The well resolved and intense satellite peaks indicate that the interfaces are smooth, and the zero order SL peak was not observed to be separated from the substrate peak within the resolution of the measurements. A simulation of the rocking curve assuming 3% As in the thin InP layer indicate clearly that the zero order SL peak should be resolved for such a barrier composition. Even two monolayers of As at the interface, simulated as a 3 Å thick InAs layer, should result in a well resolved zero order SL peak separated from the substrate peak. Concerning P incorporation into the $Ga_{0.47}In_{0.53}As$ wells, a percentage of less than 0.5% P had to be assumed in
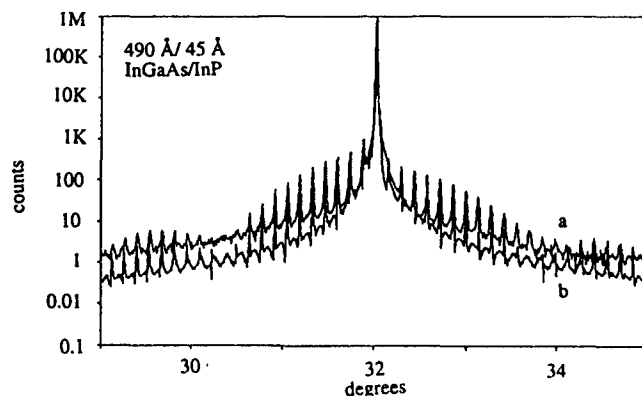
Figure 3 (a) X-ray diffraction plot of a 10 period $In_{0.53}Ga_{0.47}As$ superlattice with a period of 535 Å and well width of 490 Å. (b) Simulated x-ray diffraction plot of the same structure.

317

Table 1.

$Ga_{0.47}In_{0.53}As$ layer thickness (Å)	InP layer thickness (Å)	Total period (Å)	No. periods	Visibility of satellite peaks in HRXRD curves	PL FWHM (meV) (77 K)
560	60	620	10	+	23
55	66	121	20	+	17
29	59	88	20	+	23
30	38	68	20	-	double peak
30	45	75	20	-	37
30	55	85	20	+	24
55	40	95	20	+	21
490	45	535	10	+	20
60	300	360	10	+	6
30	100	130	15	+	13
60	600	660	20	+	13
103	31	136	10	+	22

order to fit the HRXRD simulations with our experimental rocking curves. The lack of compositional mixing in samples grown by MOMBE on exact (100)-oriented substrates, in spite of relatively long growth interruptions, was also reported in [11].

IV. Discussion

The physical origin of the observed degradation of crystalline quality in short period SLs is not easily understood. As listed in Table 1, thin layers of both InP and GaInAs of the order of 30 Å were successfully grown provided the next SL layers are thicker. This implies that the total strain of two close interfaces does not exceed some critical value. Furthermore, it is most likely that the strain of the top and bottom interfaces are almost exactly opposite in their direction and therefore compensate each other [1,4]. Thermodynamic considerations by Berger et al. [16] show that the minimum free-energy surface in a strained system is not atomically flat but has a three-dimensional form. We thus suggest that the alternating compressive and tensile strained interfaces induce some three dimensional growth, as evident in the TEM image of a SL having a period of 80 Å (Fig.2b). Fig. 2b reveals that the first interface of the short period SLs is flat but that already the second interface exhibits waviness, an effect that increases as the growth continues and more layers are added to the structure. The degradation is observed as a thickness modulation perpendicular to the growth direction, and the modulations are vertically arranged. For comparison a TEM image of a large period SL with abrupt interfaces is shown in Fig.1b. The thickness modulation of the interfaces due to three dimensional growth would induce a modulation in the interface related strain fields. When two strained interfaces are

close enough, the modulated strain fields can interact and the destort the crystal structure. Hence the distortion builds up as layer by layer are added to the structure. Interacting strain fields have been observed to be the driving force for vertically aligned self-organized InAs quantum dots on GaAs [17].

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DEMONSTRATION OF NITROGEN CARRIER GAS IN MOVPE FOR InP/InGaAs-BASED HIGH FREQUENCY AND OPTOELECTRONIC INTEGRATED DEVICES

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Introduction

InAlAs as a barrier or buffer material has many disadvantages compared to InP such as ageing, DX-centers, lack of etch control and need for surface passivation. Its use in high frequency devices is mainly historical: it is deposited by MBE, a technique which in the past was not well suited for P-based materials but well suited for obtaining homogeneous highly resistive (Al-containing) buffer layers as needed in HEMT-structures. The use of InP as the barrier layer for HEMT-structures requires highly resistive substrates and buffer layers, which are preferentially deposited by MOVPE. In this paper we will report on the suitability of 1) InP as the barrier material, 2) an innovative MOVPE process for its deposition and 3) the use of newly developed highly resistive InP wafers for high frequency and optoelectronic integrated devices. To enhance layer homogeneity, the structures were deposited in a conventional MOVPE system using nitrogen as the carrier gas.

I. Epitaxial Growth

Growth was carried out in a conventional horizontal reactor system (AIX 200) equiped with gas foil rotation at 670°C (thermocouple, effective temperature 640°C). The gas velocity was kept at 0.9 m/s and the reactor pressure at 20 mbar. The standard source chemicals TMGa, TMIn, 100% AsH_3 and PH_3 were carried to the reactor with nitrogen instead of the standardly employed hydrogen. The carrier gas N_2 was purified with a getter column (SAES Getters). Newly developed (001) exactly oriented semi-insulating InP wafers (InPact) were used. To assess the device quality of the wafers 3 µm thick InP buffer layers were deposited. The layers exhibit an electron mobility of 4,500 and 98,000 cm^2/Vs and an electron concentration of 2.4 and 1.9 * $10^{14} cm^{-3}$ at 300 and 77 K, respectively. The resistivity of substrates as well as InP buffer layers are adequate for Al-free HEMT application. The suitability of nitrogen carrier gas for the deposition of device quality layers is best demonstrated by the electrical quality as well as the layer homogeneity of the ternary compound $In_{0.53}Ga_{0.47}As$ used in the structures. 2µm thick layers exhibit a room temperature mobility of 10,600 cm^2/Vs at a carrier concentration of 1.5 * 10^{15} cm^{-3}. The standard deviation of the InGaAs layer thickness for 95 % of the 2" wafer is below 2.5 % when nitrogen carrier gas is used in comparison to only 35 % wafer surface for hydrogen carrier gas at the same standard deviation [1].

II. Device fabrication

The MOVPE system described above was used to grow layer structures for HEMTs and for MSM diodes above a modified HEMT layer system. A distributed amplifier was realized with RF-optimized HEMTs. The modified HEMT layer structure was used for optoelectronic integrated circuits (OEIC) which consist of an MSM photodetector and a HEMT based on the same layer system.

In all the layer structures the conventionally used high bandgap material InAlAs was replaced by InP. Because of the low Schottky barrier height of InP high performance of our

devices is only possible by using a Zn doped p-InP layer for barrier enhancement [2].

Fabrication of the devices consisted of standard optical lithography, metal evaporation and lift-off. The mesa to insulate the devices was performed by RIE (Reactive Ion Etching) with subsequent wet etching using a citric acid based solution. Sub-μm structures were defined by electron beam lithography. A chromium/gold metallization was used to fabricate the contact pads.

III. Properties of InP/InGaAs-based devices and integrated circuits

A. The InP/InGaAs HEMT

The layer system of the aluminum-free HEMT corresponds to a conventional InAlAs/InGaAs/InP-HEMT where the InAlAs has been replaced by InP. The 2DEG channel consists of an 8 nm thick strained $In_{0.8}Ga_{0.2}As$ layer with a 7 nm thick lattice-matched InGaAs subchannel. Diffusion of the acceptor atoms from the p-doped InP barrier enhancement layer into the carrier supply layer is suppressed by an intrinsic InP layer. A typical layer structure is shown in Fig. 1.

20nm n-InGaAs 2E18cm-3	cap layer
15nm p-InP 2E18cm-3	barrier
15nm InP	enhancement layers
5nm n-InP 7.6E18cm-3	carrier supply
6nm InP	spacer
8nm In(x) Ga(1-x)As	channel, x=80%
7nm InGaAs	subchannel
300nm InP	buffer
semi-insulating InP substate	

Fig. 1. Layer sequence of an Al-free InP/InGaAs HEMT

The gate contact fingers were carried out as T-gate using electron beam lithography and a three layer resist system. HEMTs were realized with gate lengths down to 100 nm [3], with a cutoff frequency of 160 GHz (Fig. 2). The best f_{max} value of 300 GHz was obtained at a gate

length of 200 nm. These frequency values correspond to results published for conventional Al-containing devices. Noise measurements give a minimum noise figure F_{min} below 1 dB at 10 GHz and below 2 dB at 20 GHz, which are acceptable values. The low frequency noise was about 10 dB below commercial AlGaAs/GaAs HEMTs. We attribute the better low frequency noise behavior to the lack of traps in the Al-free device.
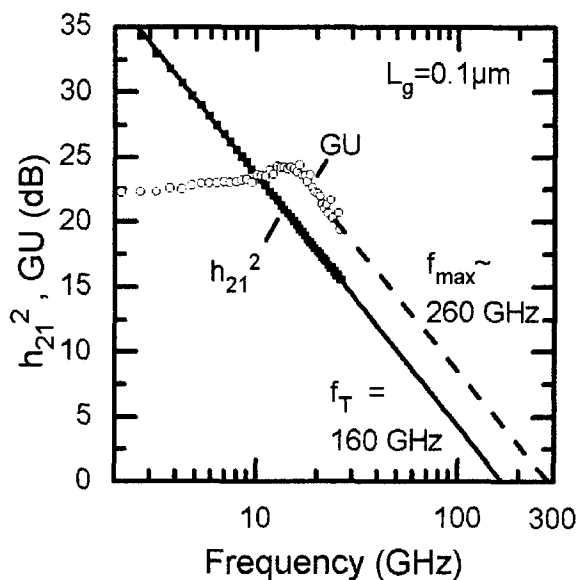
Fig. 2 Current gain and unilateral gain of an InP/InGaAs HEMT with 100 nm gate length

B. Integrated travelling wave amplifier

The possibility to integrate the Al-free InP/InGaAs HEMT into a complex circuit was demonstrated with the development of a monolithically integrated travelling wave amplifier (TWA). The TWA consists of three or more transistors that are interconnected by inductances and resistances. This circuit allows a constant amplification over a broad frequency range. The TWA was realized using the Al-free HEMT layer structure on semi-insulating substrate. Coplanar technology was used for the circuit layout. The required inductances were performed as coplanar lines. The resistances were fabricated with 10 to 50 nm thin Platinum films. An air bridge technology was developed for the interconnections of the different ground regions. Fig. 3 shows a viewgraph of a three-

321

stage TWA. First results using HEMTs with a gate length of 300 nm gave a bandwidth of 20 GHz and an amplification of 8 +/-1.5 dB. The behavior of the amplifier will be improved by using more transistor stages, 100 nm T-gate HEMTs and an optimized circuit design.
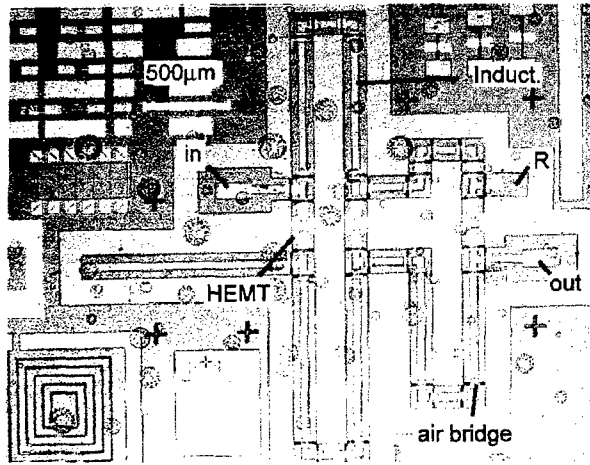
Fig. 3: Layout of a three-stage travelling wave amplifier in coplanar technology

C. MSM-2DEG photodetector

The MSM diode needs simpler fabrication processes than a pin device and has a much lower capacitance per area. Therefore it is very well suited for fast photodetector application. A disadvantage of a conventional MSM detector compared to the pin device is the shadowing of part of the active area by the Schottky contacts, which reduces the responsivity. Using transparent or semitransparent Schottky contacts to increase the responsivity leads to photogeneration of carriers below the Schottky contact in the region of low electric field. This would reduce the bandwidth of the photodetector [4]. The problem can be overcome by introducing a two dimensional electron gas (2DEG) into the layer system. The 2DEG acts as an equipotential plane and increases the electric field below the Schottky contacts [5]. The layer system of such an MSM-2DEG diode corresponds to an inverted HEMT structure, with an InGaAs absorption layer between the surface layer and the channel. Fig. 4 depicts a typical layer system of an Al-free InP/InGaAs MSM-2DEG photodetector for 1.3 and 1.55 µm wavelength light.

Layer	Description
15nm p-InP 1.5E18cm-3	barrier
15nm InP	enhancement layers
125..500nm InGaAs	absorption layer
10nm In(x) Ga(1-x)As	channel, x=77%
5nm InP	spacer
7nm n-InP 2E18cm-3	carrier supply
300nm InP	buffer
semi-insulating InP substate	

Fig. 4: Layer sequence of the MSM-2DEG photodetector

The thickness of the absorption region determines the responsivity and bandwidth of the devices. A thick absorption layer leads to a high responsivity. Reducing this layer decreases the responsivity, but gives a higher bandwidth. Fig. 5 depicts the influence of the absorption layer thickness on responsivity and bandwidth of MSM-2DEG devices with 0.5 µm finger width and spacing.
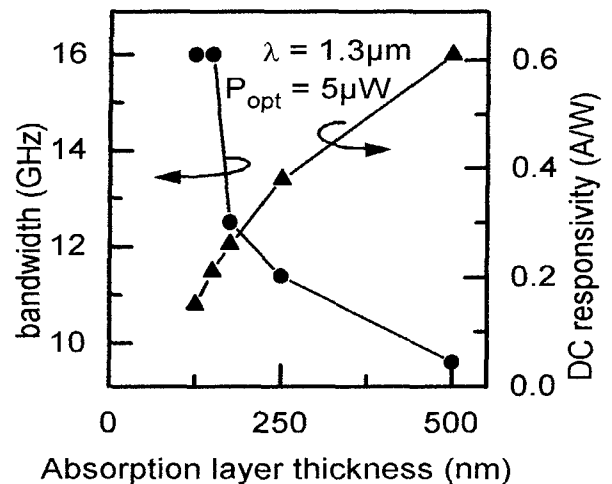
Fig. 5: Dependence of responsivity and bandwidth of an MSM-2DEG photodetector with semitransparent contacts on the absorption layer thickness (finger width and spacing of the electrodes: 0.5 µm)

A device with a 500 nm thick absorption layer had a responsivity of 0.61 A/W and a bandwidth of 9.6 GHz. An RF- optimized device

with 150 nm absorption layer showed a bandwidth of 16 GHz and a responsivity of 0.21 A/W. These are, to the authors' knowledge, best values for MSM devices at 1.3 μm wavelength.

D. Optoelectronic integrated receiver

As mentioned above the MSM-2DEG layer system consists of an inverted HEMT layer structure. Therefore the MSM-2DEG concept allows the integration of photodetector and a HEMT-based amplifier circuit by using the same layer system for detector and transistor.

The monolithic integration reduces the parasitics and noise contributions of the interconnections, compared to hybrid systems. Moreover the fabrication of an integrated circuit is cheaper than for a hybrid one. The need of only one epitaxial step reduces the effort compared to other integration concepts [6].

The HEMT properties and the detector performance depend on the absorption layer thickness of the MSM-2DEG layer system. A thick absorption layer gives a high photodetector responsivity, but at the cost of a reduced RF performance of both detector and transistor. Therefore a compromise must be found. Best results were obtained using a layer system with 150 nm absorption layer thickness. The corresponding photodetector had a responsivity of 0.21 A/W and a bandwidth of 16 GHz, the HEMT with 0.36 μm gate length showed an f_T of 45 GHz and an f_{max} of 85 GHz. A simple frontend receiver with inductive peaking was realized with this layer system. Fig. 6 shows the circuit and the frequency response of the receiver. A responsivity of 2A/W and a bandwidth of 7 GHz were measured on an optoelectronic integrated circuit with 0.5 μm gate length and 0.5 μm width and spacing of the MSM fingers. The results measured allow operation in future 10 Gbit/s communication systems.

IV. Conclusions

The presented results demonstrate that 1) the newly developed InP substrates meet the need for high frequency devices. 2) The innovative growth MOVPE process using N_2 instead of H_2 carrier gas is suitable for the deposition of devices with excellent characteristics. 3) by substituting InAlAs for InP, state of the art devices are obtained without the disadvantages observed for Al-containing materials. 4) Identical layer structures for detector and transistor fabrication together with the above results allow simple and cost-effective optoelectronic integrated circuit fabrication.
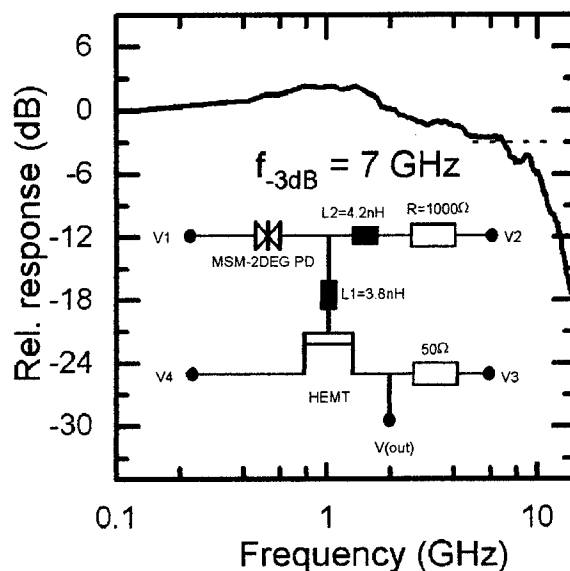
Fig. 6: Circuit diagram and frequency response of an MSM-2DEG based frontend receiver

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Study of $Ga_xIn_{1-x}P$ layers grown on InP for HFET application

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ABSTRACT

The crystalline quality of tensile strained $Ga_{0.25}In_{0.75}P$ layers grown on InP substrates was investigated. Samples were grown by metal-organic molecular beam epitaxy. Little or no relaxation was found in $Ga_{0.25}In_{0.75}P$ layers which were up 500Å thick. Thicker layers exhibited anisotropic strain relaxation, and the main relaxation direction was [$1\bar{1}0$]. Using strain compensation we were able to reduce relaxation in 650Å thick layers. HFET devices with a tensile 200Å thick $Ga_{0.25}In_{0.75}P$ barrier, a composite channel, and modulated channel doping were fabricated. The HFETs with 1 micron long gates exhibited a transconductance higher than 150 mS/mm for a wide range of gate voltages, and a breakdown voltage of 9V.

I. Introduction

Tensely strained $Ga_xIn_{1-x}P$ is an excellent candidate for replacing Al containing barrier layers in InP based heterostructure field effect transistors (HFETs) [1,2]. GaInP exhibits a large Schottky barrier to the gate metal and a large conduction band discontinuity to InP and GaInAs. Additional advantages of GaInP are a simple gate recess process, and a large valence band discontinuity to GaInAs. The Ga content of such layers is typically x~0.2 to 0.25, leading to a theoretical critical layer thickness of 55-40Å respectively [3]. However, in most HFET structures the layer thickness exceeds the critical thickness and is about 200Å.

In this publication we report on the growth of $Ga_{0.25}In_{0.75}P$ layers on InP by metal-organic molecular beam epitaxy (MOMBE). The thickness of the grown layers was varied in the range of 200Å to 1500Å. In order to measure the relaxation rate of the layers symmetric and asymmetric high resolution x-ray diffraction measurements were carried out. Schottky diodes were fabricated on the layers and their reverse leakage current was measured. HFETs having a tensile $Ga_{0.25}In_{0.75}P$ barrier and a channel composed of a lattice matched $Ga_{0.47}In_{0.53}As$ and compressive strained $Ga_{0.3}In_{0.7}As$ were fabricated and tested.

II. Growth and characterization

The layers were grown by a compact MOMBE system [4] on (001) oriented InP substrates. Trimethylindium, triethylgallium, arsine and phosphine served as group III and V sources, respectively. The growth temperature was 510°C. GaInP layers of thickness ranging from 200Å to 1500Å were grown on top of a 1000A thick InP buffer layer. The thickness of the layers was extracted from the rocking curve fringes spacing, and was found to be linearly proportional to the growth time. For the thicker (relaxed) samples where fringes were not resolved the thickness was calculated by the growth time.

X-ray diffraction experiments were carried out by a Philips high resolution diffractometer. A Bartels monocromator in a four crystal (Ge 220) setup was used with the beam limited by a 1 mm^2 slit at the exit of the monocromator. The x-ray spectra were compared to simulations based on the dynamical theory (HRS program provided by Phillips). The in-plane strain relaxation percentage of the layers was measured by obtaining the lattice constant perpendicular and parallel to the interface plane from asymmetric 115 reflections [5]. The in-plane strain relaxation was measured in the 110 and in the $1\bar{1}0$ directions separately in order to investigate strain relaxation anisotropy.

III. Results and discussion

The measured and simulated symmetric 004 x-ray reflections of the GaInP layers grown on InP are shown in Fig. 1. Up to a layer thickness of 500Å the interference fringes were well resolved, pointing already to little or no structural relaxation. Moreover, the peak width corresponded well to the simulations, and the layers looked smooth under a Nomarski interference microscope. Layers thicker than 500Å exhibited cross hatched dislocation lines, and their x-ray reflection curves indicated a degradation of their crystalline quality.

Strain compensated layers were grown as well. The symmetric 002 reflections of GaInP layers grown on top of a compressive strained 100Å thick $Ga_{0.3}In_{0.7}As$ layer are shown in Fig. 2. Up to a layer thickness of 650Å little or no structural relaxation is observed. When viewed by a Nomarski microscope the 600Å and the 650Å thick layers showed, however, some faint cross hatch patterns.

The in-plane relaxation percentage of the layers grown directly on InP is plotted versus layer thickness in Fig. 3. Negligible relaxation (0% to 3%) was found in all layers of
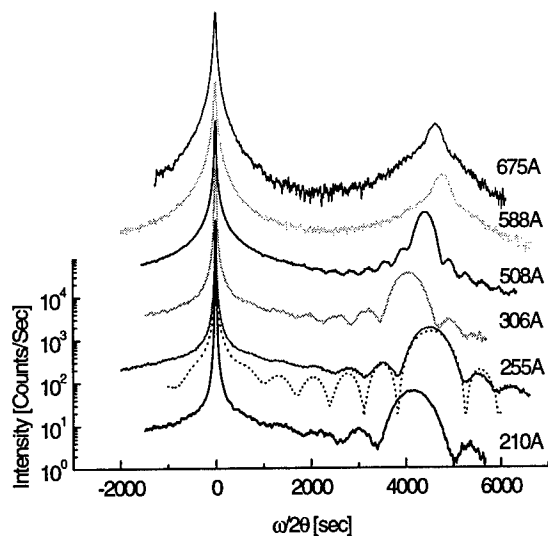
Fig. 1. Measured 004 reflections for $Ga_{0.25}In_{0.75}P$ layers of different thicknesses grown on InP. A calculated curve (dotted line) is also shown for the 255Å layer.
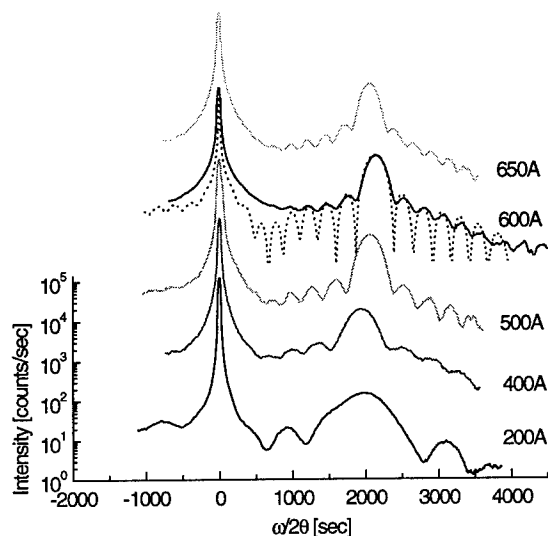

Fig. 2. Measured 002 reflections for $Ga_{0.25}In_{0.75}P$ layers of different thicknesses grown on top of a 100Å thick $Ga_{0.3}In_{0.7}As$ layer. A calculated curve (dotted line) is also shown for the 600Å layer.

thickness less than 500Å. For thicker layers larger values of in-plane relaxation were measured. The 1,500 Å thick layer exhibited anisotropic relaxation. The major relaxation axis was found to be along the [1$\bar{1}$0] direction, whereas relaxation along the [110] direction was smaller. No anisotropy was detected in the layers with a thickness less than 580Å.

Anisotropic strain relaxation was first observed in tensile and in compressivley strained $Ga_xIn_{1-x}P$ (x=0.59 and x=0.45) grown on GaAs [6]. The major relaxation axis was in the

[1$\bar{1}$0] direction regardless of the sign of the strain. The investigated layer thickness was in the range of 1700Å to 7000Å. Our results thus indicate that anisotropic relaxation develops mainly in bulk material in a manner consistent with the results reported in [6], whereas the interface dictates isotropic strain relaxation in thin layers.

We finally note that inspection of Fig. 1 reveals an asymmetric widening of the thick (relaxed) layer peak towards the substrate peak indicating composition grading. The composition grading may be a result of Ga atom segregation towards the growing surface [7]. The segregation process is an additional mechanism that can reduce the strain in the growing layer.
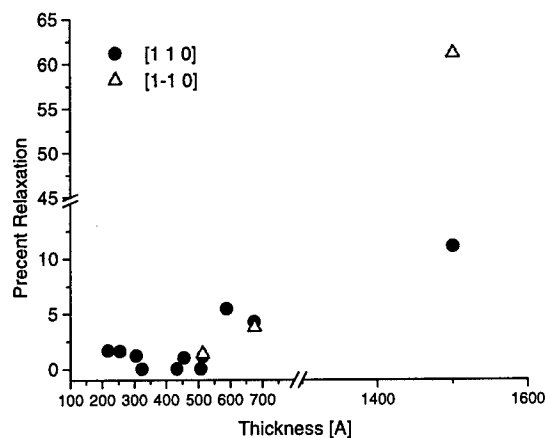
Fig 3. Percent relaxation as a function of the layer thickness in the two <110> directions. The onset thickness for relaxation is between 500Å to 580Å.

IV. Schottky diodes

Schottky Pt/Ti/Pt/Au diodes were fabricated on the GaInP layers. This method was found elsewhere to be very sensitive to the existence of dislocations in the layer [2]. In our experiments, however, low reverse leakage current of the order of $J_r=2·10^{-5}A/cm^2$ were obtained for all the layers. It thus seems that passivation of the dislocation related defects during the microfabrication process may lead to erroneous conclusions on the crystalline quality of the layers.

V. HFET fabrication and characterization

The HFET layer structure is outlined in Fig. 4. The 100Å thick compressively strained $Ga_{0.3}In_{0.7}As$ channel provided strain compensation to the tensile strained InGaP barrier. Indium rich channels also provide better electron confinement and exhibit higher electron mobility [8]. The InGaP barrier was grown undoped to improve the Schottky contact properties. Electrons were provided to the strained channel from a Sn doped lattice matched GaInAs layer grown underneath a setback layer. The x-ray 004 reflection

325

source		drain
n-GaInAs 4x10^18	gate	300A
i-Ga$_{0.25}$In$_{0.75}$P	undoped	200A
i-Ga$_{0.3}$In$_{0.7}$As	undoped	100A
i-Ga$_{0.47}$In$_{0.53}$As	undoped	100A
n-Ga$_{0.47}$In$_{0.53}$As 1x10^18		100A
i-InP buffer	undoped	1000A
S. I. InP substrate		

Fig.4. Schematic diagram of the HFET layer structure.
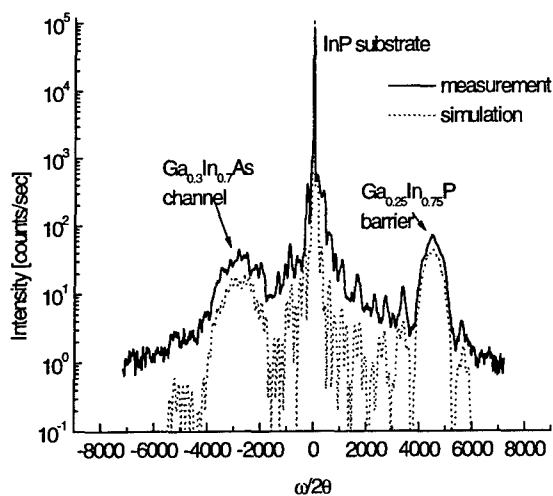
Fig 5. A measured 004 reflection of a HFET structure. Note the Ga$_{0.25}$In$_{0.75}$P layer peak (right to the InP substrate peak) and the Ga$_{0.3}$In$_{0.7}$As peak (left peak). The dotted line shows a calculated curve (The curve is shifted down for clarity)

rocking curve of the HFET layers is shown in Fig. 5. Note the presence of the separate tensile (barrier) and compressive (channel) peaks.

The HFETs were fabricated by standard lithography and wet etch technology. The gate length and width was 1μm and 50μm respectively. Source and drain ohmic Ni-Ge-Aucontacts were evaporated and then alloyed for 30 sec at 400°C. The device current-voltage characteristic is shown in figure 6, and the transconductance as a function of the source gate voltage is plotted in Fig 7. The breakdown voltage was found to be approximately 9V.

VI. Conclusion

We have studied the crystalline quality of Ga$_{0.25}$In$_{0.75}$P layers grown on InP by MOMBE. Although the theoretical critical thickness of the layers was 55Å, little or no relaxation was found in layers which were up to 500Å thick. Thicker layers exhibited anisotropic strain relaxation, and the main relaxation direction was [1$\bar{1}$0]. Using strain compensation we were able to reduce relaxation in 650Å thick layers. HFET devices with a tensile 200Å thick Ga$_{0.25}$In$_{0.75}$P barrier, a composite channel, and a modulated channel doping were fabricated. The HFETs exhibited a transconductance higher than 150 mS/mm for a wide range of gate voltages, and a breakdown voltage of 9V.
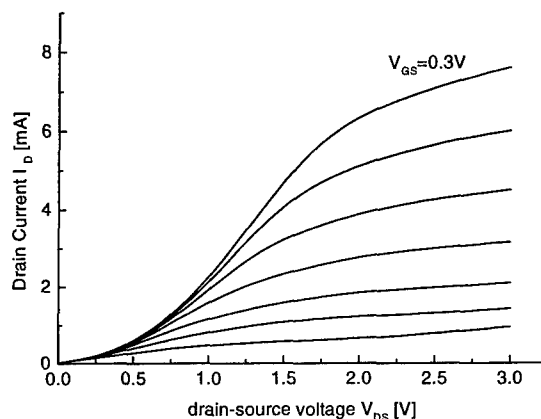
Fig 6. Current voltage output characteristics of a 1×50μm² HFET. The V$_{GS}$ step is -0.2V.
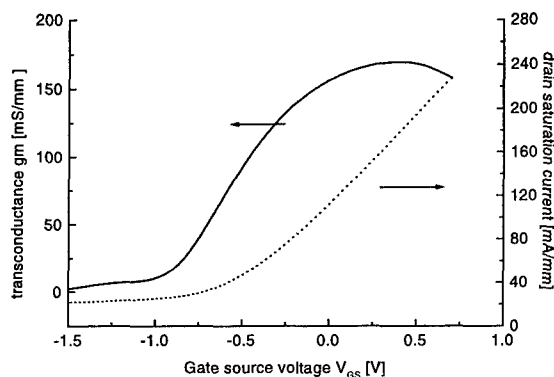
Fig 7. Influence of the gate-source V$_{GS}$ voltage on the drain saturation current I$_{DS}$ and the transconductance g$_m$.

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GROWTH OF HIGH-QUALITY InGaP ON GaAs BY GAS-SOURCE MOLECULAR BEAM EPITAXY USING TERTIARYBUTYLPHOSPHINE

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Introduction

$In_{0.48}Ga_{0.52}P$ lattice matched to GaAs are becoming increasingly important as a material for photonic and electronic devices. Gas-source molecular beam epitaxial growth (GSMBE) using tertiarybutylphosphine (TBP) is attractive growth method of InGaP combining monolayer level growth control capability of MBE with low toxic nature of TBP. However, electronic and optical properties of InGaP epitaxial layers grown by GSMBE using TBP have so far been inferior to those by GSMBE using PH_3, and those by MOCVD, and sometimes results in highly compensated undoped high-resistive layers[1].

The purpose of this paper is to demonstrate that $In_{0.48}Ga_{0.52}P$ layers having the electronic and optical properties comparable to the best data reported for MOCVD[2] can be grown by GSMBE using TBP, if the growth conditions are systematically optimized. Optimization of the growth conditions were made based on the RHEED observations. The 77K photoluminescence (PL) spectrum of $In_{0.48}Ga_{0.52}P$ layers was dominated by a peak due to a InGaP band-edge emission at 1.96eV with a narrow line width (FWHM) of 15.5meV. The undoped InGaP layers grown under the optimum growth condition showed high electron mobility values and low carrier concentrations. The highest electron mobility at 300K was 3300cm^2/V·s and that at 77K was 21000cm^2/V·s at the carrier concentration value of n=5x10^{14}-1x10^{15}cm^{-3}. These data are compared with the best values reported so far for various growth methods.

I. Experimental

All the growth was made using EIKO EVC500 GSMBE system with a modified high-pressure cracker cell and a 2800l/s diffusion pump . Metallic Ga, In, As and TBP were used as source materials. 100% TBP was decomposed in a thermal cracker cell (800-900°C) containing a molybdenum baffler and a catalytic tantalum to improve the cracking efficiency[1]. Usually, cracking temperature of 800°C was used unless otherwise noted. The substrate temperature was monitored using an pyrometer which was calibrated by the InSb melting point (525°C). After the growth of a GaAs buffer layer with thickness of about 100nm at 580°C, undoped InGaP layers with thickness between 0.9 and 1.3μm were grown within a substrate temperature range from 450 to 640°C. Growth rates of InGaP layers were varied from 0.4 to 0.9ML/s with TBP flow rates being within the range from 0.5-4sccm. RHEED observations were made to investigate the growth rate and to monitor the growth modes. The qualities of the InGaP layers were characterized by Hall effect, PL, double-crystal X-ray diffraction (XRD) measurements.

II. Results and discussion
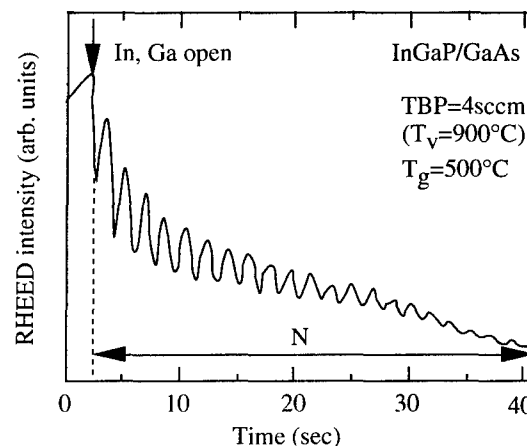
A. RHEED studies of InGaP growth

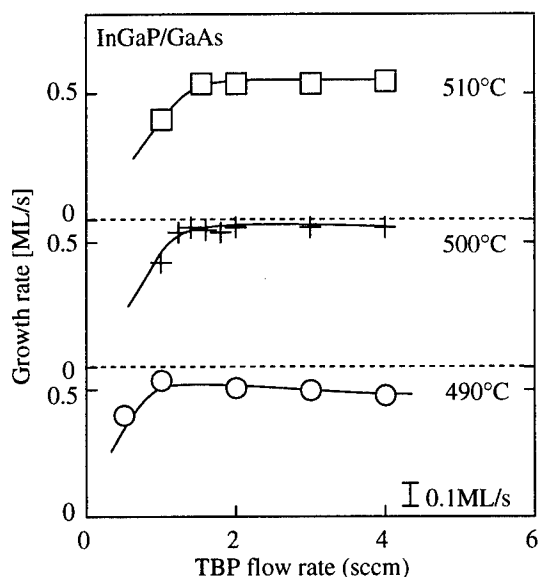Fig. 1. Typical RHEED oscillation in InGaP growth on (2x4) -GaAs surface.

Fig. 2. TBP flow rate dependence of growth rates of InGaP at various substrate temperatures.

Fig. 3. Dependence of number of RHEED oscillation cycles on growth temperature.

When InGaP was grown on As-stabilized (2x4)-GaAs surfaces, clear and persistent RHEED oscillations were observed as shown in Fig. 1, indicating realization of a stable layer-by-layer growth mode. On the other hand, growth on As-rich (2x1) surfaces resulted in growth without RHEED oscillations. Therefore, all the InGaP growth made in this study were performed on the (2x4)-GaAs surface. To preserve the (2x4)-GaAs surface at low temperature the following sequence was performed. After growth of GaAs buffer layers growth interruption of about 3 minutes was employed to set the substrate temperature to 450-640°C for the InGaP growth. It was then necessary to stop the As_4 supply below 510°C to maintain the (2x4)-GaAs surface. Then, growth of InGaP layers were started a few second after the start of P_2 supply.

During the growth of InGaP above 500°C, (2x1) and (4x2) RHEED pattern were observed at the TBP flow rate above and below 1sccm, respectively. On the other hand, in the growth below 490°C, poor resolved (2x4) or (2x1) RHEED patterns appeared within the entire TBP flow rate range from 0.5 to 4sccm.

TBP flow rate dependence of the growth rate of InGaP at various substrate temperatures obtained by measuring RHEED oscillation frequency were shown in Fig. 2. Clear RHEED oscillations were observed within the entire TBP flow rate range. As seen in Fig. 2, Growth rates were constant above the TBP flow rate of 1sccm. However, it decreased below around 1sccm.

The overall tendency of TBP flow rate dependence of growth rate can be explained in the same way as in the case of InP growth with PH_3 reported by Chin et al. and by Yang et al.[3],[4] Namely, the constant growth rate region at high

TBP flow rates corresponds to the group-III-limited growth region, and the lower growth rate region at low TBP flow rate, to the P-limited-growth region, respectively. Then, the intersection between these two region occurs when the effective supply of group III and V sources are the same. In the present case, unity ratio is realized at 1, 1.3 and 1.5sccm at the substrate temperature of 490, 500 and 510°C, respectively. Temperature dependence of the position of the intersections seen in Fig. 2 may be due to the fact that the lifetime of P adatom on the surface also depends on the substrate temperature.

Figure 3 shows the substrate temperature dependence of the number of RHEED oscillation cycles taken during the growth of InGaP under TBP flow rate of 4sccm. The number of oscillations was found to be strongly dependent on the growth temperature and took a broad maximum within a substrate temperature range of 480-510°C. Particularly, extremely smooth surfaces were obtained at 470-490°C. At high temperatures (>550°C), the oscillation number drastically decreased as shown in Fig. 3. In addition to this, metal-stabilized (4x2) RHEED pattern was observed in this temperature range and the growth usually resulted in rough surfaces.

Figure 4 shows the TBP flow rate dependence of number of RHEED oscillation cycle taken during InGaP growth. The TBP flow rates realizing unity V/III ratio obtained from Fig. 2 are indicated by arrows in Fig. 4. As seen in Fig. 4, the number of RHEED oscillations was found to saturate at TBP flow rates above 2sccm at 490°C. On the other hand, in the growth temperature above 500°C, number of RHEED oscillations does not saturate below at least up to TBP flow rate of 4sccm and the resultant InGaP surfaces were usually rough. It was found that, in the range of substrate temperature that gave smooth InGaP surfaces,
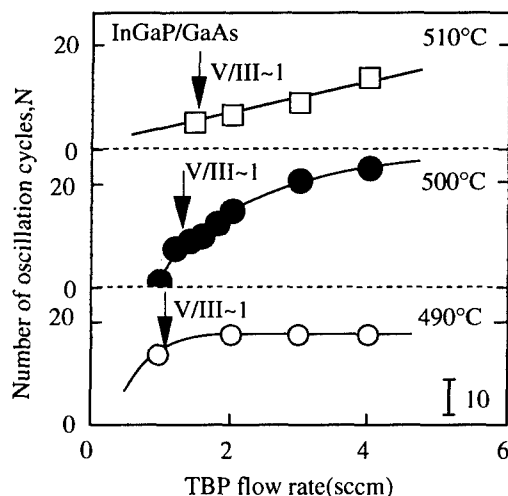
Fig. 4. TBP flow rate dependence of number of RHEED oscillation cycles at various substrate temperature.

saturation of observable RHEED oscillation numbers with respect to TBP flow rates always took place.

In terms of the V/III ratio, the V/III ratio should be larger than 2 for stable two dimensional growth of InGaP at 490°C according to Fig. 4. Here, in this paper, V/III ratios are defined as a TBP flow rates normalized by those at the intersections, following the manner reported by Chin et al. and by Yang et al.[3],[4] However, at 500°C, V/III ratio of 3 obtained at the TBP flow rate of 4sccm was still not enough for realization of stable two dimensional growth mode although the growth rate seems to saturate at higher V/III ratio. Actually, by increasing the cracking temperature to 900°C to increase the cracking efficiency, the number of RHEED oscillation was found to saturate and a smooth surface was obtained at 500°C at TBP flow rate of 4sccm (V/III=5.2).

B. Electrical and optical properties of InGaP layers

Figure 5 summarizes PL spectra of the InGaP layers grown at various substrate temperatures taken at 77K. In this case, the TBP flow rate and the cracking temperature were fixed at 4sccm and 800°C, respectively. All the PL spectra of the samples grown below 485°C have two peaks around 1.91 and 1.96eV, respectively. The peaks around 1.96eV can be assigned as the InGaP band-edge emissions. The side peaks at 1.91eV are due to donor-acceptor(D-A) pair emissions as reported by Su et al.[5] The peak due to the InGaP band-edge emission became strong and narrow with increasing growth temperature up to 485°C, whereas the side peak became dominant at low growth temperatures. On the other hand, only a weak and broad peak was observed in the case of InGaP layer grown at 500°C. Room temperature PL spectra of the sample grown at 485°C has a peak at 1.89eV which is consistent with the data obtained

for $In_{0.48}Ga_{0.52}P$ layer with no ordering grown by MOMBE using TBP.[6] Figure 6 summarizes substrate temperature dependence of the FWHM values of the PL peaks at 77K and those of XRD peaks observed in the InGaP layers. Both values were found to be correlated with each other and strongly dependent on substrate temperature. Both took minimums values of 15.5 meV and 18s, respectively at T_g=485°C. Namely, the highest uniformity of the epitaxial layer giving the narrowest PL and XRD peaks can be realized by the growth at 485°C. These FWHM values are

Fig.5. PL sectra of InGaP layers grown at various substrate temperattures.

Fig. 6. Substrate temperature dependences of FWHM of PL at 77K and XRD.

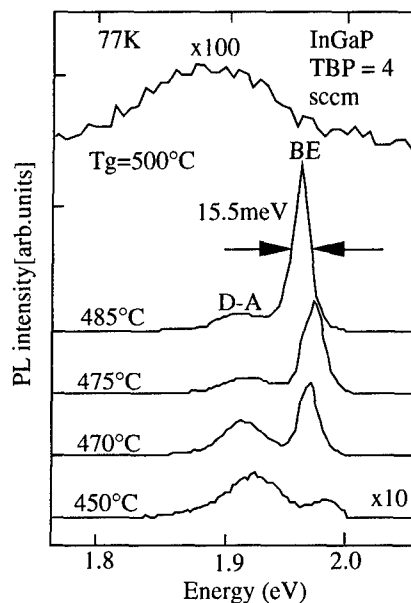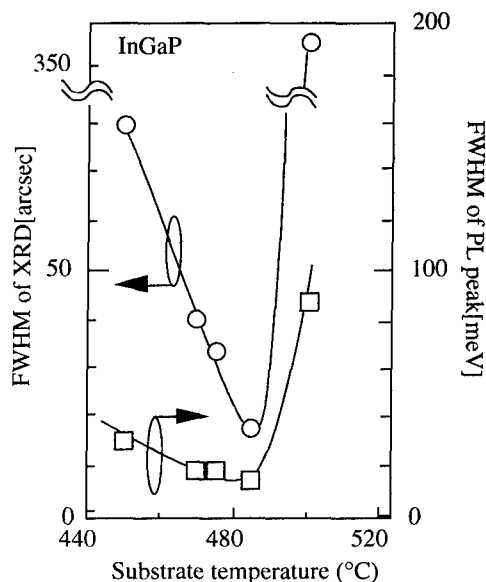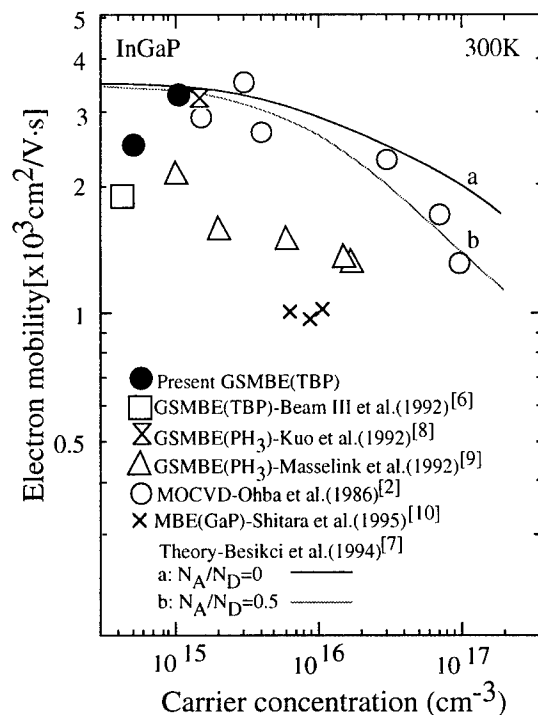Fig. 7. Relationship between electron mobilities and carrier concentration for InGaP at 300K.

good optical properties as shown in Fig. 5, its electrical properties was rather poor compared with the sample grown at 485°C. This means that careful optimization of the growth condition is necessary to realize an InGaP layer with both of good electrical and optical properties. More specifically, high growth temperature and high V/III ratio seems to be two key factors for growing high quality InGaP layers. The poor quality of InGaP layer grown at high growth temperature may be due to the defects created by P vacancy. On the other hand, the poor quality of the sample grown at low temperature may be attributed to the defect related to excess phosphorus as in the care of GSMBE growth of InP using PH_3.[4]

III. Conclusions

A systematic study on the growth mode and properties of InGaP layers grown by GSMBE using TBP at various growth conditions were made. High growth temperature and high V/III ratio are found to be essentially important for realizing high quality InGaP layers.

The InGaP layer grown under the optimum growth condition showed a intense band-edge emission at 1.96eV with narrow FWHM of 15.5meV, as well as, the high electron mobilities of 3300 and 21000cm^2/V·s at 300 and 77K, respectively, with low carrier concentrations. These data are not only the best of TBP-based MBE but also among the best data obtained by various growth methods.[2],[6],[8],[9],[10]

comparable to the best values reported for InGaP layers grown by other methods, and are narrowest of all the reported values for InGaP layers grown by GSMBE using TBP.

The relationship between the carrier concentration and Hall mobility of the undoped InGaP epitaxial layers measured at 300K are shown in Fig. 7 together with the best values reported so far for various growth methods. Theoretically expected μ-n relationship for two compensation ratios of N_A/N_D=0 and 0.5[7] are also plotted in Fig. 7. Growth below 475°C usually led to highly resistive InGaP layers. The undoped InGaP layers grown at 485°C showed high electron mobility values of 2500cm^2/V·s and a low carrier concentrations of n=$5 \times 10^{14}cm^{-3}$ at 300K. In addition, the highest electron mobility of 3300cm^2/V·s at 300K and that of 21000cm^2/V·s at 77K at the low carrier concentration value of 5×10^{14}-$1 \times 10^{15}cm^{-3}$ were achieved in the InGaP layer grown at 500°C under the high V/III ratio of 5.2 realized by high cracking temperature of 900°C.

As seen in Fig. 7, the data obtained in the present work is not only the best of TBP-based MBE but also among the best data obtained by various growth methods.[2],[6],[8],[9],[10] In addition, this data point lies on the theoretical μ-n curve[7].

As for the growth at cracking temperature of 800°C, the best optical and electrical properties were realized at the same substrate temperature of 485°C. However, although the InGaP layer grown at 475°C showed relatively

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Optical and Structural Characterization of InAsP/InGaP Strain Compensated Multiple Quantum Wells Grown by GSMBE

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Introduction

For optoelectronic applications in the 0.9-1.5 μm range, the ternary $InAs_xP_{1-x}/InP$ material system grown by GSMBE has a number of advantages over GaInAsP/InP, including independent control of InAsP thickness (determined by In flux) and composition (determined by AsH_3/PH_3 ratio), as well as reduced alloy scattering[1]. In addition, this material system has a larger conduction band offset ratio than GaInAsP/InP which can reduce the hot electron overflow and improve the temperature characteristics of a laser diode[1,2]. Thus, InAsP has great potential for replacing GaInAsP in opto-electronic devices such as lasers and modulators[1,3]. A primary disadvantage of InAsP materials, however, is that their high compressive strain makes it difficult to grow thick layers on InP. To solve this problem, tensile-strained GaInAsP and GaInP has been used as strain-compensating barrier materials so that net strain can be reduced and a stable structure with an increasing number of periods can be achieved.[3-5] Some results have shown that this use of strain-compensated MQWs (SC-MQWs) can indeed improve crystal quality and device performance, but more recent investigations have also shown that crystal quality may degrade when a strain compensated barrier is used instead of a lattice-matched barrier[6,7]. Unfortunately, few in-depth investigations on strain compensation mechanisms have been made. Thus, controversy exists regarding the actual effectiveness of SC-MQW.

Patriarche *et al.* demonstrated by using XTEM that the insertion of thin layer of InP at the interfaces between the highly strained layers of a SC-MQW may prevent the catastrophic morphological degration of the epitaxial structure as growth procedes[8]. They showed that the InP insertion layer restores the planarity of lateral thickness undulations, thus yielding high overall crystal quality. In this paper, we report the characterization of $InAs_{0.5}P_{0.5}/In_{0.8}Ga_{0.2}P$ SC-MQW structures with an emission wavelength ~1.3 μm. In particular, the importance of the InP insertion layer is studied by the growth of a series of $InAs_{0.5}P_{0.5}/InP/In_{0.8}Ga_{0.2}P$ SC-MQW structures with the thickness of InP insertion layer varied from 0 to 3 ML. SC-MQW samples with and without InP insertion layer were evaluated by cross-sectional TEM analysis (XTEM), x-ray rocking curves and dynamical simulations, and photoluminescence (PL) measurements. All of these characterizations show greatly improved crystal quality of SC-MQW with a 3ML InP
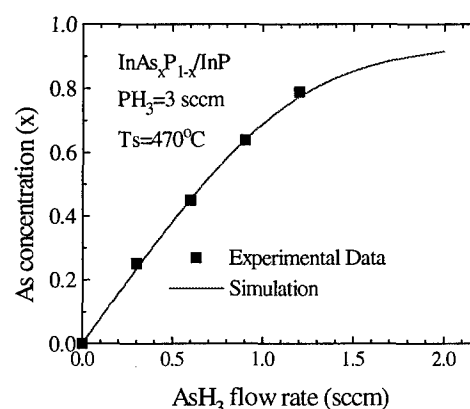

Fig. 1 Experimental and simulated arsenic solid composition as a function of AsH_3 flow rate.

insertion layer at the interfaces between the highly strained layers of the structures.

Experimental Details

Epitaxial growth was performed in a modified Perkin-Elmer 430P GSMBE/CBE system. The growth chamber was equipped with a 5000 l/s cryopump and a 2200 l/s turbomolecular pump. Cracked AsH_3 and PH_3 (100%) were used as the group V sources, while elemental solid sources in effusion cells were used for the group III sources. All $InAs_xP_{1-x}$/$In_yGa_{1-y}P$ SC-MQWs in this study were grown on InP SI substrates at 470°C. The solid composition of $In_yGa_{1-y}P$ was controlled by In and Ga flux determined by RHEED oscillation, while the composition of $InAs_xP_{1-x}$ was controlled by adjusting AsH_3 and PH_3 flow rates as predicted by a kinetic model[2,9]. Fig. 1 shows the experimental and simulated arsenic solid composition as a function of AsH_3 flow rate[2]. Experimental X-ray (004) rocking curve of InAsP/InGaP SC-MQWs were taken with a Phillips x-ray diffractiometer with double crystal geometry, and XTEM measurements made on a Hitachi H800 electron microscope operated at 200kV. Photoluminescence measurements were carried out at 300 K and 77 K with argon-ion laser excitation, and the luminescence was analyzed by a SPEX 1m monochromator and detected by a LN_2 cooled Ge detector connected to a lock-in amplifer. The laser power was varied over the range of 2.4 to 65 mW.

Results and Discussion

a. Structural analysis

InAsP/InGaP SC-MQWs without and with InP(3ML) insertion layers were analyzed by high-resolution x-ray diffraction. Figure 2(a) and (b) shows x-ray (004) rocking curves for SC-MQWs without and with 3ML InP insertion layer. The 0th-order is located just on the substrate peak for both samples, indicating the average lattice constant of the epitaxial layers is almost the same as that of InP substrate.
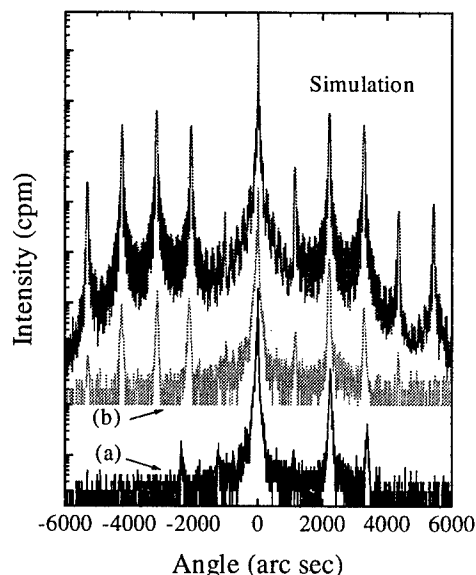
Fig. 2. Measured and simulated X-ray rocking curve of 20 period InAsP/InGaP SC-MQW (a) without InP insertion layer, (b) with InP insertion layer

Fig. 3. (002) cross-sectional transmission electron microscopy image taken from SC-MQW with InP insertion layer.

However, asymmetric satellites were observed for the SC-MQWs without InP insertion layer. The Intensity of +2nd and +3rd satellites is much larger than -2nd and -3rd, respectively, which indicates that there are asymmetric heterointerfaces of InAsP-on-InGaP and InGaP-on-InAsP. In contrast, more symmetric and sharp satellite peaks up to the 5th order are observed for SC-MQW with InP insertion layers. These narrow and symmetric satellite peaks are indicative of strong periodicity, a high

degree of lateral uniformity, and well-defined interfaces. The simulated DCXRD spectrum is shown in the top of Fig. 2 for comparison. The best fit of the experimental spectrum suggests the SC-MQW with InP insertion layer consists of 13.5 ML $In_{0.2}Ga_{0.8}P$, 3ML InP and 12 ML $InAs_{0.5}P_{0.5}$, which correspond well with the nominal values determined by RHEED oscillation and kinetic model predication.

An (002) cross-sectional transmission electron microscopy image taken from SC-MQW with InP insertion layer is shown in Fig. 3. The layer thickness deduced from DCXRD of both samples agrees with the TEM measurement. Despite the growth of 30 periods, it is clear from Fig. 3 that the whole structure is free of misfit dislocations. From XTEM micrographs, the 3 ML InP insertion layers allow planaraization of lateral thickness undulations, so that both normal (InAsP on InP/InGaP) and inverted (InGaP on InP/InAsP) interfaces are clearly defined, thus yielding high overall crystal quality.

b. Optical analysis
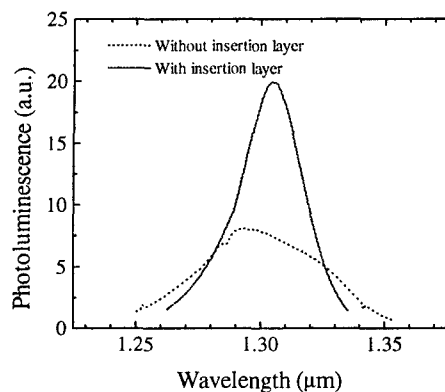
Fig. 4. Room temperature photoluminescence (PL) spectrum of SC-MQW with and without InP insertion layer

Fig. 4 shows the room temperature PL spectra of the SC-MQWs with and without InP insertion layers. The emission wavelength for both samples is around 1.3 μm. As shown in this figure, the intensity of the SC-MQW without insertion layer is much lower than the SC-MQW with the InP insertion layers. To investigate the importance of the InP insertion layers, the

thickness of the layers was varied (0 ML-3 ML) and experimentally correlated with overall crystal quality. The full-width at half-maximum (FWHM) of the room-temperature PL spectrum for these structures is plotted against the thickness of the InP insertion layer in Fig. 5, which shows that the FWHM decrease with increasing InP insertion layer thickness. The improvement in FWHM indicates an improvement in material quality.
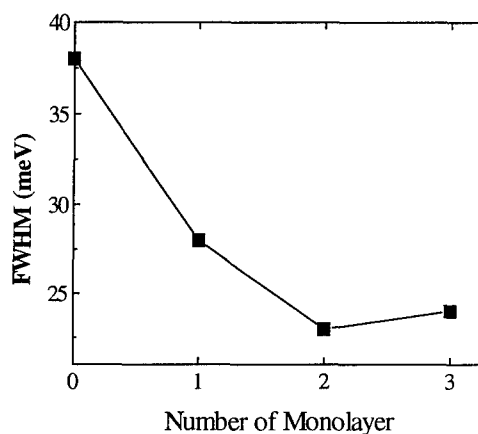
Fig. 5. The full width at half maximum (FWHM) of room temperature photoluminescence (PL) spectrum plotted against the thickness of InP intermediate layer.

The PL emission wavelength variation with excitation power can also indicate the quality of InAsP/InGaP heterointerfaces. Fig. 6 shows the PL emission wavelength as a function of the excitation intensity for SC-MQWs with and without InP insertion layers. The emission of the SC-MQWs with InP insertion layers is nearly constant for the excitation intensities investigated at 77K and 300K suggesting that the main emission from the samples is associated with the recombination of the heavy-hole bound excitons and that all of the PL has fa single origin. However, the dependence of the PL emission wavelength on the excitation intensity on SC-MQW without InP insertion layer exhibits more complicated behavior. The emission wavelength rapidly increases and reaches a maximum blue shift of about 12nm as

334

the excitation intensity increases up to 45 mW. As the excitation intensity intensity increases further, the emission wavelength shows a small red shift. This suggests that the PL has multiple origins and that the percentage of the thin part of the well which produces the high energy level is very small in this sample, resulting in early saturation of the states by increasing excitation intensity at low intensity.
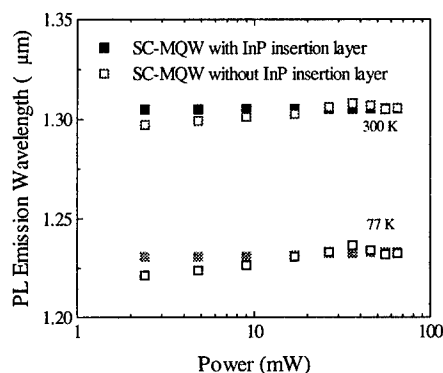
Fig. 6 Variation of the PL peak emission wavelength with the excitation power.
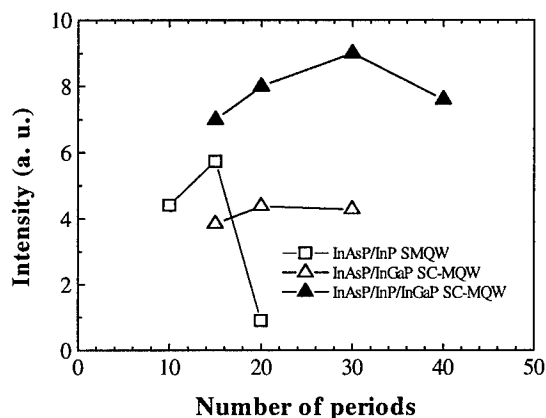
Fig. 7. The luminescence intensity of the room temperature PL spectra of the uncompensated InAsP/InP strained MQWs and InAsP/InGaP SC-MQWs with and without intermediate InP layers.

Finally, a series of strain-compensated InAsP/InP(3ML)/InGaP MQWs with differing numbers of periods (15, 20, 30, and 40) were grown. No misfit dislocations were observed

even for a 40-period structure. The intensity of the room temperature PL spectra are much improved over the uncompensated InAsP/InP strained MQWs and InAsP/InGaP SC-MQWs without insertion InP layers as shown in Fig 7.

Conclusion

High-quality InAsP/ InP(3ML)/InGaP SC-MQWs with zero net strain up to 40 periods were grown by GSMBE. Compared with uncompensated InAsP/InP strained MQWs and InAsP/InGaP SC-MQWs without the InP insertion layers, much sharper and symmetric satellite peaks in double-crystal X-ray diffraction and excellent photoluminescence was obtained from SC-MQWs with the InP insertion layers.

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SOLID SOURCE MOLECULAR BEAM EPITAXY GROWTH OF GaInP/AlGaInP HETEROSTRUCTURES AND 600-nm-RANGE QUANTUM WELL LASER DIODES

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Introduction

AlGaInP visible laser diodes have become increasingly attractive as light sources in various applications. Until now these lasers have been almost entirely grown by metalorganic chemical vapor deposition (MOCVD). Recently, there have been a few reports on solid source molecular beam epitaxy (SSMBE) growth of AlGaInP layers and GaInP/AlGaInP laser structures. Although the quality of SSMBE grown AlGaInP material has been shown to be good, the performance of SSMBE grown 600-nm-range laser diodes has been clearly inferior to that attained by MOCVD.

We have studied the growth of $(Al_xGa_{1-x})_{0.51}In_{0.49}P$ quaternary alloy and GaInP/AlGaInP heterostructures using solid, elemental phosphorus in a valved cracking cell by molecular beam epitaxy. The results obtained have been applied for the growth of strained-layer quantum well laser structures emitting at red-light region. In order to further assess the quality of our materials, the grown laser structures have been processed into laser diodes that have been characterized. The measured threshold current densities of the 1 mm long as-cleaved broad-area laser diodes were 385 A/cm^2 and 820 A/cm^2 at 680 nm and 633 nm, respectively. To the best of our knowledge these values are the lowest reported threshold current densities for SSMBE grown lasers in this wavelength range. A high T_0 of 113 K was obtained for double-QW in the temperature interval of 20 °C - 90 °C. All these results clearly demonstrate that state-of-the-art 600-nm-range laser diodes can be prepared using only solid sources.

I. Background

AlGaInP alloy is widely used in the fabrication of visible laser diodes. By varying the alloy composition and using the effects of strain it is possible to fabricate devices emitting from 620 nm to 690 nm. These red laser diodes are attractive light sources for many applications, such as high density optical disk memory systems, medical and industrial instrumentation, plastic fiber optics, bar-code readers, and solid state laser pumping. Many of these applications require high light output power, in addition to low operating currents and reliability.

Nowadays, GaInP/AlGaInP quantum well (QW) laser diodes with low threshold current and high optical output power are mostly being grown by metalorganic chemical vapor deposition (MOCVD).[1,2] Solid source molecular beam epitaxy (SSMBE), using a valved cracking cell loaded with elemental solid phosphorus, has recently been applied for the growth of AlGaInP material and GaInP/AlGaInP heterostructures.[3] SSMBE allows the growth of these phosphides without toxic phosphine gas. However, there have

not yet been many reports on the SSMBE grown red laser diodes.[4,5] In addition, the performance of these lasers has been modest compared to that of the lasers grown by MOCVD. Apparently, more work is needed to optimize the SSMBE growth procedures for AlGaInP alloy and 600-nm-range laser diodes.

II. Experimental

The MBE system used in this work was a VG V80H equipped with two independent valved cracking cells for P$_2$ and As$_{2(4)}$ flux generation. The phosphorus cracking cell had three separately heated zones and was loaded with elemental red phosphorus of 7N purity. Prior to growth an amount of white phosphorus was formed in the cell by heating the red phosphorus charge for a fixed time.[6] The group III and dopant materials (Si and Be) were evaporated from conventional effusion cells. The phosphorus cracking head was operated at 950 °C, whereas the arsenic cracking head was kept at 650 °C during this study to minimize the thermal load for the system. A more detailed description of our

growth system and deposition procedures can be found elsewhere.[7]

All the structures studied in this work were grown on exactly (100) oriented n-GaAs substrates.

III. Results and Discussion

A. Growth of AlGaInP

We first grew $(Al_xGa_{1-x})_{0.51}In_{0.49}P$ layers with different Al mole fraction in order to optimize the growth conditions. Narrow double crystal x-ray diffraction line widths ~25 arc sec (substrate 20 arc sec) were recorded across the whole composition range for layers over 2 μm in thickness. The optimal growth temperature was found to be around 510 °C. The growth rate was 1 - 2 μm/h and the beam equivalent pressure (BEP) of P_2 was about 2×10^{-5} mbar. Dopant concentrations over 10^{18} cm^{-3} were easily achieved for both the n- and p-type samples. Room temperature photoluminescence (RT PL) measurements for heavily Be-doped AlGaInP layers revealed the presence of a deep levels that may be due to the Al-Be related defects.[8]

Fig. 1 shows the RT PL peak intensity and the full width at half maximum (FWHM) of undoped 2 μm thick bulk $(Al_xGa_{1-x})_{0.51}In_{0.49}P$ layers as a function of Al composition. The band-edge luminescence was dominant in all these samples. The relatively narrow line widths indicate good homogeneity and optical quality of the epitaxial layers.

A broadening of the PL line width and a decrease in peak intensity were observed with increasing Al composition. The measured values are consistent with the previously reported data on MBE grown AlGaInP layers.[9]

B. Growth of GaInP/AlGaInP heterostructures

We have grown a multilayer structure containing 5 unstrained $Ga_{0.51}In_{0.49}P$ QWs sandwiched between 300 Å thick $(Al_{0.5}Ga_{0.5})_{0.51}In_{0.49}P$ barriers. The nominal well widths were 25, 50, 75, 100 and 150 Å. Fig. 2 shows the low-temperature PL (8 K) spectrum of this sample. The sample was excited by 488 nm light from an Ar$^+$ ion laser. The quantum wells exhibited very intense PL and their structural quality was good, as demonstrated by the narrow PL linewidths. The values obtained were 12, 8, 8, 10 and 14 meV for well widths of 150, 100, 75, 50 and 25 Å, respectively. These linewidths are comparable to the best values reported in literature.[3]
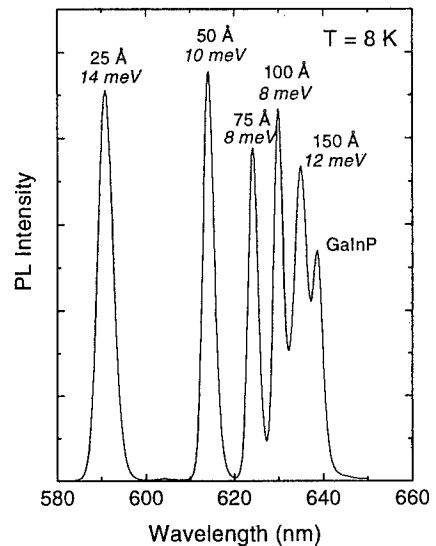
Fig. 2. Low temperature (8 K) PL spectrum of multiple single-QW sample. Unstrained $Ga_{0.51}In_{0.49}P$ QWs were sandwiched between $(Al_{0.5}Ga_{0.5})_{0.51}In_{0.49}P$ barriers. PL peak marked as 'GaInP' corresponds to a 0.1 μm thick bulk $Ga_{0.51}In_{0.49}P$ layer. QW thickneses and FWHM values are given in the figure.

A good agreement between experimental and calculated (applying a simple envelope wavefunction approximation with the effective masses given in Ref. [10]) PL energies were obtained if the values of 0.23 eV and 0.075 eV were used for ΔE_c and ΔE_V, respectively.

In addition, several PL test layers were prepared with an anticipation of growth of laser diodes. The test samples contained either a compressively strained or a tensile-strained QW sandwiched between AlGaInP guiding and cladding layers. Fig. 3 displays the PL peak intensities as a function of growth temperature for PL from both the QW ($Ga_{0.4}In_{0.6}P$) and the barriers ($(Al_{0.3}Ga_{0.7})_{0.51}In_{0.49}P$). The FWHM for 670 nm QWs was around 26 meV. The maximum PL intensity was obtained for the samples grown at the temperature of about 480 °C.
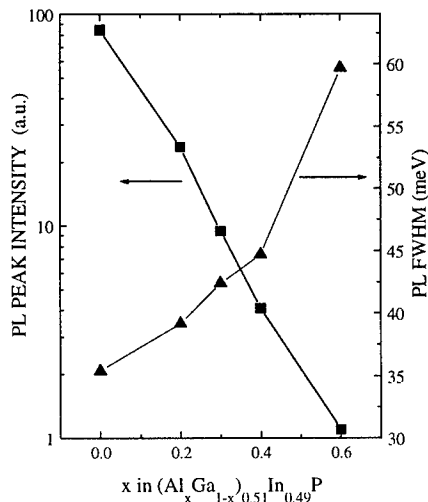

Fig. 1. Photoluminescence peak intensity and full width at half maximum of undoped 2 μm thick $(Al_xGa_{1-x})_{0.51}In_{0.49}P$ layers measured at room temperature as a function of Al composition. All the layers are closely lattice-matched to GaAs.

337

Fig. 3. PL peak intensities from both a compressively strained 670 nm quantum well (upper curve) and $(Al_{0.3}Ga_{0.7})_{0.51}In_{0.49}P$ waveguide/barrier material (lower curve) as a function of growth temperature are shown.

We should note that this PL behaviour did not correlate with the performance of the laser diode structures grown at different temperatures. The optimum growth temperature for the studied laser structures was found to be around 510 °C.

C. Growth and characterization of 600-nm-range laser diodes

Having studied the above test samples we proceeded to grow graded-index separate confinement heterostructure GaInP/AlGaInP QW lasers. These lasers comprised one or two compressively strained QWs (680 nm) or one tensile-strained QW (633 nm). The laser structures are shown schematically in Fig. 4.

Prior to growth, the substrates were thoroughly outgassed at 200 °C in a separate preparation chamber to minimize the water vapor contamination into the growth chamber. In addition, an extensive outgassing of source materials was carried out before growths.

The GaAs buffer layer was grown at 590 °C and the p-GaAs top contact layer near 530 °C. The growth temperature for AlGaInP was ~510 °C and for GaInP 500 °C. The growth rate of AlGaInP was 1 μm/h. The other growth rates were selected on condition that no growth interruptions were needed near the active region.

Prior to device fabrication, *ex situ* annealing (~900 °C for 1 sec) of the prepared laser wafers was applied. The optimization of annealing conditions will be discussed in greater detail elsewhere. The prepared laser structures were processed into 40 - 120 μm wide oxide stripe lasers wi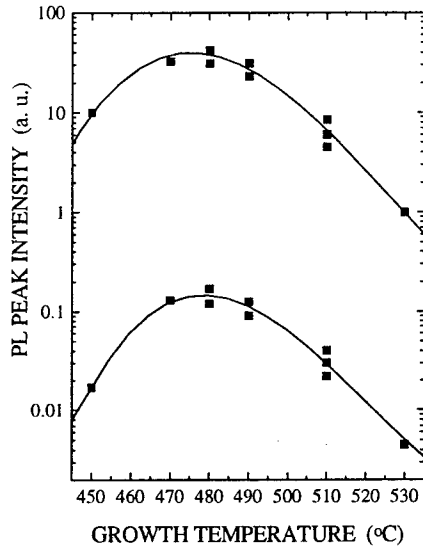th cavity lengths ranging from 400 to 2000 μm. The chips were wire bonded p-side up by epoxy on copper heat-sinks for testing.

p+ GaAs contact	0.15 μm	$p = 5 \times 10^{19}$ cm^{-3}
p+ $Ga_{0.51}In_{0.49}P$	0.1 μm	$p = 2 \times 10^{19}$ cm^{-3}
p-$(Al_xGa_{1-x})_{0.51}In_{0.49}P$ cladding	0.9 μm	$p = 1 \times 10^{18}$ cm^{-3}
$(Al_xGa_{1-x})_{0.51}In_{0.49}P$ GRIN	0.1 μm	undoped
$(Al_xGa_{1-x})_{0.51}In_{0.49}P$ waveguide	0.05 μm	undoped
$Ga_yIn_{1-y}P$ quantum well		undoped
$(Al_xGa_{1-x})_{0.51}In_{0.49}P$ waveguide	0.05 μm	undoped
$(Al_xGa_{1-x})_{0.51}In_{0.49}P$ GRIN	0.1 μm	undoped
n-$(Al_xGa_{1-x})_{0.51}In_{0.49}P$ cladding	0.9 μm	$n = 1 \times 10^{18}$ cm^{-3}
n-$Ga_{0.51}In_{0.49}P$	0.05 μm	$n = 2 \times 10^{18}$ cm^{-3}
n-GaAs buffer	0.1 μm	$n = 2 \times 10^{18}$ cm^{-3}
n-GaAs (100) exact cut substrate		

Fig. 4. Schematic layer structures for 633 nm and 680 nm lasers studied in the present work. The 633 nm lasers contained a 8 nm thick tensile-strained QW with y = 0.6. The x value was 0.6 and 0.95 in the guiding and cladding layers, respectively. The 680 nm laser contained 7 nm thick compressively strained QWs (y=0.42), and waveguides with x = 0.3 and claddings with x = 0.7. The GRIN regions were linearly graded from the composition of the claddings to the composition of the waveguides in the both structures.

Fig. 5 shows the threshold current density (J_{th}) of as-cleaved 680 nm and 633 nm lasers as a function of inverse cavity length. A 1 mm long 680 nm (633 nm) laser exhibited a J_{th} = 385 A/cm^2 (820 A/cm^2). The measured values are very close to those obtained by MOCVD.
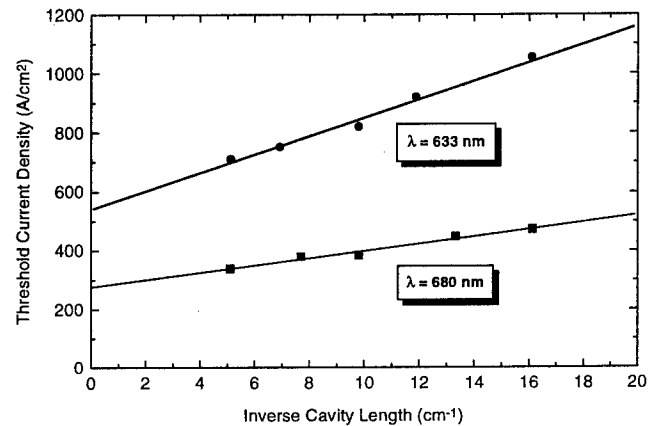

Fig. 5. Threshold current density versus inverse cavity length for 633 nm and 680 nm lasers.

338

The differential quantum efficiency (η_D) per facet was 26 % for the 633 nm $L = 1000$ μm laser and 28 % for the 680 nm $L = 800$ μm laser. These η_D's are comparable to those reported for the MOCVD-grown lasers. The internal losses were low, 5.3 cm^{-1} and 3.9 cm^{-1} for the 633 nm and 680 nm lasers, respectively.

The temperature dependence of J_{th} for single and double QW 680 nm lasers is shown in Fig. 6. A high T_0 of 113 K was obtained for double-QW in the heat-sink temperature interval from 20 to 90 °C. For the 633 nm lasers ($L = 1000$ μm) T_0 was typically around 45 K between 10°C and 60 °C.
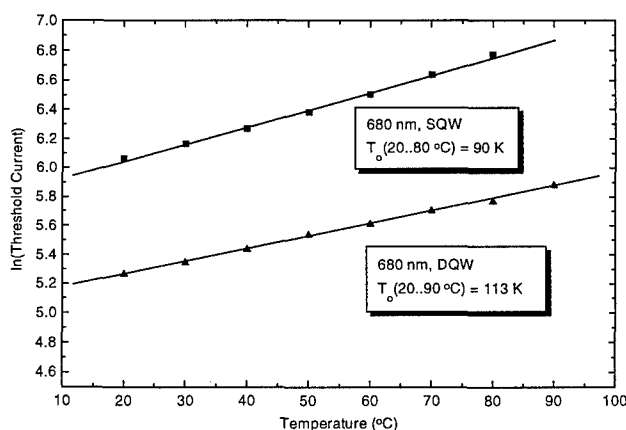

Fig. 6. *Temperature dependence of threshold current density of single-QW and double-QW lasers emitting at 680 nm.*

IV. Conclusions

SSMBE growth of the $(Al_xGa_{1-x})_{0.51}In_{0.49}P$ quaternary alloy, GaInP/AlGaInP heterostructures, and 600-nm-range laser diodes has been studied in this paper. The optimization of SSMBE growth conditions for these materials and structures has been carried out to a reasonable extent. As a result, high-quality epilayers and laser diode structures have been prepared. The performance characteristics of the fabricated laser diodes are very close to those achieved by MOCVD.

We have found it very important that unintentional impurities, notably oxygen and water, originating from the effusion cells and the growth environment are prevented from incorporating into the growing front of AlGaInP layers. This can be achieved by extensive, pre-growth outgassing of the source materials and the substrate. If such a care is properly exercised and the ultra-pure source materials are used, then high-performance red laser diodes can be made by SSMBE. We shall also note that the reproducibility of the samples from one growth to another looks reasonably good.

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Growth and Characterization of GSMBE Grown Strained

InGaAs/InGaAsP Structures for MQW Lasers at 2.0μm

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Introduction

In this paper we report on the growth, characterization and performance of compressively strained $In_{0.75}Ga_{0.25}As$/InGaAsP (λ_g=1.3μm) MQW structures on InP substrates for laser diodes at 2.0-2.1 μm range. These laser wafers were grown by gas source molecular beam epitaxy (GSMBE) for the first time. Both of broad area and ridge-waveguide structure lasers have been fabricated and evaluated. The electrical and optical properties of high quality of InGaAsP corresponding to the band wavelength of 1.3μm have been investigated in details.

I. Background

mid-infrared lasers offer many important applications for laser spectroscopy, atmospheric transmission, eye-safe medical care and trace chemical detection. We have investigated AlGaAsSb/InGaAsSb QWLD on GaSb substrates grown by solid source molecular beam epitaxy (SSMBE) with lasing wavelengths at room temperature in the range 2.0-2.1μm as light source for these applications.[1] Strained InGaAsP/InGaAs structures on InP substrate by MOCVD have been reported as one alternated approach for the development of semiconductor laser diodes in the spectral range 1.8-2.1μm.[2-5] In this letter, we report the growth and characterization of compressively strained $In_{0.75}Ga_{0.25}As$/InGaAsP/InP MQW structures for laser diodes at 2.0μm range by gas source MBE for the first time.

II. Experiments

The InGaAs/InGaAsP strained MQW structures for this study consists two wells of $In_{0.75}Ga_{0.25}As$, separated by barrier of InGaAsP with a composition corresponding to

wavelength of 1.3μm. The InGaAsP single layers and the laser structures were grown on (100) oriented semi-insulating InP substrates or on S-doped n-type InP substrates by GSMBE respectively. The pre-growth heat treatment was carried out in phosphorus beams at a temperature of about 520°C measured by an infrared pyrometer. The In and Ga flux were calculated and precisely measured by an in situ ion gauge to get appropriate In to Ga ratio of composition in InGaAsP alloy for the wavelength at 1.3μm. The growth rate was 1.2μm/hour. The ratio of PH_3 pressure to AsH_3 pressure was varied to achieve lattice matching of InGaAsP with InP substrate. The substrate temperatures were also varied for study of the dependence of layer properties on the substrate temperatures. The structural, electrical and optical properties were evaluated and determined by double-crystal X-ray diffraction rocking curve (DCXRC), Hall measurement and Fourier transform photoluminescence (FTPL).

The laser structures reported here consist of two quantum wells of $In_{0.75}Ga_{0.25}As$ each 10nm wide, separated by 20nm of InGaAsP barrier (band gap wavelength of 1.3μm), sandwiched between 0.15μm InGaAsP on both sides. Si-doped InP and Be-doped InGaAsP were used as lower cladding layer and upper cladding layer, respectively. Finally heavily Be-doped $In_{0.53}Ga_{0.47}As$ was grown on the top as contacting layer. Two device structures were fabricated by wet chemical process, broad stripe structure with 100μm in width and 500μm in length and ridge waveguide structure with 10μm in width, to test the performance of the lasers.

III. Results and discussion

A. The properties of InGaAsP

Table 1 shows the double crystal X-ray rocking curves (DCXRC) and Hall measurement results of unintentionally doped InGaAsP ($\lambda_g=1.3$μm) layers. The growth rates are 1.2μm/hr. The ratio of AsH_3/PH_3 are 290 Torr / 420 Torr, except sample GM603 being 300 Torr / 400Torr.

Table 1 Some structural and electrical properties of unintentionally doped InGaAsP ($\lambda_g=1.3$μm)

Sample No.	Sub. Temp. (°C)	$\Delta d/d$	FWHM ('')	n_{300} (cm^{-3})	μ_{300} (cm^2/V.s)	n_{77} (cm^{-3})	μ_{77} (cm^2/V.s)
GM603	520	2.4×10^{-3}	106	2.4×10^{-16}	2,488	1.3×10^{-16}	6,329
GM608	510	3.0×10^{-4}	64	8.6×10^{-15}	3,974	6.9×10^{-15}	8,699
GM607	500	4.8×10^{-4}	50	8.2×10^{-15}	4,167	6.6×10^{-15}	9,316
GM655	480	-1.3×10^{-3}	13	2.6×10^{-15}	4,262	1.6×10^{-15}	13,000

Table 1 indicates that the substrate temperatures have sensitive effect on the layer properties. At high growth temperature, the layers have poor crystal properties with large full width at half maximum (FWHM) of DCXRC and poor electrical properties with low mobilities. As the growth temperature from 520°C down to 480°C, the FWHM of DCXRC became narrower and dramatically down to 13''. The mobility at room temperature and 77K were enhanced as high as 4262cm^2/V.s and 1.3×10^{3}cm^2/V.s, respectively. The surface morphologies of the samples under Normaski interference microscope shown the similar dependence on the growth temperature. The layers had rough surface at high temperature while the surface became smooth at low temperature. The sensitive dependence of layer qualities on the growth temperature

may results from the existence of a miscibility gap near the InGaAsP alloy compositions corresponding to the wavelength 1.3μm. The broading of DCXRC peaks is usually due to high defect densities, cluster formation or other material inhomogeneities and the reduction in Hall mobilities may be due to the additional scattering mechanisms caused by material inhomogeneities.

Si doped InGaAsP were grown at low temperature (480°C) and constant AsH$_3$ and PH$_3$ pressures. The dependence of electron Hall mobility on the electron concentration is shown in Fig. 1.
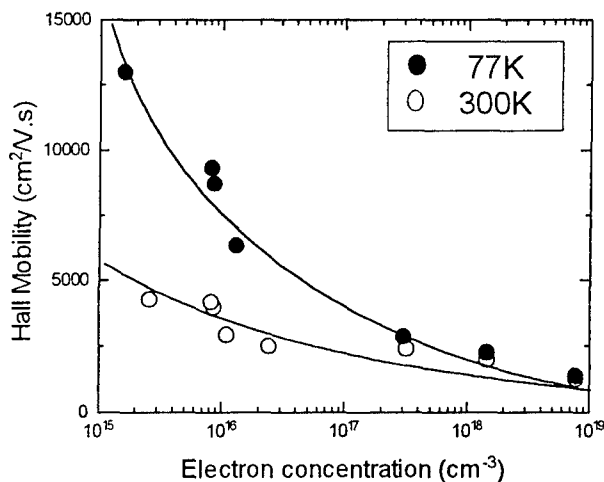
Fig. 1 The dependence of Hall mobility on the electron concentration of GSMBE grown InGaAsP

Fig. 2 shows the PL spectrum of one InGaAsP sample at 77K. The FWHM of PL was 20meV from the figure while it is 50meV at room temperature. The FWHM agree with well the value of 1.8KT (46meV at room temperature and 13meV at 77K) expected for a band to band transition between simple parabolic bands.

B. InGaAs/InGaAsP QW lasers

Both of broad stripe structures with 100μm in width and 500μm in length and ridge waveguide structure with 10μm in width laser diodes were fabricated to test the performance of InGaAs/InGaAsP strained QW lasers. Both of two structures were fabricated using same one epi-wafers. The current-voltage characteristics of the devices shown a turn-on voltage of ~0.7V and very low reverse leakage current that indicated the high quality of the grown epilayers. The room temperature eletroluminescence (EL) spectrum for the broad stripe structure is shown in Fig. 3. The peak wavelength is 1.98μm with FWHM =119meV which indicated the precise design and control of material composition and thickness. Fig. 4 shows the lasing spectrum of the ridge waveguide structure at 77K with an pulsed injection current 70mA. The FWHM dramatically decreased to 5.3nm. For ridge waveguide lasers, the lasing at room temperature have also been achieved.

Fig 2. The PL spectrum of InGaAsP at 77K
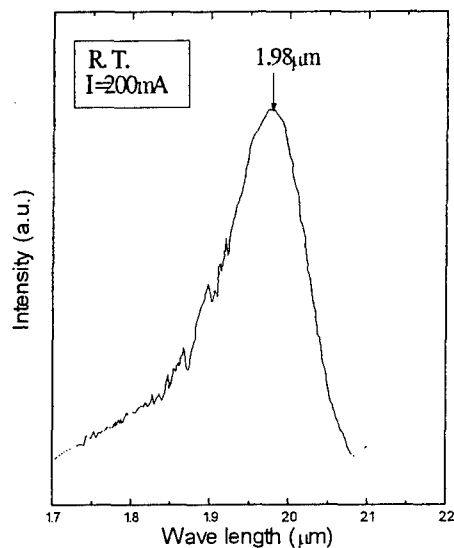
Fig 3. The electroluminescence of broad-area InGaAs/GaInAsP quantum structure at room temperature
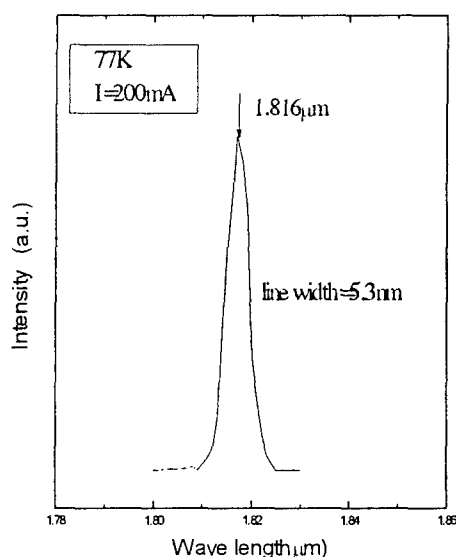
Fig. 4. The lasing spectrum of ridge
waveguide structure at 77K

IV. Conclusions

High quality of InGaAsP layers corresponding to band wavelength of 1.3μm and strained InGaAs/InGaAsP MQW laser structures have been grown by GSMBE. The properties of InGaAsP layers have a sensitive dependence on the growth temperature. With the optimization of growth condition, high quality InGaAsP layer with narrow DCXRC and PL FWHM, high Hall mobility have been obtained. The EL at room temperature of broad-area of InGaAs/InGaAsP strained MQW laser structures have shown the peak wavelengthat 1.98μm, indicating the precise control of material composition and layer thickness. Pulsed lasing at 77K have been achieved under injection current of 70mA for the ridge waveguide structure of laser diodes and the FWHM of spectrum is 5.3nm with peak at 1.816μm. The lasing at 300K have also been observed

V. Acknowledgements

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DARK CURRENTS IN COMPOSITIONALLY-GRADED In$_x$Ga$_{1-x}$As (.53 < x < .82)

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Introduction

Best results with light detection in the near-infrared spectrum (0.5 - 2.5 μm) have been obtained with indium gallium arsenide (In$_x$Ga$_{1-x}$As). One- and two-dimensional arrays of this material are used in applications as diverse as blood glucose monitoring and artwork analysis. In$_{.53}$Ga$_{.47}$As cameras are particularly well suited for night vision using the afterglow of the night sky, especially on moonless nights. This composition is "lattice-matched" to InP substrates and produces dark currents nearly as low as theoretical predictions. However, to detect light in the 2 μm region, it has been necessary[1] to "compositionally-grade" this material to higher indium content and thereby introduce dislocations which can increase dark currents by several orders of magnitude. This paper reviews the current state-of-the-art of compositionally-graded InGaAs, including crystal growth techniques, figures of merit, and future projections for this material over the next several years.

I. CRYSTAL GROWTH TECHNIQUES

Compositionally graded alloys of InGaAs have been grown by hydride[2] and chloride[3] vapor phase epitaxy (VPE), organometallic VPE[4] (OMVPE), molecular beam epitaxy (MBE)[5] and even bulk[6]. InGaAs has also been used for high-speed electronics applications, due to its high mobility. Here, we will be concerned with optoelectronic device applications, primarily in near-infrared detection.

Figure 1 contains a description of two methods of compositional grading employed to fabricate photodetectors for the 2 μm spectral region. These techniques are employed to reduce dislocation density in the p/n junction region to decrease dark current. The method in Figure 1a is typically employed by all three VPE techniques (hydride, chloride, and OMVPE) while the method in Figure 1b is typical of MBE and requires much thinner layers.

The hydride VPE technique has the major advantage that it typically achieves growth rates of 20 - 30 μm/hr to allow easy fabrication of thick structures such as Figure 1a. Chloride VPE, with its ~10 μm/hr grow rate has also grown these structures successfully. The early use of these thick graded structures provided a barrier to both OMVPE and MBE with their 1 - 2 μm/hr growth rates although the structure shown in Figure 1a has also been grown by OMVPE. The structure shown in Figure 1b is the type that is typically employed with MBE. Although hydride VPE has the growth rate advantage, ultimately the OMVPE and MBE techniques should win out for 2.0 - 2.5 μm detector fabrication (as OMVPE already has for lattice-matched 1.7 μm detector production) due to their much higher uniformity and potential for 3" and 4" wafers. The MBE technique has limited flexibility with phosphorous

compounds and thus has typically used InAlAs as the high bandgap material.

The sensitivity of InGaAs detectors is limited by the detector dark current (leakage current that flows under reverse bias of 1 - 10 volts) or "shunt resistance" (R_0 - the slope of the voltage-current curve near zero bias). A characteristic figure of merit is the shunt resistance-area product or "R_0A". Both dark currents, and R_0 are limited by background doping and crystal defects in the InGaAs. These defects, which include misfit dislocations and stacking faults, are introduced during the growth of these materials when the composition is changed from x = 0.53 (lattice-matched to the InP substrate) to higher values which allow absorption of longer wavelengths. Cutoff wavelengths can be varied from 1.7 μm (x=0.53) to 2.1 μm (x=0.73) and 2.5 μm (x=0.82).

InGaAs focal plane arrays are typically seven to ten mm square and could constitute the first real commercial demand for larger size and volume of InP substrates for optoelectronic applications.

II. DETECTOR RESULTS

There are numerous reports on dark current values from p/n junction photodiodes made in graded In$_x$Ga$_{1-x}$As (0.53 < x < 0.82). These values range from 30 mA/cm^2 for hydride VPE-grown[7] 2.5 μm material, to 0.1 mA/cm^2 for OMVPE grown[8] 2.1 μm material to 2 mA/cm^2 for MBE grown[9] 2.1 μm material. These values are constantly being improved upon and are highly dependent on

processing and grading techniques employed, as well as basic material parameters. Thus comparisons between techniques and laboratories are difficult at best. We have had an ongoing program to characterize InGaAs material for use in commercial 1.7 - 2.5 μm detector arrays and cameras. Infrared detectors are often operated near zero reverse bias to minimize their dark currents. Table 1 contains a summary of present-day results, all obtained in our laboratory using the same processing and measurement techniques and equipment on wafers produced by the different growth techniques. While commercially viable devices have been made with these materials, higher values have been reported and we expect marked improvements with all the techniques in the next 2 - 3 years.

Table 1. Typical InGaAs R_0A values (ohm-cm^2) @ 300 K

	2.1 μm	2.5 μm
VPE	1000	300
OMVPE	500	10
MBE	200	3

III. THE FUTURE

What can be expected? High-quality lattice-matched $In_{.53}Ga_{.47}As/InP$ detector structures with 1.7 μm cutoffs are nearly dislocation-free and produce R_0A values in excess of 500,000 ohm-cm^2. If the defects associated with compositional grading could be removed, it is interesting to speculate on what R_0A values might be obtainable for 2.1 and 2.5 μm cutoff detectors. Assuming that the only difference among the materials is the exponential dependence of R_0 upon bandgap, the decrease in R_0A product due to bandgap alone is estimated[10] to be on the order of 100X for 2.1 μm $In_{.7}Ga_{.3}As$ and 1000X for 2.5 μm $In_{.8}Ga_{.2}As$. Thus one might speculate that by eliminating dislocations in these materials, the R_0A product could be increased nearly 10X for both cutoff wavelengths. This in turn translates into a 3X increase in overall detector sensitivity, a significant improvement. And how might these dislocations be removed? Two solutions have been offered at this conference. Bonner[6] reports the bulk growth of ternary InAsP substrates with arsenic concentrations of ~10%. If values near 40% can be achieved, the substrate lattice parameter will match the epitaxial layer and no grading will be necessary. Ejeckam et al[11] reports the use of a "compliant universal"(CU) substrate: a highly significant new technique of using wafer bonding with "twist" boundaries to allow the epitaxial growth of thick epitaxial layers with over 14% lattice mismatch without dislocation propagation into the epitaxial layer. The next two years should witness some dramatic breakthroughs with so-called "lattice-mismatched" materials. Cameras based on 1 cm^2 square InGaAs imaging chips[12] will undoubtedly

increase the drive toward 3" and 4" diameter InP substrates as their costs drop and uniformity improve towards silicon based devices.

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12 M.J. Cohen, "Near Infrared InGaAs Cameras", Laser Focus World 29, 109-112 (1993)

a) VPE

InAs.5P.5 CAP

In.76Ga.24As

y=.50

InAsyP1-y buffer structure

y=.45
y=.40
y=.35
y=.30
y=.25
y=.20
y=.15
y=.10
y=.05

15 μm

b) MBE

contact
cap
In.74Ga.26As
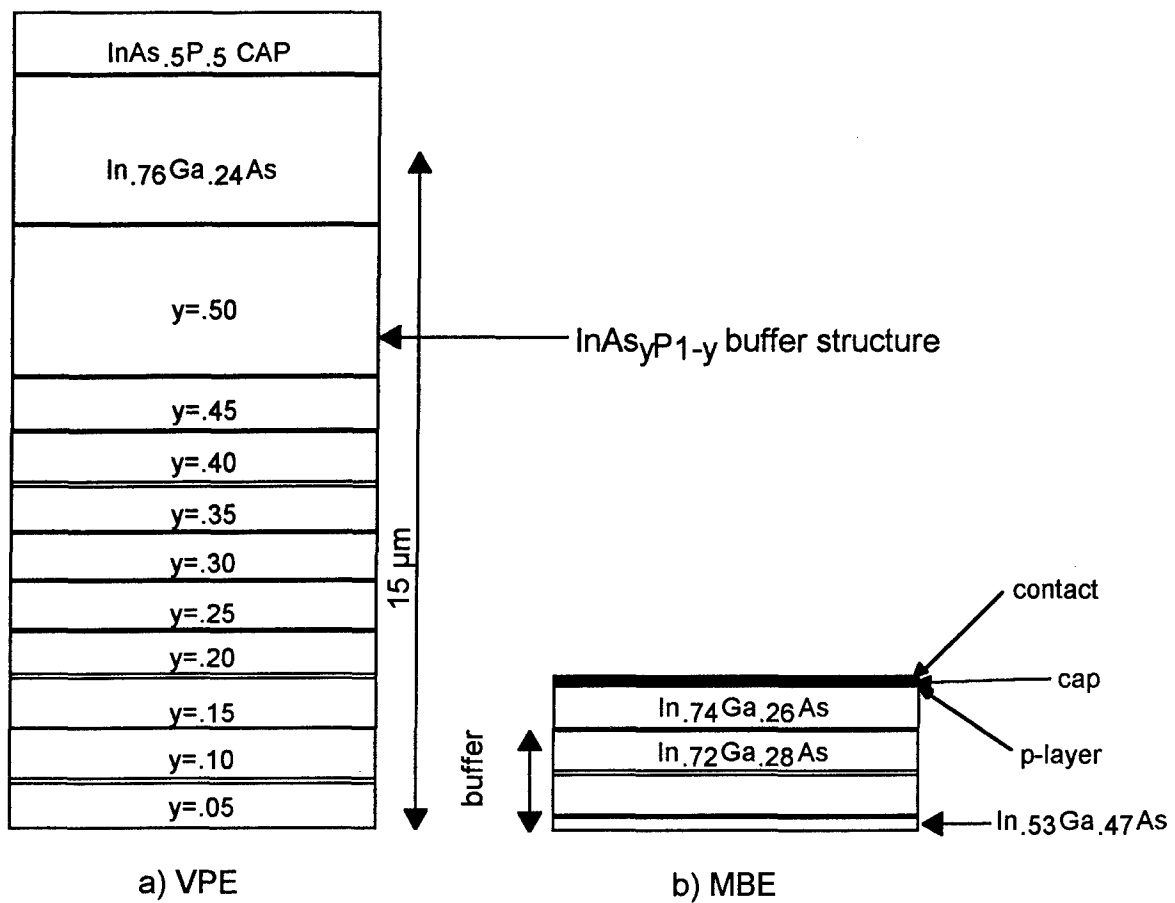In.72Ga.28As
p-layer
In.53Ga.47As

buffer

Figure. 1.   Epitaxial structures used to grow VPE and MBE InGaAs wafers for 2.1 μm.

InP BASED MATERIALS FOR LONG WAVELENGTH OPTOELECTRONICS GROWN IN MULTIWAFER PLANETARY REACTORS®

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Introduction

We present an investigation of the growth of InP based materials in a Multiwafer Planetary Reactor®. A reactor suited for the simultaneous growth of 15 x 2", 8 x 3" or 5 x 4" wafers was used to grow InP, GaInAs and various GaInAsP compositions. As predicted by the theory of the Planetary Reactor® principle, excellent uniformities of all layer properties were found. Without any tuning of process parameters, thickness variations of ±1% or better were obtained. The compositional uniformity was also very good. This was confirmed by X-ray diffraction and PL mapping. Emission wavelength uniformities were in the 1 nm range. P-and n-type doping was also investigated. Sheet resistivity measurements on doped samples reveal uniformities around 1%.

I. General

Multiwafer MOVPE is a state-of-the-art technique for the industrial mass production of III-V devices. This is true for all devices where large wafer areas are required, especially for GaAs based solar cells and UHB-LEDs based on AlGaInP. These materials are grown in multiwafer Planetary Reactors® with wafer loading capacities of 7x2", 15x2", 35x2" or 95x2" wafers. The reactors have some unique properties in common. They are true horizontal reactors with a central gas injection while the gas is flowing radially to an exhaust ring. Thus the gas velocity changes with the radius leading to nearly linear depletion profiles instead of the usual exponential ones. Since the wafers are rotated twice in this reactor, excellent uniformities can be obtained in combination with high growth efficiencies (depending on the reactor size between 30 and 50% for the group III alkyles). Furthermore, the uniformity is an inherent property of the reactors. In wide parameter ranges a good uniformity can be obtained. No tuning of flow rates is necessary to grow uniform layers.

The gas flowing through the reactor does not see any side walls since it is injected in the center of the reactor. The reactor top consists of a thermostated ceiling in order to minimize deposition there. However, it can be exchanged easily during loading the reactor.

Planetary Reactors® have been used for years, mainly for GaAs based materials. Some are already producing InP based materials. These are 7x2" wafer reactors so far. Now, for the first time a 15x2" wafer machine was used. According to the considerations above, no serious problems should arise when scaling up the process. The aim of this paper is to demonstrate this.

II. Experimental

As a growth reactor an AIX 2400 Planetary Reactor® was used. Various susceptor geometries can be used by simple replacement of graphite parts. 11x2", 15x2", 5x4" or 8x3" wafer setups are possible. A sketch of these different setups is shown in fig. 1. The reactor is lamp heated and operated at total pressures between 50 and 200 mbar. For this study, a total pressure of 200 mbar was chosen. The total gas flow rate was 22.4 l/min and the deposition temperature measured by a thermocouple was 660 °C. V/III ratios were typically around 100. Group V and group III injection flows are separated; the injection flow ratio was 1:14.

Growth was performed on various types of InP substrates, usually (100), 2° off-oriented. Characterization was done by DCXD using a Bede QC2a diffractometer and by room temperature PL using a Waterloo PLM mapper. Thickness measurements were performed by white light interference measurements. Doping uniformity was checked by a Lehighton sheet resistivity mapper.
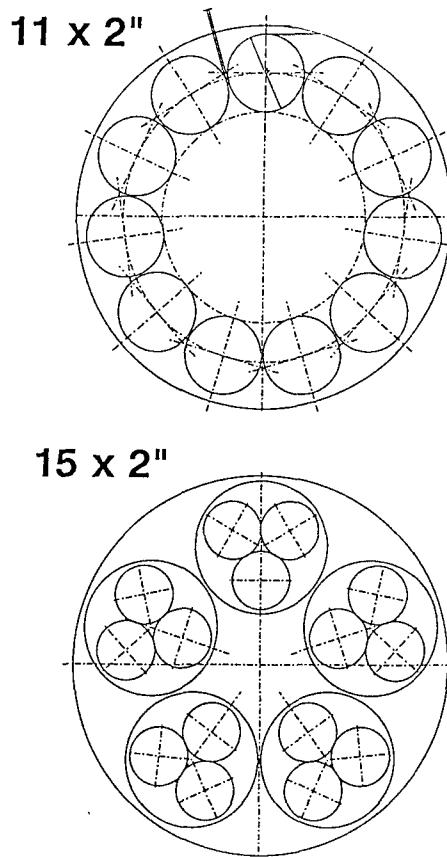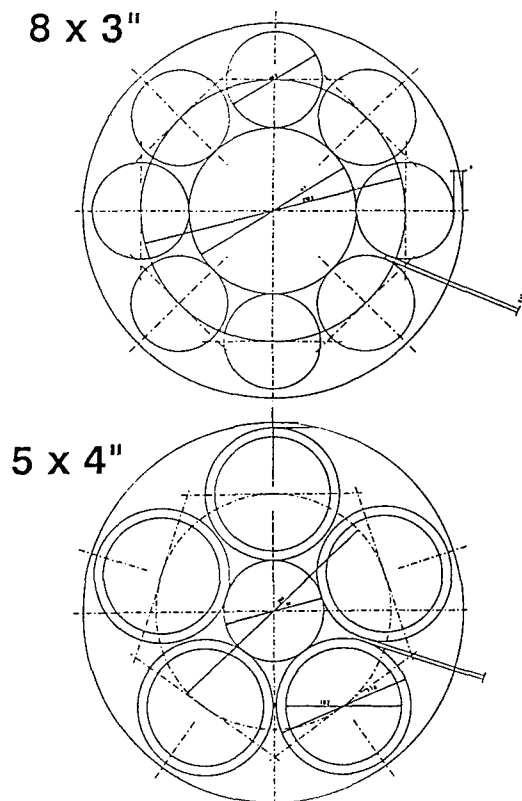
Fig. 1: Susceptor geometries of the AIX 2400 Planetary Reactor®

III. Results

As test materials InP and GaInAsP with an emission wavelength of approx. 1.5 µm was chosen. Growth rates around 1 µm/h were adjusted. The layers revealed smooth surfaces. Thickness variations were below 2% across a 2" wafer. This was found to be similar for GaInAsP and InP layers. The most important layer property, however, was the compositional uniformity. This was checked by room temperature PL mapping. A result of a PL measurement is shown in fig. 2.

348

based materials. Furthermore, it indicates a good temperature uniformity across the wafers because the incorporation ratio of arsenic and phosphorus is extremely temperature dependent.

Similar results are obtained from DCXD measurements. Across a 2" wafer, variations of the lattice mismatch of only 100 ppm were measured.

Variations in the surface temperature would also affect the doping uniformity. To investigate this, doping experiments were performed using DEZn and SiH$_4$ as dopant sources. Fig. 3 shows a sheet resistivity map of a Si-doped InP sample. The standard deviation of the sheet resistivity is less than 1.5%.

Spatial Step	:	(1000.0,	1000.0)	um
Spectral Range	:	1350.0 - 1550.0		nm
-Step Size	:	0.5		nm
Avg. Wavelength	:	1479.88	nm	
Std Deviation	:	1.26	nm	

Fig. 2: Room temperature PL map of a GaInAsP layer

Number of points	:	25	
Average measurement	:	11.67	ohm/sq.
Max. value	:	11.86	ohm/sq.
Min. value	:	11.30	ohm/sq.
Variation in measurement	:	4.805	%
Std. dev. from average	:	0.17	ohm/sq.
Uniformity of wafer	:	1.44	%

Fig. 3: Sheet resistivity map of a 2" InP:Si wafer

The excellent compositional uniformity with a standard deviation of 1.26 nm confirms that the principle of Planetary Reactors® works for InP based materials as well as for GaAs

Similar uniformities can be obtained for Zn-doped InP (Fig. 4). Thus all requirements for the fabrication of optoelectronic devices concerning doping uniformity are met.
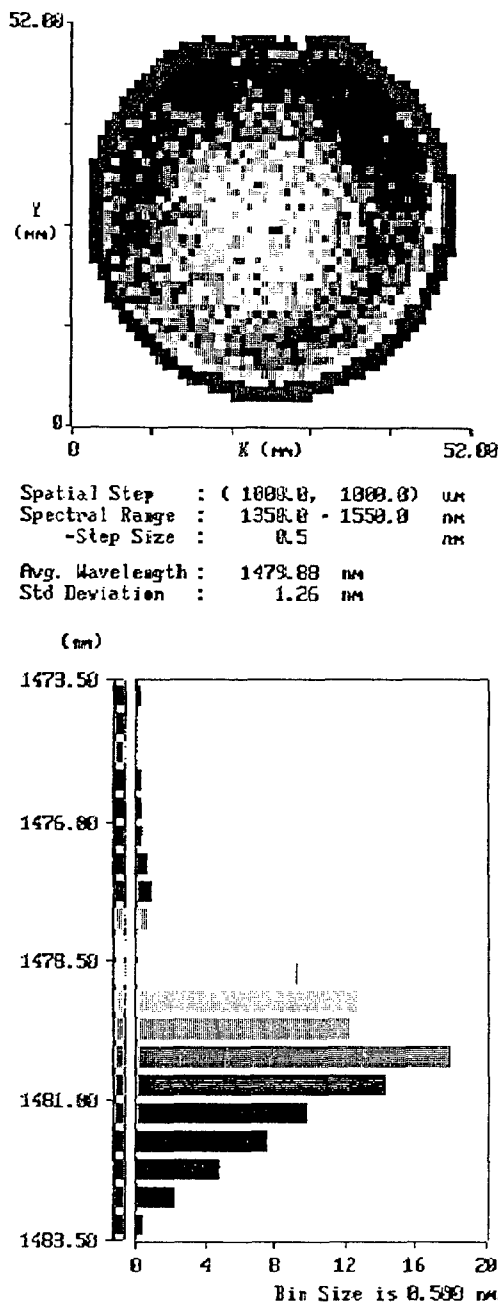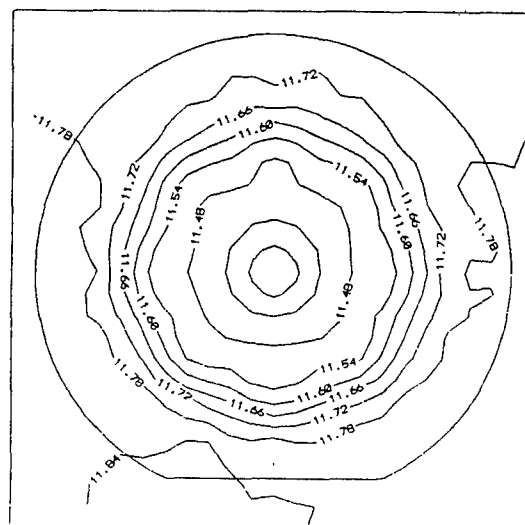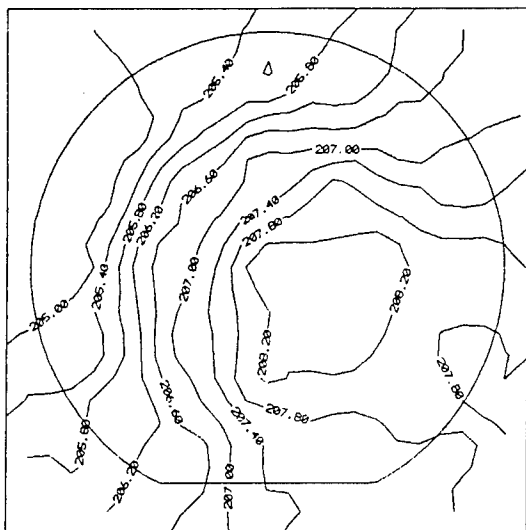
```
Number of points        :  25
Average measurement     :  206.8  ohm/sq.
Max. value              :  208.6  ohm/sq.
Min. value              :  204.6  ohm/sq.
Variation in measurement:  1.915  %
Std. dev. from average   :     1.27 ohm/sq.
Uniformity of wafer     :   .61   %
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Fig. 4: Sheet resistivity map of a 2" InP:Zn wafer

IV. Summary

A multiwafer Planetary Reactor® has been used to grow InP based materials. The reactor allows simultaneous growth on up to 15x2" wafers. PL and X-ray maps reveal excellent compositional uniformities. Sheet resistivity uniformities measured on n-type and p-type material are in the 1 percent range indicating very uniform wafer temperatures. Thickness measurements show homogeneous growth with variations below 2% across a 2" wafer. Thus the Planetary Reactors® are ideal tools for an efficient mass production of long wavelength optoelectronic devices for telecom applications.

V. References

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Present Ability of Commercial Molecular Beam Epitaxy

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Our entry into InP-based materials is the result of increasing demand for higher performance electronic devices. InGaAs/InAlAs High Electron Mobility Transistors (HEMTs) lattice-matched to InP exhibit simultaneously higher charge and higher mobility than similar devices in the GaAs/AlGaAs and InGaAs/GaAs/AlGaAs material systems and are thus well suited for these applications. A typical lattice-matched HEMT, for example, might have a mobility of 11,000 cm^2/Vs with a sheet charge density greater than $2x10^{12}$ cm^{-2}, compared to a 7000 cm^2/Vs mobility for the same charge in a GaAs-based PHEMT. With a psuedomorphic channel in an InGaAs/InAlAs HEMT we have pushed these numbers to 6.5 $x10^{12}$ cm^{-2} at a mobility of 7,200 cm^2/Vs.

While isolated results are important to demonstrate the potential of this material system, a commercial vendor must also demonstrate uniformity and repeatability of both electrical and crystalline properties. A plot of thickness and compositional variation across a typical 3" wafer is shown in Figure 1, demonstrating the inherent uniformity of Molecular Beam Epitaxy (MBE) material. This underlying material uniformity- total variations of 0.1 in mole fraction and 2.6% in thickness- leads to a typical sheet resistance variation of only 0.6% (1-sigma) across the wafer. Typical run-to-run repeatability (without feedback) is less than 1% for the sheet resistance and 0.0024 for the mole fraction, Figure 2. While not required for HEMT growths, we have also developed procedures to maintain lattice-matching for the growth of several micron thick InGaAs layers on InP.

This paper will illustrate the development of our InP market and our capabilities to meet the demands of that market with commercial MBE.
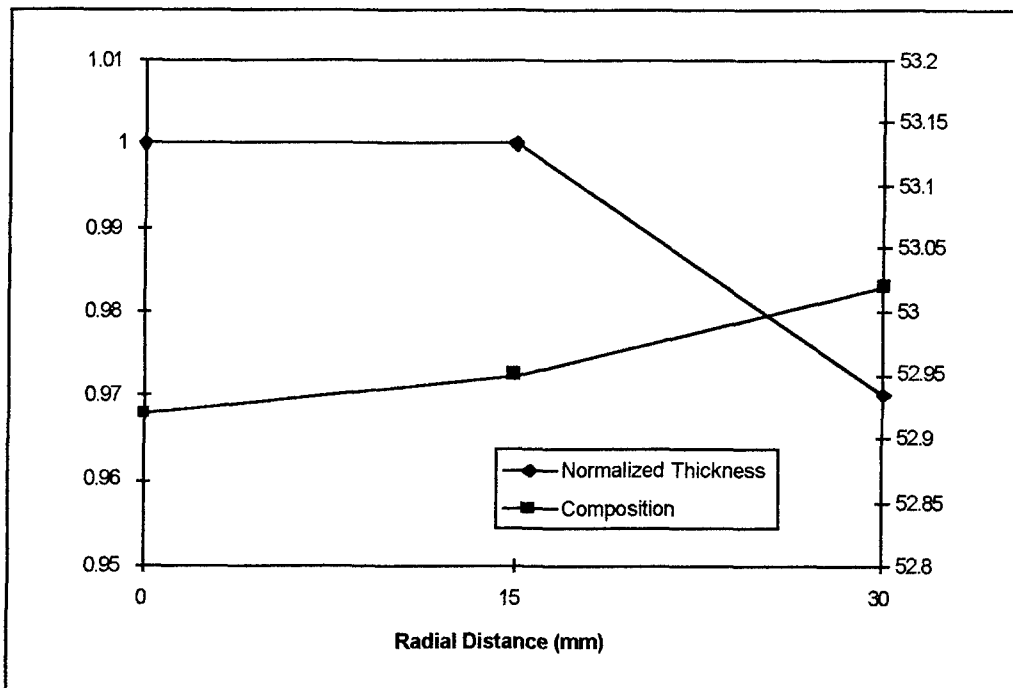
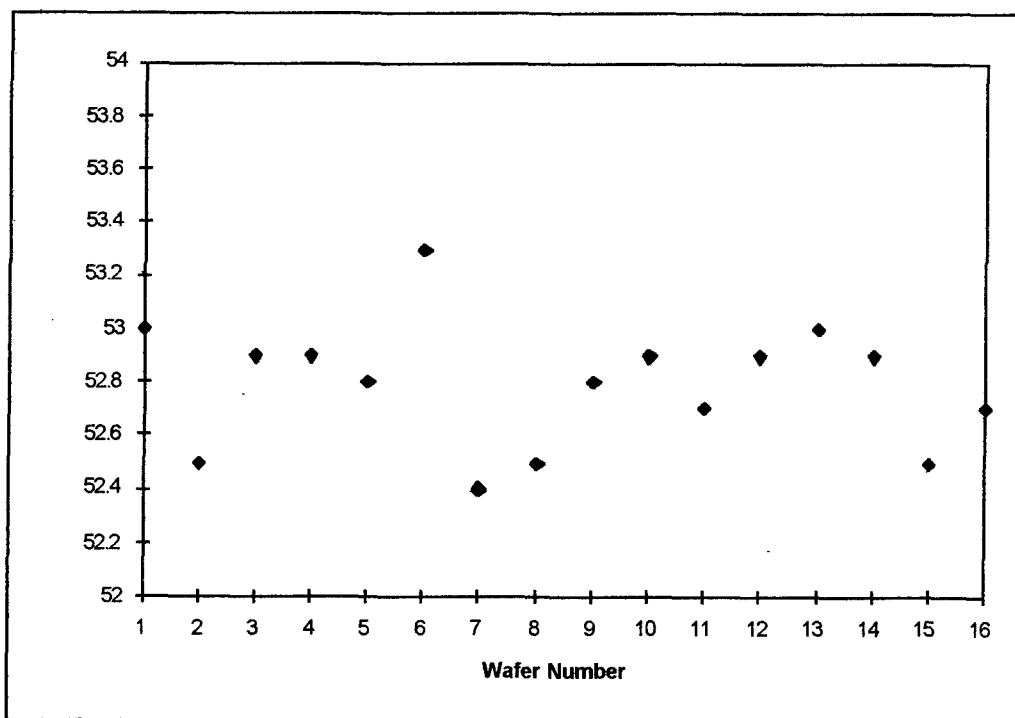**Figure 1: Typical thickness and composition variation across a 3" wafer.**

Figure 2: Run-to-run compositional variation.

Dynamics of the Kink Effect in InAlAs/InGaAs HEMTs

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Abstract

We have carried out pulsed measurements of the *kink effect* in InAlAs/InGaAs on InP HEMTs with nanosecond resolution. Our measurements show that the kink turns on first the higher V_{DS} is. The rate at which the kink builds-up is seen to increase with both V_{DS} and V_{GS}. In general, the kink's characteristic time constant strongly depends on V_{DS} and V_{GS}. Values between 50 ns and 100 μs have been measured in a single device. These data should be instrumental in formulating a hypothesis for the physical origin of the kink.

I. Introduction

InAlAs/InGaAs high electron mobility transistors (HEMTs) show significant promise for low-noise and high-power millimeter-wave applications. A significant anomaly in their behavior is the *kink-effect*, a sudden rise in drain current at a certain drain-to-source voltage that results in high drain conductance and g_m compression, leading to reduced voltage gain and poor linearity. The physical origin of the kink is an issue of considerable contention at this time. Conventional wisdom has attributed the kink effect to traps or their interaction with high-fields or impact ionization (II) [1]-[3]. Recently, simulations [4] as well as light emission, channel-engineering and body contact experiments [5]-[7] have suggested a link between impact ionization and the kink. Indeed, measurements showing direct correlation between II and the kink have been presented [8]. Several models involving II have been proposed including pure II [9], an SOI-like mechanism [7], hole trap charging [10], and *conductivity modulation* of the source [11]-[12].

A new perspective on this problem can be obtained by studying the dynamics of the kink under pulsed operation. Besides providing insight about the origin of the kink, pulsed characterization has been proven to be a good predictor of large-signal high-frequency performance [13]. In this work we have carried out the first experimental time-domain study of the kink effect in InAlAs/InGaAs on InP HEMTs with nanosecond resolution.

II. Experimental

We have designed a pulsed I-V setup able to measure drain response transients with nanosecond resolution. The setup is illustrated in fig. 1 and works as follows: the drain is biased via a DC power sup-
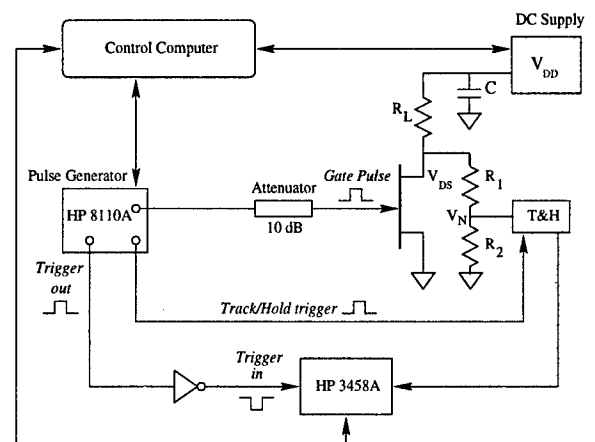
Figure 1: *Pulsed I-V setup used in this work.*

ply (V_{DD}) and a load resistance, R_L ($R_L = 50 \ \Omega$). The current drawn by the transistor is evaluated by measuring the voltage at the drain through the R_1/R_2 voltage divider, which is required to protect the T&H due to its limited maximum input voltage. The gate is pulsed from threshold to the desired gate-to-source voltage, V_{GS}, by a dual pulsed generator (PG). The 10 dB attenuator is used to minimize reflections due to impedance mismatch between the 50 Ω environment presented by the cables and the gate. After a programmable delay (T_d) from the gate pulse, a second pulse is sent to a track-and-hold amplifier (T&H). When triggered, the T&H holds constant the voltage read at node V_N at the instant of the trigger. This allows a voltmeter to read V_N when triggered by the PG. The relative delays between the pulses sent from the PG to the gate, T&H, and voltmeter are independently programmable and have nanosecond resolution. Once $V_N(T_d)$ is known, $V_{DS}(T_d)$ and $I_D(T_d)$ are easily calculated. The whole schematic is implemented in a specially designed high-speed board to mini-
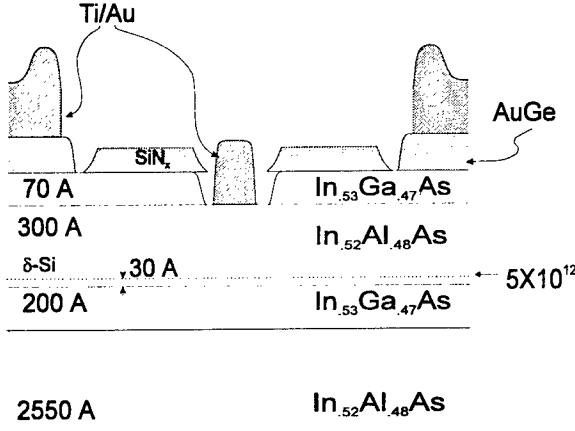
Figure 2: *Schematic cross-section of InAlAs/ In-GaAs single-heterostructure HEMT used in this work.*
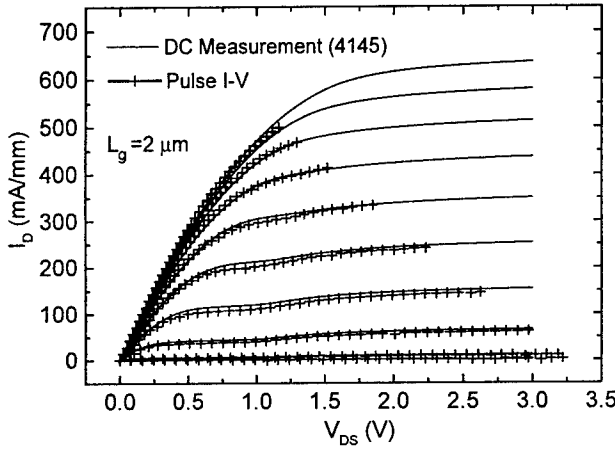
Figure 3: *Pulsed I-V set-up validation: pulsed I-V curves for $T_d \simeq 500\ \mu s$ (crossed-lines) are compared with DC HP-4145B I-V curves (full lines). Good agreement is observed.*

mize wire inductance, crosstalk, and ground bouncing. Measurements are carried out "on-wafer" using coplanar microwave probes. All components have a bandwidth of at least 4 GHz. All measurements have been carried out at room temperature.

In order to trace the whole $I_D - V_{DS}$ plane, for given V_{GS} and T_d, V_{DD} is swept in incremental steps from 0 V to $V_{DD,max}$, where $V_{DD,max}$ is kept below the off-state breakdown voltage. This procedure is then repeated for several values of V_{GS}. For each $V_{DD} - V_{GS}$ pair, T_d samples between 5 ns 500 μs are acquired.

As a vehicle for this study we used a lattice-matched, MBE-grown, InAlAs/InGaAs HEMT schematically illustrated in fig. 2. The layer structure consists of a 2550 Å InGaAs buffer, a 200 Å InGaAs channel, a 300 Å pseudo-insulator, and a 70 Å InGaAs cap. A delta-doped electron supply layer located 30 Å above the channel yields a sheet carrier
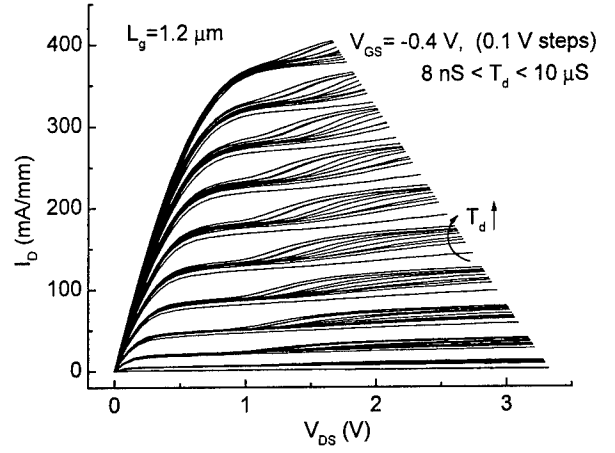
Figure 4: *Pulsed I-V curves for varying delay times, T_d. No kink is seen below $T_d = 10$ ns. For a given V_{GS}, the larger V_{DS}, the earlier the kink turns on and the faster it saturates.*

concentration of 3.6×10^{12} cm^{-2}. Fabrication consists of device isolation via a mesa etch with sidewall recess, a PECVD Si$_3$N$_4$ layer for liftoff assistance, Au/Ge ohmic contacts, a selective gate recess, and Pt/Ti/Au gates and interconnects [8, 12]. Devices with gate lengths 1.2 μm and 2 μm were characterized. The devices exhibit $I_{D,max} = 700$ mA/mm, $g_{m,peak} = 540$ mS/mm, and $BV_{DS(off)} \simeq 5$ V.

The setup was validated by measuring pulsed I-V characteristics for relatively long T_d ($T_d \simeq 500$ μs) and comparing them with DC characteristics obtained using an HP-4145B. Good agreement was observed as shown in fig. 3.

III. Results and Discussion

Pulsed I-V characteristics of an $L_g = 1.2$ μm device for 8 ns $\leq T_d \leq 10$ μs are shown in Fig. 4 for a wide range of V_{DS} and V_{GS}. Two observations can be made: *i*) there is no kink for short T_d (below 10 ns); *ii*) the kink turns-on first and rises faster the higher V_{DS} is. Similar results are obtained for $L_g = 2$ μm devices. These observations are consistent with reports in the literature on output conductance measurements of both InAlAs/InGaAs/InP HEMTs [3] and In-AlAs/InGaAs/InAlAs MESFETs [14] in which no kink is observed at high frequencies despite its prominence at DC.

To further analyze our results, we have defined a "kink" current as follows:

$$\Delta I_D(T_d) =$$
$$I_D(T_d) - [I_{D,prek}(T_d) + g_d(V_{DS} - V_{DS,prek})] \quad (1)$$

where $I_{D,prek}$, $V_{DS,prek}$, and g_d are respectively the "pre-kink" drain current, drain-to-source voltage,

Figure 5: ΔI_D as a function of T_d for different values of V_{DS} but constant V_{GS}.

Figure 6: ΔI_D as a function of T_d for different values of V_{GS} but constant V_{DS}.

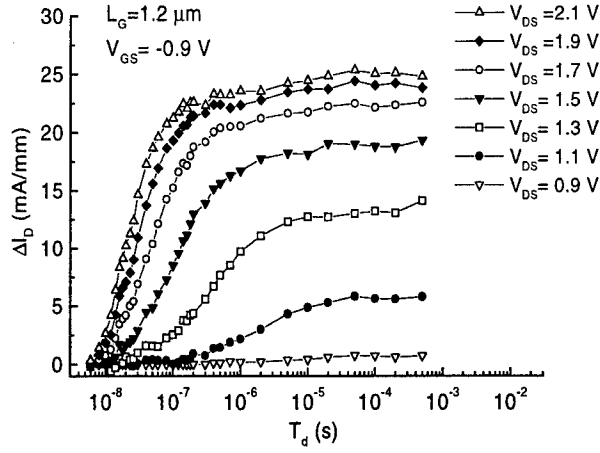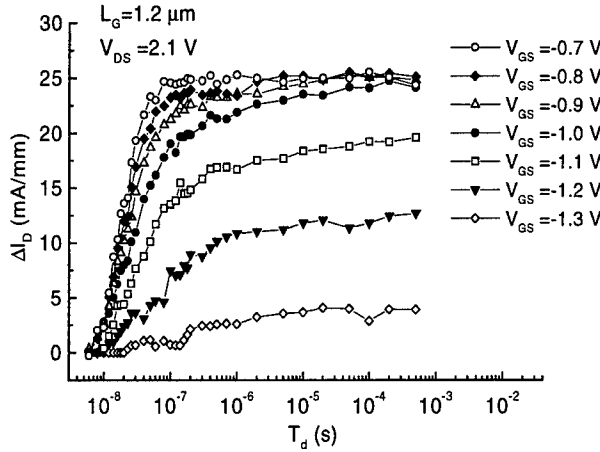and saturation output conductance, and $V_{DS,sat} \leq V_{DS,pre_k} \leq V_{DS}$. In other words, ΔI_D is the drain current exceeding the "pre-kink" saturation drain current after output conductance compensation. Note that, as seen in fig. 4, $I_{D,prek}$ is slightly time dependent. The origin of this is not known. Eq. 1 accounts for this effect.

We plot in fig. 5 ΔI_D as a function of T_d for different values of V_{DS} ($V_{GS} = -0.9$ V). Some peculiar features of the kink can be observed: ΔI_D increases with V_{DS} but seems to saturate for sufficient large values of V_{DS}. This is the standard DC behavior of the kink [8, 12]. Dynamically, the rate at which ΔI_D builds up with time is faster the higher V_{DS} is. Interestingly, the kink's saturation also gets sharper for increasing V_{DS}.

Let us now examine the characteristics of the kink dynamics for different values of V_{GS} and constant V_{DS} ($V_{DS} = 2.1$ V). The following features can be observed: *i)* the DC magnitude of ΔI_D increases
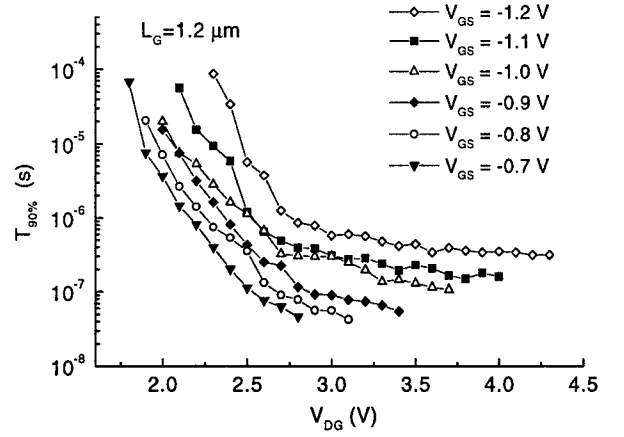
Figure 7: $T_{90\%}$, the time it takes for the kink to reach 90% of its final DC value, as a function of V_{DG} for different values of V_{GS}.

as V_{GS} increases above threshold. *ii)* For -0.9 V $\leq V_{GS} \leq$ -0.7 V, the DC magnitude of ΔI_D is about the same. *iii)* The kink saturates faster the higher V_{GS} is.

The above results show that the kink's characteristic time constant is strongly dependent on both V_{DS} and V_{GS}. This can be seen in a more quantitative way by examining the rise time of the kink, $T_{90\%}$, which we define as the time for ΔI_D to rise to 90% of its final DC value. $T_{90\%}$ is plotted in fig. 7 as a function of V_{DG} for different values of V_{GS}. $T_{90\%}$ is found to be a strong function of V_{GS} and V_{DG} for $V_{DG} \leq 2.8$ V. For $V_{GS} = -0.7$ V, for example, $T_{90\%}$ drops by three decades, from ~ 100 μs down to ~ 50 ns, as V_{DG} increases from 1.7 to 2.8 V. Interestingly, $T_{90\%}$ becomes rather independent of V_{DG} for $V_{DG} \geq 2.8$ V. Note also that $T_{90\%}$ is smaller for constant V_{DG} but increasing values of V_{GS}. Clearly, the dynamics of the kink are not characterized by a single time constant that is independent of V_{DS} and V_{GS}.

The data presented in this work should be instrumented in formulating a hypothesis for the physical origin of the kink effect in InAlAs/InGaAs HEMTs.

IV. Conclusions

In summary, we have carried out for the first time pulsed measurements of the kink dynamics of InAlAs/InGaAs on InP HEMTs in the nanosecond regime. Our measurements show that the kink's characteristic time constant is characterized by two regimes: for small values of V_{DG}, it decreases exponentially with V_{DG}; on the other hand, for large values of V_{DG}, it becomes independent of V_{DG}. Time constants between 50 ns and 100 μs have been observed.

355

Acknowledgments

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Semi-Analytical Analysis for Optimization of 0.1-μm InGaAs-Channel MODFETs TuP23
with Emphasis on On-State Breakdown and Reliability

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Abstract

We have measured and analyzed the bias limitations of our 0.1-μm $In_{.53}Ga_{.47}As$-channel MODFETs. A semi-analytical model allows us to correlate a major degradation mechanism, the increase in drain resistance [1], to impact ionization in the narrow-bandgap channel. We find, as others have [2], that this mechanism also determines the on-state breakdown voltage $BV_{DS}^{(on)}$, and thus limits the operating regime. The modeling predicts the shape of $BV_{DS}^{(on)}$ vs. I_D and shows that the off-state breakdown voltage is irrelevant for practical load-lines. $BV_{DS}^{(on)}(I_D)$ deviates markedly from a constant power locus. In fact, it tends to have a flat minimum $BV_{DS}^{(on,min)}$ (corresponding to maximum impact ionization current) near the I_D of maximum transconductance. $BV_{DS}^{(on,min)}$ becomes the most significant measure of FET breakdown. Most of our device variations have tended to produce a constant-power trade-off of $BV_{DS}^{(on,min)}$ with its associated I_D, in contrast to the non-constant-power locus of $BV_{DS}^{(on)}(I_D)$. The model predicts both trends well.

I. Introduction

The device and circuit characteristics of our 0.1-μm $In_{.53}Ga_{.47}As$-channel MODFET process are described elsewhere [3,4]. The process has been optimized for low noise, high gain and high cutoff frequencies. These are the well-established advantages of this type of FET. However, some important applications require moderately high mm-wave output power which is difficult to produce reliably with short narrow-bandgap MOD-FETs. In this work we measure and analyze the bias limitations for power applications. Section II describes and discusses the experimental observations and the model predictions. Section III describes the model used to analyze the data.

II. R_d Degradation and On-State Breakdown

We have identified the drain resistance R_d as a parameter in our FETs particularly prone to degradation as the drain bias V_D is increased beyond a minimum value [1]. Fig. 1 shows an example. A FET was stressed at room temperature by four times sweeping, with an HP4145B, the gate bias V_G over the modulating regime at a fixed V_D (increased in 50 mV steps). Three features are noteworthy. The source resistance R_s, to which no
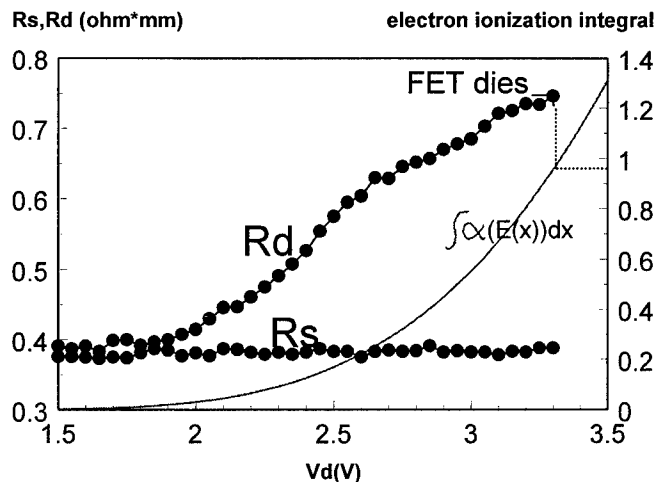
high field region contributes, remains constant. In contrast, R_d, to which the high-field drain region contributes, starts to degrade at the point where the theoretically calculated electron ionization integral I_n deviates noticeably from zero. Finally, at a point where I_n and the multiplication factor M_{np} (Section III) are significant ($\approx$ 1 and 2, respectively), the FET dies abruptly. The gradual degradation over V_D=2-3.5V before it dies probably occurs rather uniformly along the width of the gate. The final destructive breakdown appears, from the observation of a faint subsurface 0.5-2 μm drain-side perturbation, to occur in a filament. This would be similar to MESFETs [5].

In the following we do not record the gradual R_d degradation. Instead we sweep V_D at a fixed V_G, using the HP4145B long integration time and a 100 Ω "buffering" series drain resistor, until the FET dies. Fig. 2 shows burnout biases (I_D, $BV_{DS}^{(on)}$) for 0.1-μm $In_{.53}Ga_{.47}As$-channel MODFETs with two gate widths (2x11 and 2x75 μm) across a wafer, at various current levels. Superimposed are theoretical curves showing loci of constant DC power dissipation, constant predicted secondary current $(M_{np}-1)\cdot I_D$ generated by impact ionization, maximum drain current, and three potential load-lines. Several things are noteworthy. First, the burnout biases do not follow a constant-
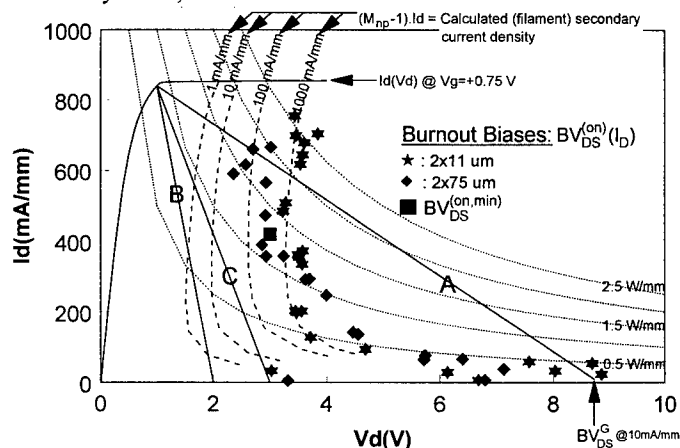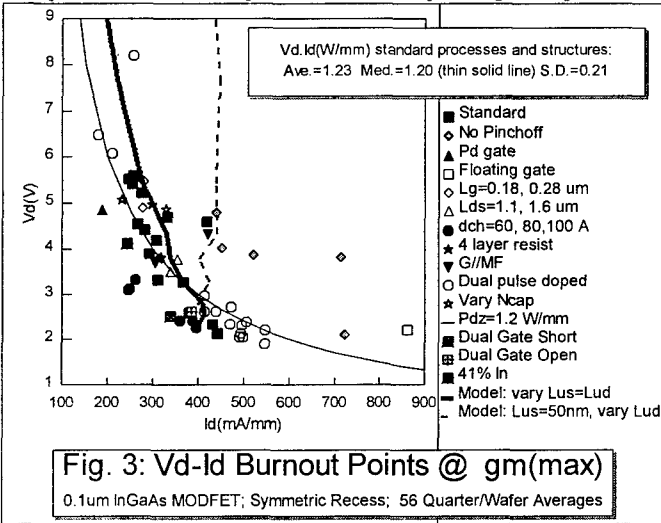
Rs,Rd (ohm*mm)   **electron ionization integral**

Fig. 1: Bias-induced room temperature R_d degradation

Fig. 2: Measured burnout biases in a theoretical context (see text).

power curve. Instead, the 22 µm FET traces almost perfectly the locus of $(M_{np}-1) \cdot I_D$ =1000 mA/mm. The 150 µm FETs deviate somewhat from this pure behavior by what is natural to interpret as a small thermal burnout component (wafer thickness = 500 µm). Nevertheless the adherence to the impact ionization trends is striking. It is possible that the thermal component is due to the temperature dependence of the ionization coefficient [6]. The trend is very similar to the onset, in an InAs-inserted channel MODFET, of kink and gate hole current at low temperature [7]. These effects were shown to be related to impact ionization. The trend is very different, however, from the GaAs MESFETs in [5] where the pulsed (non-destructive) on-state breakdown follows a constant 3.4 W/mm power locus. For the higher current levels our In.53Ga.47As MODFETs reach 2.5 W/mm, but because of the larger fields at lower current, impact ionization limits the power to much lower values there. The presence of impact ionization is clearly evident in the gate current [1]. The drain current, however, only rarely shows a significant upturn [2] before the FET breaks down. This is similar to [5], despite the different measurement technique used and is probably in large part due to the filament nature of the breakdown. To estimate the total secondary current, $(M_{np}-1) \cdot I_D$ in Fig. 2 should be multiplied by the filament width ($\approx$ 1 µm).

As a consequence of these observations, the oft quoted *off*-state breakdown voltage is irrelevant for practical loads. Consider load-line A (4.9 V drain bias) in Fig. 2 which is based on $BV_{DS}{}^G$ [8] measured at 10 mA/mm. Although the mm-wave output power would be an impressive 825 mW/mm, the FET would be biased in (and the voltage would swing further into) the region of destructive breakdown. For reliable operation one should back off to load-line B (1.5 V drain bias) corresponding to 107 mW/mm. This allows for the 1.5 V range of R_d degradation in Fig. 1. Using the less conservative loadline C (2 V drain bias), we have, at 60 GHz, measured the expected 214 mW/mm saturated output power.

Note that $BV_{DS}{}^{(on)}(I_D)$ has a flat minimum near the I_D ($\approx I_D{}^{(max)}/2$) of maximum transconductance. $BV_{DS}{}^{(on,min)}$ becomes the most significant measure of FET breakdown. We focus on this parameter in our optimization attempts. Fig. 3 represents a

Fig. 3: Vd-Id Burnout Points @ gm(max)
0.1um InGaAs MODFET; Symmetric Recess; 56 Quarter/Wafer Averages

large collection of experimental data. As the legend suggests, the MBE structure, process geometry, orientation and biasing scheme were varied widely. It is striking how relatively close the experimental burnout points hug the 1.2 W/mm locus, independent of the experimental variations. This contrasts to the strong deviation from constant power loci of burnout points over a wafer when the current from FET to FET is varied by varying V_G (Fig. 2). Beside backside (dual) doping, the main parameter determining the maximum current (and that at maximum g_m) in our FETs is the amount of source-side lateral recess L_{us}. In our symmetric recess the drain-side value L_{ud} is the same. The thick solid line in Fig. 3 is the model prediction for a 50 to 360 nm simultaneous variation in these parameters. We used the $(M_{np}-1) \cdot I_D$ = 1000 mA/mm criterion suggested by Fig. 2. The model predictions follow quite well (without fitting) the standard data points, and suggest a more complex tradeoff than constant power. Note, of course, how much better an asymmetric recess would be. For the dashed line we kept L_{us} to the minimum value while increasing only L_{ud}. We could then, with no tradeoff in current, increase the breakdown voltage. At some point, however, the frequency performance would suffer [9].

III. Semi-Analytical Model for Short Gate MODFETs

For our MODFET development we have historically relied on analytical and semi-analytical models for device optimization, even as gate lengths have shrunk from 1 µm [10] to 50 nm [11], and the material structure has become more complex [3,4]. Full numerical modeling has mostly been used for the one-dimensional MODFET 2DEG charge control $n_s(V_G)$ [12]. The non-linear characteristic of $n_s(V_G)$ is well represented by an integrable function involving $tanh(x)$ [13]. The field-dependent mobility and velocity saturation/overshoot is well represented, even for very short gates [11], by an analytical two-piece $v(E)$ curve that saturates at the steady-state *peak* velocity v_{sat} ($2.8 \cdot 10^7$ cm/s for In.53Ga.47As). The only modification for short gates is a reduced L_g-dependent mobility [11] to account for a minimum required electron energy for saturation. A MESFET equivalent (for easier depiction of carrier depletion) of the essential geometry of our nominal MODFET is shown in Fig. 4, together with the solution for channel potential $V_c(y)$ and drift field $E_c(y)$ for V_D=1.5 V and maximum g_m. The source- and drain-side caps have been removed laterally for $L_{us} = L_{ud}$ =100 nm by the vertically selective recess etch [4]. The gradual part of the channel ($y<y_s$) is solved as described in [13]. Since the days of the original model, however, gates have shrunk to a point where the laterally etched nonlinear access regions adjacent to the gate have become increasingly important to the performance, and can no longer simply be treated as linear resistors. In fact, the velocity-saturated region typically extends as far beyond the gate (ΔL_x) as underneath the gate (ΔL_i), and the field is larger beyond the gate. For $y>y_s$ we solve the following equation which introduces the effective gating voltage $V_{surf}(y)$ exerted by either the free surface or the gate (depending on y)

$$\frac{d^2 V_c}{dy^2} = \frac{[V_G - V_c(y_s)] - [V_{surf}(y) - V_c(y)]}{a^2}. \tag{1}$$
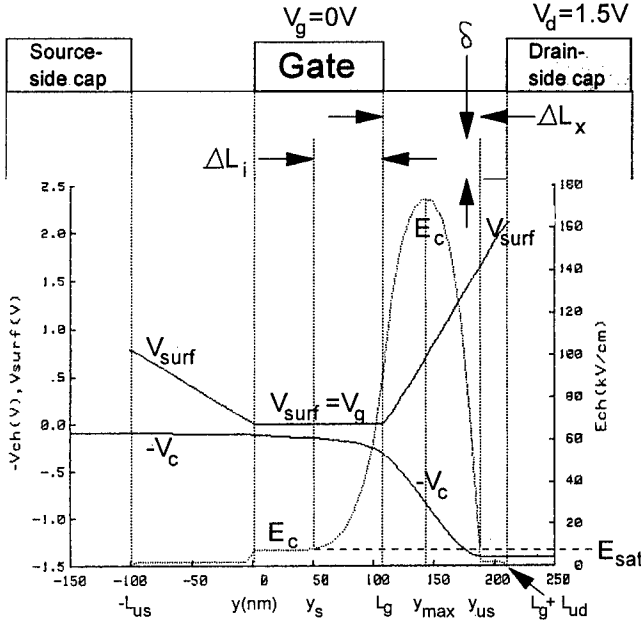
Fig. 4: Simplified FET geometry with modeled field and potential profiles

$V_c(y_s)$ is a function of V_G and I_D [13]. Equation (1) represents the mixed charge control by the surface (gated or not) and the gradient in lateral field $E_c(y)$. The parameter a^2 thus depends on y through n_s and the effective channel thickness δ [11]. However, we make the equation analytically solvable by assuming a constant a^2. Its value emerges when considering the situation $V_g-V_c(y_{dc})=V_g^{(min)}$, defined by $n_s(V_g<V_g^{(min)})=0$ [13], when V_{surf} loses control over the channel charge, and n_s is totally supported by dE_c/dy. In this regime

$$\frac{d^2V_c}{dy^2} = \frac{I_D}{W\varepsilon\delta v_{sat}}.$$ (2)

At the point $y=y_{dc}$ of "deconfinement" under the gate, we set the left hand sides of (1) and (2) equal (for continuity also of dE_c/dy). We arrive at

$$a^2(V_G) = \frac{V_G - V_G^{(min)} - V_c(y_s)}{I_D^{(sat)}(V_G)} W\varepsilon\delta v_{sat}.$$ (3)

In saturation, even at the point of deconfinement (not reached at the drain biased used in Fig. 4), I_D is not much larger than its value $I_D^{(sat)}(V_G)$ at saturation. We have thus, in (3), used this current, which emerges from the solution to the gradual channel [13]. Like Hariu et al. [14] we assume a linear $V_{surf}(y)$. This allows for an analytical solution to (1), and the determination of interesting points such as y_s, y_{us} (unsaturation), y_{rc} (reconfinement) and y_{max} (maximum field; $> y_{rc}$) [11]. But we also realize that, at $y=L_g+L_{ud}$, V_{surf}, being an effective gating potential, is not equal to $V_D-R_dI_D$, but rather this value plus an effective gate voltage ($\approx +0.7$ V) necessary to appropriately fill the channel under the cap. The approach boils down to calculating $V_c(L_g+L_{gd})$, and making sure, with a root-finding method, that this is equal to $V_D-R_cI_D$ at the drain contact. The assumption of a linear $V_{surf}(y)$ is obviously questionable, as measurements of the surface potential [15] show. Nevertheless, the approach is

necessary for an analytical solution, and clearly is an improvement over analytical approaches that ignore the surface altogether. The high-field domain in Fig. 4 is in our model the result of the free surface gradually restoring the channel from its pinched-down state under the drain-side edge of the gate. This differs from the common view of a MESFET having a transport (rather than surface) induced stationary Gunn domain beyond the gate. Fully numerical MODFET modeling [16] appear to validate our approach.

In the source-side access region the fields are typically low, but the free surface still has an important current-limiting effect [17]. Because of lateral charge support, however, this is not a hard limit. We account for the non-linear part of the source access region by solving for $V_c(y)$ (to second order in y)

$$I_D = W\left(qn_s(V_G^{(ugt)}) + \varepsilon\delta\frac{d^2V_c}{dy^2}\right)\frac{\mu\frac{dV_c}{dy}}{1 + \frac{\mu}{v_{sat}^{(ugt)}}\frac{dV_c}{dy}}.$$ (4)

The first term in the brackets accounts for the limited amount of electrons allowed by the surface. The effective gating voltage $V_G^{(ugt)}$ ("ugt" for UnGated Trough) is set to $+0.26$ V. 0.1 V comes from the ungated AlInAs having approximately this amount less band bending than when gated [18]. 0.16 V comes from the Pt gate sintering 25 A into the semiconductor, making the adjacent AlInAs surface less current-limiting. The second term in the bracket models the additional space-charge limited current allowed by the channel. This is particularly important for enhancement-mode operation. The last factor, outside the brackets, allows for field-dependent mobility and velocity saturation [17]. The approach correctly predicts the maximum current for our standard FET (Fig. 2) to be considerably smaller than the $qWn_{so}v_{sat}$ one would expect were the free surface not accounted for. For FETs with larger L_{us} we vary $v_{sat}^{(ugt)}$ smoothly from the peak velocity v_{sat} to the much lower high-field saturated velocity $(6.5\cdot10^6$ cm/s) as L_{us} varies from 0 to ∞. An exponential rate of change is picked to produce the low (300 mA/mm) measured current in the extreme case of $L_{us}=L_{ud}=850$ nm. Only when $y_s<0$ ($V_G\rightarrow V_g^{(min)}$, V_D large) will the source-side $V_{surf}(y)$ be used in the calculation.

In Section II we used the model to predict the level of impact ionization expected from the field profiles. Given the semi-analytical nature of the model we cannot include this effect self-consistently. This would require a fully numerical model [19]. We do use the complete field profile, rather than an average field [20]. This is important given the nonlinear characteristics of the electron impact ionization coefficient $\alpha_n(E_c)$ [20]. We base impact ionization on the local field in the classical way

$$I_n = \int_{-L_{us}}^{L_g+L_{ud}} \alpha_n(E_c(y))dy.$$ (5)

If one makes the assumption $\alpha_p=k_p\alpha_n$ ($k_p=0.5$ [21]) the double integral I_{np} for impact ionization [19,21] is significantly simplified:

359

$$I_{np} = \frac{1 - e^{-(1-k_p)/l_n}}{1 - k_p}.$$ (6)

Rather than settling for a lower and upper bound [21], this expression explicitly accounts for the different ionization coefficient for holes. The electron multiplication factor is

$$M_{np} = \frac{1}{1 - I_{np}}.$$ (7)

Having calculated $E_c(y)$ and $V_c(y)$, we can also estimate the tunneling reverse gate current I_G [22] using the (transverse) field at the gate metal approximately given by

$$E_{t_g}(y) = \frac{qn_d}{\varepsilon} - \frac{V_G - V_{th} - V_c(y)}{d_{wb}} + E_{sat}\frac{\sinh(\beta(y - y_s))}{\sin(\beta d_{gc})},$$ (8)

where

$$\beta = \frac{\cosh^{-1}(E_c(L_g)/E_{sat})}{L_g - y_s}.$$ (9)

d_{wb} is the thickness of the wider-bandgap AlInAs Schottky-barrier layer, d_{gc} the slightly larger gate-to-channel distance, n_d the sheet donor concentration, and V_{th} the threshold voltage (slightly larger than $V_G^{(min)}$). The I_n and I_G integrals are calculated numerically with Simpson's formula.

Fig. 5 shows the predicted drain current for our nominal FET. The onset of impact ionization follows the trend discussed in Section II. Even close to threshold, corresponding to off-state breakdown, the tunneling gate current (even when augmented with impact ionization in AlInAs) is negligible, consistent with [2]. It would hardly be visible if plotted in Fig. 2. At BV_{DS}^G it is predicted to be less than a tenth of the 10 mA/mm that defines this off-state breakdown voltage. Impact ionization is negligible below 2 V and does not explain the normal (not kink related) output conductance g_d [20,21]. δ affects g_d, and can be used for fitting [11], but in the present work we left δ at its nominal 12.5 nm value. Above 2 V, where Fig. 5 predicts (and the measured gate current confirms [1]) impact ionization, it only rarely shows up in the measured I_D. There are several possible reasons for this. The increased filament nature of the secondary current as breakdown is approached was mentioned in Section II. In addition, the secondary current is smaller than predicted because of recombination and field redistribution caused by the
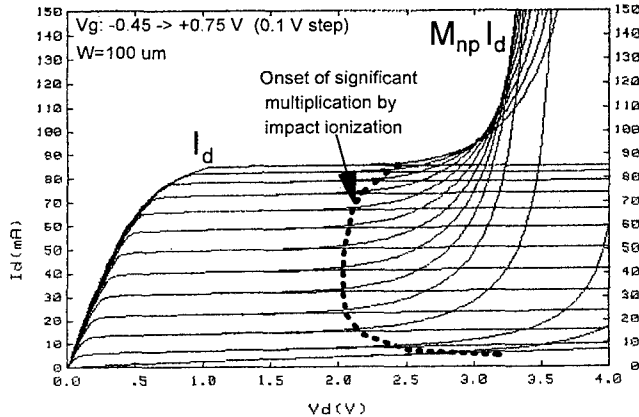
additional carriers [21], as well as from real-space transfer. Electron heating and negative differential mobility, if significant, reduce the primary current. Using the local electric field, rather than the carrier energies, affects the predictions quantitatively, but not qualitatively [19].

IV. Conclusions

A semi-analytical model has helped us analyze the effects of impact ionization on the breakdown characteristics and reliability of our 0.1-μm In$_{.53}$Ga$_{.47}$As MODFETs. Rather than a full-blown numerical model accounting for all conceivable physics, or a fit-based CAD model for circuit design, it is a guide for a device or process engineer working in a lab environment, optimizing real FETs. The model captures the essential device physics, as confirmed by reverse modeling [11], and its predictions agree well with measurements. In the present paper we have found that while impact ionization does not explain the magnitude of the output conductance, it causes these FETs to degrade, and determines their on-state breakdown. Off-state breakdown and gate tunneling appear to be of only secondary importance.

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Fig. 5: Modeled drain characteristic of standard FET

High Performance InGaP/GaAs HBTs with AlGaAs/InGaP Emitter Passivated Ledges for Reliable Power Applications

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Abstracts

High performance InGaP/GaAs HBTs have been demonstrated with novel AlGaAs/InGaP emitter passivated ledges on the extrinsic base region to achieve good device reliability. Using this technology, our X-band HBTs fabricated have been under stress test for ~ 2500 hours with an initial junction temperature of 200°C and a J_C of 50 KA/cm^2 and there is only ~ 5% degradation observed with no early catastrophic failure. In terms of power performance, our X-band HBT power amplifiers achieved typical output power of 1.32 W CW (4.42 W/mm), 60% power added efficiency, 70.6% collector efficiency and 8.18 dB associated gain at 10 GHz.

I. Introduction

High speed [1] and high reliability [2] InGaP/GaAs heterojunction bipolar transistors (HBTs) have been reported previously. The best reliability data [2] reported is 10^6 hours mean time to failure (MTTF) at a junction temperature (Tj) of 200° C with a collector current density (Jc) of 6×10^4 A/cm^2. Meanwhile an effective passivation ledge [3,4] has been proven to be necessary and critical to HBT's reliability. To contact the thin base layer with good passivation, a diffusive base metal scheme such as Pd/Zn/Pt/Au was deposited on the wide bandgap InGaP passivation emitter material and a sequential annealing process allowed metal penetrating through the thin InGaP passivation layer and contacting to the base layer. The approach offered very effective passivation but a stringent metal scheme and annealing condition were required to make a good base contact with a low contact resistance and without punching through the base layer. Therefore, a non-alloyed base metal directly contact to the base layer is preferable to achieve a low base contact resistance for high frequency applications.

In this study, HBTs with a novel AlGaAs(graded)/InGaP passivation ledge design is proposed and demonstrated using a non-alloyed base metal scheme directly contact to the base layer. As shown in Fig.1, the proposed AlGaAs(graded)/InGaP junction structure forms a hot electron launcher to enhance device speed by reducing emitter charging time [5] and also provides an additional barrier to block minority carriers from injecting into the surface states of the extrinsic base region to achieve good passivation and reliable devices.

This paper starts from the description of experimental procedures and then addresses device performance including dc, microwave and X-band power performance. Small-signal microwave performance is also compared for the HBTs with the AlGaAs/InGaP and a conventional InGaP emitter layers. Then 2500-hour device reliability test data is presented. Finally, a brief summary concludes the paper.

II. Experiment

The wafers were grown by metal-organic chemical vapor deposition (MOCVD) using tetriarybutylarsine and tetriarybutyl-phosphine as group V sources. The n-type and p-type dopants were Si and C, respectively. The typical active regions of the HBTs consist of
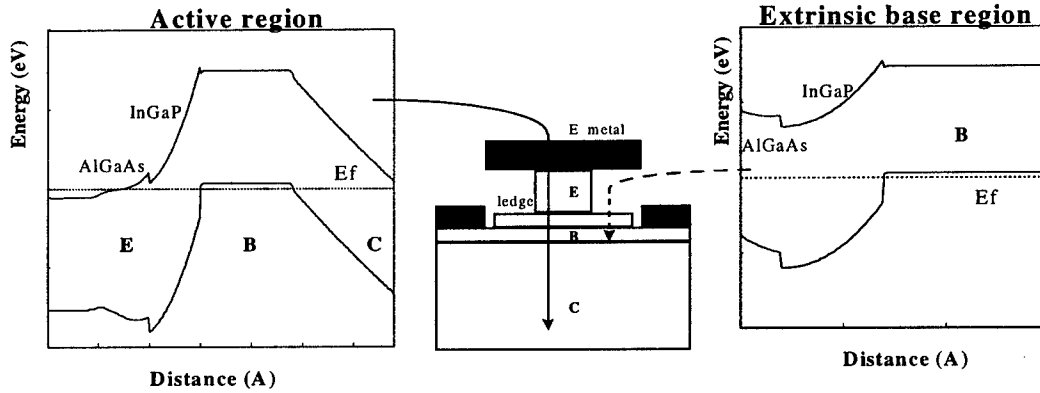
Fig. 1 Equilibrium band diagrams in the active and extrinsic base regions. A hot electron launcher is formed by the AlGaAs/InGaP heterojunction to reduce emitter charging time. The AlGaAs/InGaP heterojunction also provides an additional barrier to block minority carriers from injecting into the surface states.

an n-InGaP or AlGaAs(graded)/InGaP emitter layer doped at ~ 5 x 10^{17} cm^{-3}, a 700 Å p-GaAs base layer doped at 4 x 10^{19} cm^{-3} and a ~ 0.5 μm or 1 μm n-GaAs collector layer doped at 2 x 10^{16} cm^{-3}. The 0.5 μm collector layer is designed to evaluate small signal devices and 1.0 μm one is for power and reliability devices. The emitter passivation ledge was fabricated using our standard ledge process and it can be non self-aligned or self-aligned to the emitter metal, as shown in Fig. 2. The InGaP/GaAs HBTs were fabricated using our standard process [6]. First, conventional photolithography was adopted for metal contact lift-off and Ti/Pt/Au (or Pt/Au) was deposited for emitter and base contacts. Then AuGe/Ni/Au was used for collector ohmic contacts and air-bridges were plated for interconnect metals. DC characteristics were measured first then small signal on wafer S-parameter measurements were performed from 0.1 GHz to 50.1 GHz for extrapolating f_T and f_{max}. X-band power performance was measured at 10 GHz.
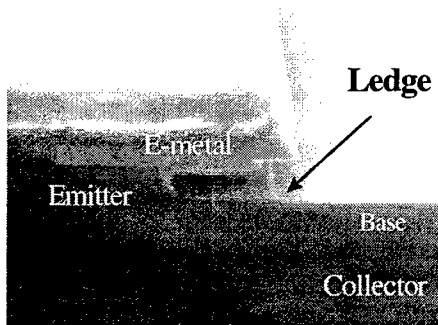

Fig. 2 A typical SEM picture of a self-aligned AlGaAs/InGaP emitter passivated ledge.

III. Results and discussions

There is little difference in dc characteristics for the HBTs with the AlGaAs/InGaP or InGaP emitter layers. The typical common emitter I-V characteristics showed a Vce offset voltage of ~ 0.17 V and a knee voltage < 0.5 V at a collector current density (J_C) of 1 x 10^4 A/cm^2 for a device with an emitter area of 4 x 60 μm^2. For the same devices, the ideality factors were nc~1.01 and nb~1.16 from the Gummel plots.

However, in terms of base contact resistance, the HBTs with an InGaP emitter layer had Pt/Au base metal on top of the InGaP layer and the typical contact resistivity (ρc) was ~ 5 x 10^{-5} Ωcm^2 range. For the HBTs with an AlGaAs/InGaP emitter layer, Ti/Pt/Au was used as base metal directly contact to the GaAs base layer and the typical ρc is < 5 x 10^{-6} Ωcm^2 range. The difference in base contact resistance can be attributed to (1) non-optimization of the Pt/Au base metal or (2) the wide bandgap InGaP emitter layer. If further optimization is pursued, the Pt/Au or other base metal scheme may provide a better base contact resistance, however long term stability and punching through the base layer are still big concerns.

In terms of small-signal performance, the HBTs with the AlGaAs/InGaP emitter layer and an emitter area of 3x10 μm^2 showed a better current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). As shown in Fig. 3, the f_T(H_{21}) and f_{max}(Gmax) reach ~ 70 GHz and 120 GHz for this type of HBTs. On the other hand, for the HBTs with a conventional InGaP

362

emitter layer, the $f_T(H_{21})$ and $f_{max}(Gmax)$ only reach ~ 60 GHz and 85 GHz. The better performance for the HBTs with the AlGaAs/InGaP emitter layer can be attributed to several reasons. First, the AlGaAs grading layer provides a lower series emitter resistance. For different growth conditions, the InGaP layer grown could be ordered, disordered or partially disordered. High growth temperature tends to produce an ordered InGaP layer which has a ΔE_C of 0.03 eV with a GaAs layer. On the other hand, disordered InGaP usually results from a lower growth temperature and the ΔE_C is ~ 0.22 eV. For the growth temperature used (nominal 530°C), partially disordered InGaP layer was obtained and the ΔE_C is between 0.03 eV and 0.22 eV. Therefore, the grading AlGaAs layer can reduce a significant barrier and emitter series resistance. The Al fraction was also carefully chosen such that the ΔE_C provide a hot electron emitter launcher and the excess energy is not higher than the upper valley energy to avoid intervalley scatterings. Moreover, a lower base contact resistance and higher f_T result in the better fmax seen from the HBTs with the AlGaAs/InGaP emitter layer.
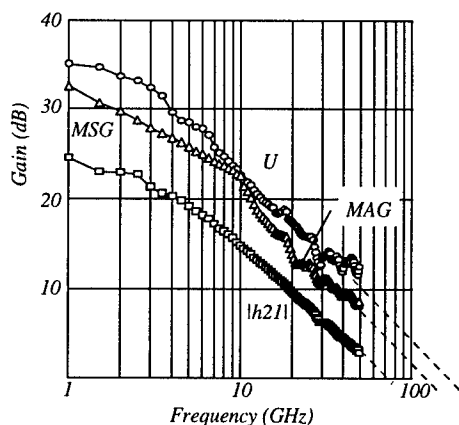

Fig. 3 Small signal gain versus frequency for an HBT with an emitter area of 3 x 10 μm^2 and AlGaAs/InGaP emitter layer.

The small-signal performance, especially the Gmax, is significantly better for the HBTs with the AlGaAs/InGaP emitter layer. Therefore, power measurements were also performed for the HBTs with a 0.65 μm self-aligned ledge width. As shown in Fig. 4, the typical output power achieved is ~ 1.32 W CW (4.42 W/mm), 60% power added efficiency,

70.6% collector efficiency and 8.18 dB associated gain at 10 GHz for power cells with an emitter area of 10 (fingers) x 2.2 (width) x 30 (length) μm^2. This result is comparable to our typical base-line X-band AlGaAs/GaAs HBT power unit cells with an AlGaAs passivation ledge.
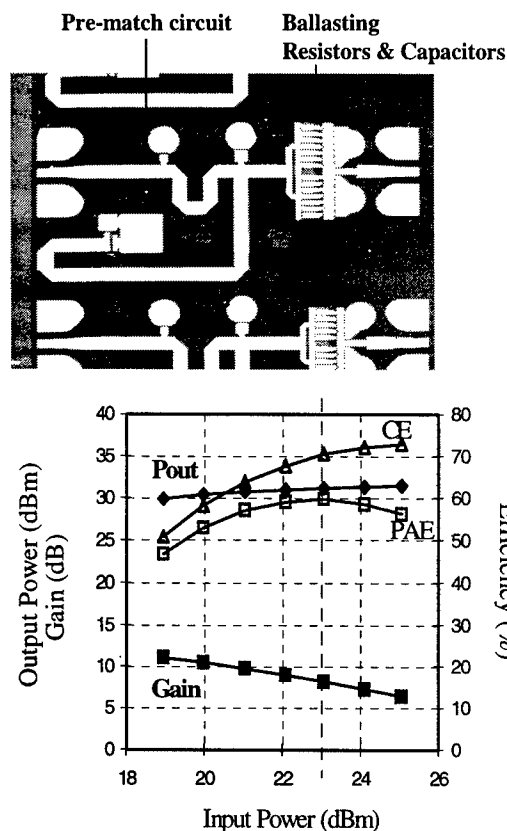

Fig. 4 X-band power unit cell layout and X-band power performance for the HBTs with 0.65 μm self-aligned AlGaAs/InGaP emitter passivated ledges.

As mentioned, the advantages of using the AlGaAs/InGaP emitter layers offer better device performance and good passivation for reliable devices. As shown in Fig. 1, the conduction band alignment is type-II between the AlGaAs and InGaP layers. In the extrinsic base region, the additional conduction band discontinuity, ΔE_{C1}, helps to block minority carriers (electrons) from injecting into the surface states to reduce surface recombination. It is believed that extrinsic base surface recombination enhances defect formation and device degradation. In the past, surface passivation techniques just used a thin depleted

363

wide-bandgap material to block minority carriers. Such a thin wide-bandgap material needs to be completely depleted to prevent lateral conduction. However, if this layer is too thin, surface electric field will reduce the effectiveness of the passivation layer. The proposed new design will offer more freedom to achieve an effective passivation ledge. In this design, the minority carriers are not only blocked by the surface field but also impaired by the ΔE_{C1} between the AlGaAs and InGaP layers.

For reliability test, our single-finger (~ 2 x 60 μm^2) X-band HBTs with the AlGaAs/InGaP passivation ledges were biased at an initial junction temperature ~ 200° C and a J_C of 5 x 10^4 A/cm^2. For the best set of InGaP HBTs, they have been under test for 2500 hours as the paper is being written and there is only averaged 5% degradation observed with no early failure as shown in Fig. 5. Devices without emitter ledge passivation failed in a relatively shorter time as addressed in Ref. [4].
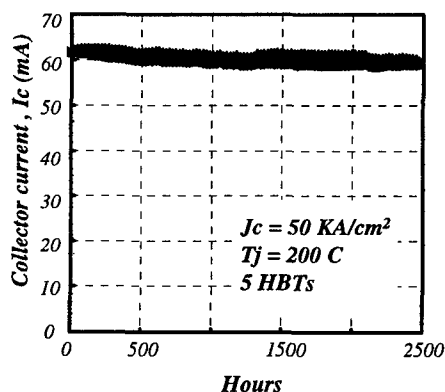

Fig. 5. X-band InGaP HBTs reliability test at an elevated Tj= 200 C and Jc =50 KA/cm^2 for 2500 hours with no early failure.

III. Conclusions

In conclusions, to our knowledge, this is the first report in the literature to implement the AlGaAs/InGaP ledges in InGaP/GaAs HBT circuits successfully. DC, small-signal and large-signal X-band power performance are reported along with good device reliability.

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Mechanism and structural dependence of kink phenomena in InAlAs/InGaAs HEMTs

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I. Introduction

InAlAs/InGaAs HEMTs have demonstrated excellent high-frequency, high-gain performance [1]. Although they are most promising devices for high-speed and high-frequency integrated circuits, some drawbacks have to be eliminated. One of these is the kink phenomenon, an anomalous increase in drain current at a certain drain-to-source voltage. Many studies of the kink in InGaAs-channel HEMTs have suggested that the impact ionization and the trap [2,3] are responsible for the kink. According to the models used in these studies, the appearance of the kink depends on the growth condition of the epitaxial layers. In our experience, however, the kink can have different characteristics even in devices on the same wafer, so it must be related to process conditions as well as the crystal growth. A model in which a parasitic source resistance in a side-etched region, formed during a gate-recess etching, is modified by the holes generated by impact ionization has recently been suggested [4] and improved [5]. This model can explain the process dependence by means of a dispersion of the side-etching length. However, the mechanism by which the parasitic source resistance changes is not completely clear yet, so no model has provided a clue about how to eliminate the kink.

The aim of this study is to find out the relationship between the kink and the structure of the InAlAs/InGaAs HEMTs, or in other words, what the main parameters affecting the kink are. Two-dimensional device simulations were performed for this purpose, in which impact ionization and surface states were considered. For the impact ionization, an improved model which takes into account the non-local effects was used for accurate estimation of ionization coefficients. The surface states in the side-etched region, expressed using a deep-level trap, were also necessary to represent the kink in the device simulation.

II. MODELING FOR DEVICE ANALYSIS

The device simulation system is based on the drift-diffusion model [6]. In this paper, the description of the physical model is focused in the two important parts for the simulation: impact ionization and surface pinning.

A. Impact ionization

An impact ionization coefficient, α, is generally given as a function of the electric field. When an FET is operated in the saturation region, however, most of the voltage drop is distributed between the gate and drain of the FET, so the extent of the high-field region is sometimes comparable to the energy relaxation length of carriers. Therefore, α depends on the field on the current path as well as the field at the present point. To consider such a non-local effect, the carrier temperature, T_n, is first obtained from the electric field $\mathbf{F}$. Since the energy regime we have interest here is high enough that carrier velocity reaches the saturation regime, the carrier drift velocity, $\mathbf{v}$, is assumed to be constant. In this condition, T_n can be calculated [7] as

$$T_n - T_0 = \frac{2}{5}\frac{q}{k_B}\int_{-\infty}^{s}\frac{-v\cdot F}{v}e^{-\frac{3}{5}\frac{s-s'}{v\tau}}ds', \qquad (1)$$

where s is the length of the current path, T_0 is the lattice temperature, and τ is the energy relaxation time for the carrier. Once T_n is obtained, α is given as

$$\alpha = A\exp\left(-\frac{E}{k_B(T_n - T_0)}\right), \qquad (2)$$

A and E are determined from the experimental data [8]. The parameters used in the simulation are listed in Table I.

B. Surface pinning

The Fermi level pinning at the surface of the side-etched region causes the surface depletion by which the density of the channel electron is decreased. Assuming that the density of surface states is so large that the change in the surface potential is small

enough when the trap charge is changed, the carrier trapping in the surface states is expressed like a one-level acceptor-like trap described by Shockley-Read-Hall model. The charge density of the trap, Q_{ss}, is given as follows:

$$Q_{ss} = -qf_T N_T, \qquad (3)$$

where N_T is the trap density, f_T is the percentage of the traps occupied by electrons, determined by the energy level of the trap, E_T. Unfortunately, little data is available on the surface states of InAlAs, so E_T and N_T were regarded as fitting parameters in the simulation and referred data of the deep level of bulk InAlAs [9].

Table I. Parameters used in the simulations.

		InGaAs		InAlAs	
		Electron	Hole	Electron	Hole
Mobility	μ [cm^2/V s]	10000	100	6000	100
Saturation velocity	v_s [cm s^{-1}]	2.7x10^7	1x10^7	8x10^6	1x10^7
Ionization parameters	A [cm^{-1}]	6.9x10^4	1.2x10^6	8.6x10^6	2.3x10^7
	E [eV]	4.1	2.8	4.7	7.5
	τ [fs]	250	250	250	250
Carrier lifetime	[ns]	1	1	1	1

C. Device structure

The device structure used for the simulation is shown in Fig. 1. The heterostructure consists of n-InAlAs cap layer (N_D = 1x10^{19} cm^{-3}, 250 Å thick), i-InAlAs barrier layer (N_D = 1x10^{15} cm^{-3}, 80 Å), n-InAlAs carrier supply layer (N_D = 1x10^{19} cm^{-3}, 50 Å), i-InAlAs spacer layer (N_D = 1x10^{15} cm^{-3}, 20 Å), i-InGaAs channel layer (N_D = 1x10^{15} cm^{-3}, 150 Å), and i-InAlAs buffer layer (N_D =

1×10^{15} cm^{-3}, 4000 Å). The deep level traps in 10-Å-thick regions at the surface of the side-etched region adjacent to the gate metal represent surface states. The Schottky barrier height of the gate electrode is 0.7 V. At the bottom of the buffer layer, Fermi energy is fixed to the middle of the bandgap. The lattice temperature was set to 300 K for all simulations.
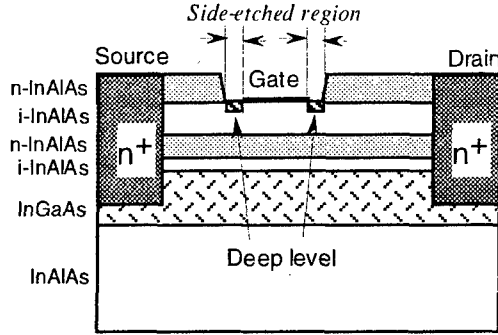

Fig. 1 Device structure for simulation.

III. CALCULATION RESULTS

A. Influence of impact ionization

Figure 2 shows the calculated I-V characteristics. The parameters for traps were $E_T = 1.0$ eV (measured from the bottom of the conduction band), $N_T = 6 \times 10^{13}$ cm^{-2}. The result shown by solid curves was calculated taking into account the impact ionization. The drain-to-source voltage (V_{ds}) at which the kink appears depends on the gate-to-source voltage (V_{gs}) but it is near the energy of the bandgap of InGaAs. In contrast, the result calculated without taking the impact ionization into account (dashed curves) does not show a kink.
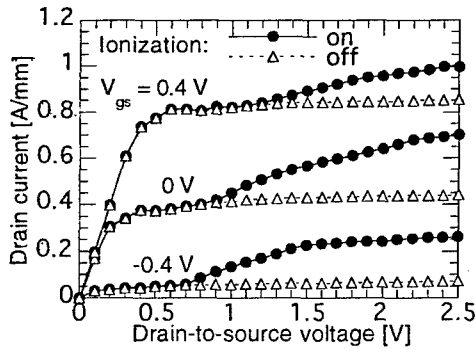

Fig. 2 I-V characteristics calculated with and without impact ionization. Gate length is 0.2 μm.

Some experiments show that the ionized holes are related to the kink [10]. The accumulation of the holes has also been observed experimentally by electroluminescence (EL) measurements [11]. Figure 3 shows the EL intensity and the simulation results of the sheet density of holes in the source-to-gate side-etched region. The gate length was 0.7 μm. The slope of the curve for the hole density is in good agreement with that of the EL intensity curve.

B. Influence of side-etched region

Figure 4(a) shows the calculated I-V characteristics at N_T's

between 1×10^{12} and 6×10^{14} cm^{-2}. When N_T is small, the kink does not appear. Thus, the impact ionization does not cause the kink by itself. The magnitude of the kink becomes larger as N_T increases. Figure 4(b) shows the simulation results when the energy level of the surface pinning, E_T, was changed from 0.6 to 1.2 V. The kink becomes significant as the surface pinning level gets closer to the valence band. These results can be understood as indicating that the electron density in the channel of the side-etched region decreases and, as a result, the parasitic resistance increases as the surface depletion becomes stronger.
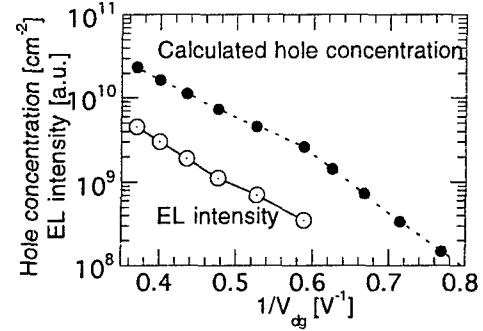

Fig. 3 Hole density in source-to-gate side-etched region and EL intensity. Gate length is 0.7 μm, and gate-to-source voltage is 0.3 V.
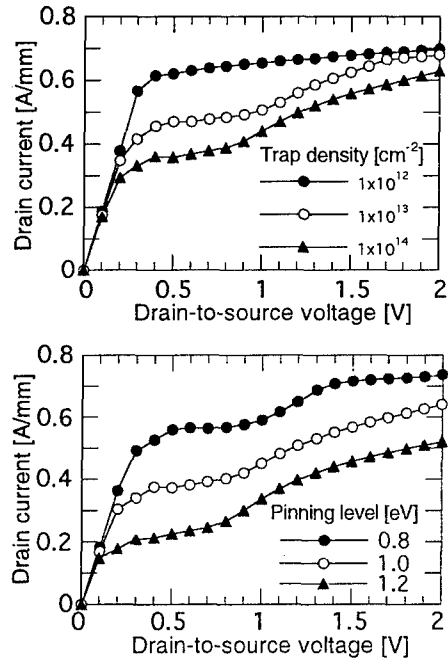

Fig. 4 Dependence of I-V characteristics on (a) surface trap density (top), and (b) pinning level (bottom). Gate length is 0.2 μm and gate-to-source voltage is 0 V.

Figure 5(a) shows the dependence of the I-V characteristics on the length of side-etched region. The drop of the drain current at $V_{ds} = 0.5$ V is also shown in Fig. 5(b) as a function of the side-etching length. The magnitude of the kink increases markedly with the

366

change in the side-etching length. This may result in poor reproducibility of the kink since this length cannot be controlled precisely when wet chemical etching is used in gate-recess process. Note that the drain-current drop plotted in Fig. 5(b) does not start from the origin. This result seems to indicate that the channel electron density at the edges of the side-etched region is higher than at the middle of the region because of the diffusion of electrons from the adjacent regions.
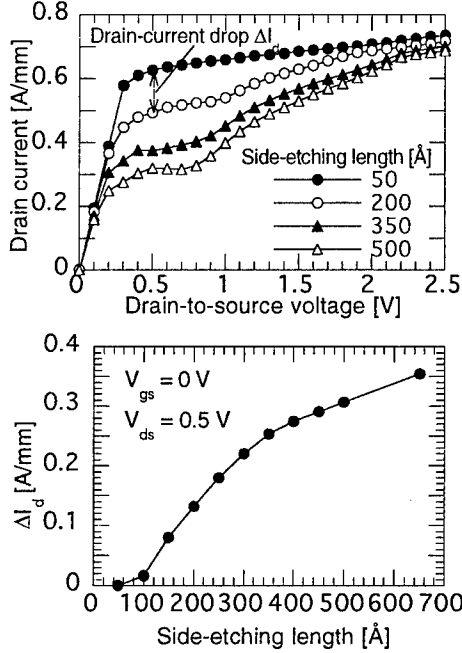

Fig. 5 (a) Dependence of I-V characteristics on side-etching length (top), and (b) Dependence of drain-current drop on side-etching length (bottom). $N_T = 6 \times 10^{13}$ cm^{-2}, $E_T = 1.0$ eV. Gate length and gate-to-source voltage are 0.2 μm and 0 V.

IV. DISCUSSIONS

A. Model of the kink

At first, the parasitic source resistance is divided into two part: the resistance of capped region, R_{s0}, and side-etched region, R_{ss}. Resistance R_{ss} is simply given as follows:

$$R_{ss} = \int_0^{L_{side}} \frac{dx}{q \mu_n n_s(x)}, \qquad (4)$$

where μ_n is the electron mobility, and n_s is the electron sheet density at position x. Figure 6 shows the V_{ds} dependence of the calculated sheet densities of electrons and holes at the source-to-gate side-etched region. In general, the electron density increases as a function of the logarithm of the hole density. Therefore, n_s is separated into two parts: the intrinsic part, n_{s0}, and the increase due to hole accumulation, Δn_s. Thus,

$$n_s(x) = n_{s0}(x) + \Delta n_s(x). \qquad (5)$$

However, another contribution is confirmed in the increase in electron density. The electron diffusion from the adjacent capped and gate regions are suspected. So n_{s0} is expressed by the sum of

the contributions of the surface pinning and the electron diffusion:

$$n_{s0}(x) = n_{ss}(\phi_B) + \Delta n_{s0}(x, V_{gs}, V_{ds}), \qquad (6)$$

where ϕ_B is the surface potential which depends on the density and pinning level of the surface states. Δn_{s0} expresses the electron diffusion from the adjacent regions: the source capped region and the gate region. It is a function of not only the position x but also V_{gs} because the electron density in the channel of the gate region increases with V_{gs}, resulting in the decrease in the magnitude of the kink at higher V_{gs}. The voltage V_{ds} also seems to affect Δn_{s0}, especially in HEMTs with a short gate length. In Fig. 6, two curves for hole density are shown: sheet density of holes in the channel layer, and the sum of the densities in the barrier and channel layers. The difference between the curves means that holes mainly distribute in the surface depletion region in the barrier layer at low V_{ds} whereas the hole density in the channel becomes dominant as V_{ds} increases. The V_{ds} at which the channel hole density becomes dominant is similar to that at which the slope of the electron density increases.
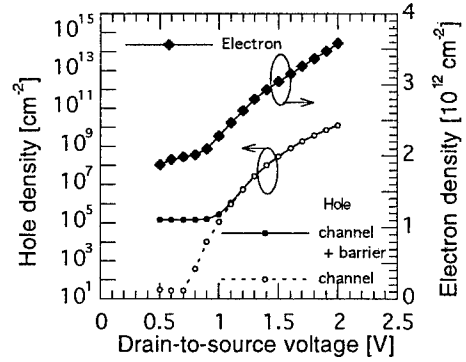

Fig. 6 Electron and hole densities in source-to-gate side-etched region. $N_T = 6 \times 10^{13}$ cm^{-2}, and $E_T = 1.0$ eV. Gate-to-source voltage is 0 V.

The mechanism of the change in the electron density is illustrated in Fig. 7. In equilibrium, the Fermi level is equal throughout the layers and is pinned by the surface states. When V_{ds} increase, the impact ionization occurs and holes begin to accumulate. The quasi-Fermi level for holes, E_{Fp}, in the channel layer gets closer to the valence band. Since hole current should not flow perpendicular to the layers, some of the holes moves to the barrier layer to equalize the E_{Fp} in both layers. As a result, the surface depletion in the side-etched region becomes smaller and the electron density in the channel increases. In this condition, the quasi-Fermi levels for electrons and holes are no longer equal. The difference is given as

$$E_{Fn} - E_{Fp} = \frac{k_B T}{q} \left(\ln \frac{n_s}{n_{s0}} + \ln \frac{p_s}{p_{s0}} \right), \qquad (7)$$

where n_{s0} and p_{s0} are the electron and hole densities in equilibrium. Here, since $(n_s/n_{s0}) \ll (p_s/p_{s0})$. Δn_s is given using the simple capacitance model as follows:

$$\Delta n_s(x) = \frac{\epsilon k_B T}{q^2 d} \ln \frac{p_s(x)}{p_{s0}(x)}. \qquad (8)$$

Once n_s is obtained, R_{ss} is obtained by substituting n_s into Equation (4). Finally, the expression of the drain current

367

including the kink is given as

$$I_d = \frac{g_{m0}(V_{gs}-V_{th})}{1+g_{m0}(R_s+R_{ss})},$$ (9)

where g_{m0} is the intrinsic transconductance. From Equation (9), it is found that the kink becomes significant when g_{m0} gets higher and R_s gets lower; i.e., when the performance of the HEMT improves.
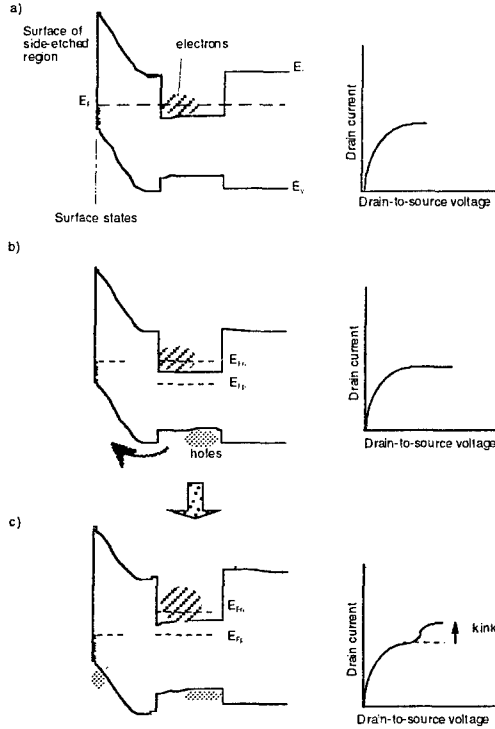

Fig. 7 Mechanism of kink. (a) quasi-Fermi level for electron, E_{Fn}, and hole, E_{Fp}, are equal at low V_{ds}. (b) when holes begin to accumulate, E_{Fp} gets closer to valence band in channel, (c) some of the holes move to the surface depletion region to equalize E_{Fp}, resulting in an increase in channel electron density.

B. How to eliminate the kink

It is found from Equation (4) that the kink arises from the change in n_s with the increase in V_{ds}, and that the magnitude of the kink depends on the inverse of n_s. Therefore, if n_s is large enough, the influence of a small change in n_s on the drain current is negligible; thus, the kink cannot appear. However, n_s generally becomes smaller when the threshold voltage of the HEMTs becomes higher, i.e., the threshold voltage approaches or exceeds 0 V. This is because the electron density of the gate and side-etched regions cannot be controlled independently by a gate-recess etching. If high-threshold-voltage HEMTs are required, the electron density of the gate region is small. As a result, the density of electrons in the side-etched region is also low and the kink is significant. However, as predicted in the discussion of Fig. 5, if the side-etching length is short enough, less than 100 Å (depends on the surface states), the contribution of R_{ss} to the drain current is

small because of the electron diffusion from the adjacent regions and the kink seems to be suppressed.

V. CONCLUSION

A model of the kink phenomena in InAlAs/InGaAs HEMTs was investigated using two-dimensional numerical device simulation. Taking into account non-local effect of impact ionization and surface states in the side-etched region of the HEMTs enables us to represent the kink in the simulation. The analysis of electron and hole density in the side-etched region leads to the following model of the kink: The electron density in the channel of the side-etched region is reduced by surface states. Once holes are generated by impact ionization and accumulate in the source-to-gate side-etched region, the potential profile is modified and the electron density is recovered. This results in the reduction of the parasitic source resistance and the kink appears. Therefore, keeping the electron density in the side-etched region high, and/or making the side-etching length short seem to be effective for eliminating the kink.

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368

A V-Band Monolithic InP HEMT Resistive Mixer with Low LO-Power Requirement

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Abstract

We report on a 60 GHz-band InP HEMT resistive mixer that can be operated with very low LO-power. The mixer is fabricated using Coplanar Waveguide (CPW) techniques to reduce production costs. A narrow source-to-drain space and a short length gate (0.15μm) are employed in order to reduce the LO-power requirement. The minimum conversion loss of 8.4 dB is achieved at a 55 GHz RF frequency with LO power of -2 dBm. This low LO-power is comparable with the best data ever reported for millimeter-wave passive mixers. In addition, the mixer has an excellent IF output linearity that indicates capability to provide good intermodulation performance.

Introduction

V-band and other millimeter-wave frequencies are very attractive for indoor communication LANs, collision avoidance radar, etc., because of large frequency resources, less potential for interfering with other wireless communication systems, and potential for small and light devices. Monolithic microwave / millimeter-wave ICs(MMICs) have advantages over hybrid microwave ICs(HMIC) in terms of miniaturization, good reproducibility, and low cost at high production volumes because of little interference from many connections such as bond-wires. These advantages are particularly notable in the millimeter-wave range, so MMIC technologies are essential in developing millimeter-wave systems.

Mixers are key devices for these front-end components and require low conversion loss, low local power and low intermodulation distortion(IMD). Operation with the low LO-power is an important requirement because of the difficulties in achieving oscillators with high output and high stability at the millimter-wave range. Good linearity is also required because of the wide dynamic range for receivers and low degradation of the modulated transmitted signal required for transmitters. Recently, resistive mixers have been widely investigated up to F-band because of low IMD performances and no dc bias to FET devices[1-2]. Because of abrupt changes in channel resistance[3], performance of InP HEMT-based resistive mixers is superior to that of mixers based on other materials.

In this study, a V-band monolithic InP HEMT resistive mixer using the CPW structure has been developed with a low LO power requirement for millimeter-wave communication and radar systems. The minimum conversion loss of 8.4 dB is achieved at 55 GHz RF frequency with LO power of -2 dBm.

Circuit design and fabrication

An AlInAs/InGaAs/InP HEMT is used for the MMIC mixer. Figure 1 shows a cross section of the HEMT. This HEMT typically indicates sheet carrier density of 3.0 X 10^{12} cm^{-2} and mobility of 1.0X10^4 cm^2/Vs at 300 K. The
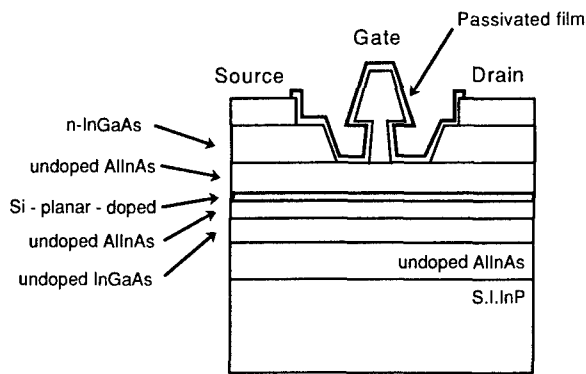
Fig. 1 Cross section of the InP HEMT.

Fig. 2 Microphotograph of the monolithic resistive mixer.

epitaxial layers are mesa-etched by wet etching to isolate each device. A narrow source to drain spacing of 1.5 μm is employed to reduce the parasitic resistance caused by the bulk. The 0.15 μm T-shaped gate structure is fabricated by a photo/EB hybrid exposure process[4], since it provides superior throughput to EB exposure alone. The gate recess is formed by the selective wet gate recess etching process with good uniformity. This etchant is a pH-adjusted citric acid/NH_4OH/H_2O_2 mixture. The etching sensitivity is more than 30 for InGaAs over AlInAs[5].

Figure 2 shows a microphotograph of the MMIC mixer. The chip size is 1.0 mm X 1.1 mm. The gate width of the HEMT is 80 μm. The CPW structure is chosen for MMIC fabrication in order to reduce production costs because of no via holes and backside processes. Non-linear parameters are obtained by DC measurements and S-pa-
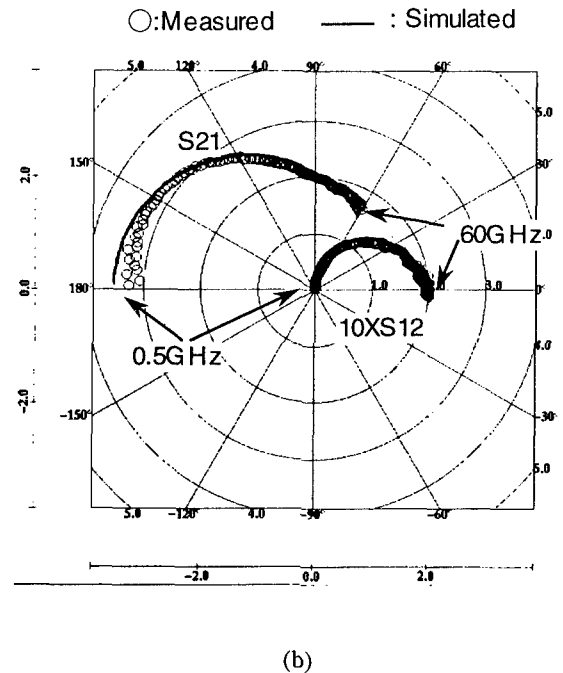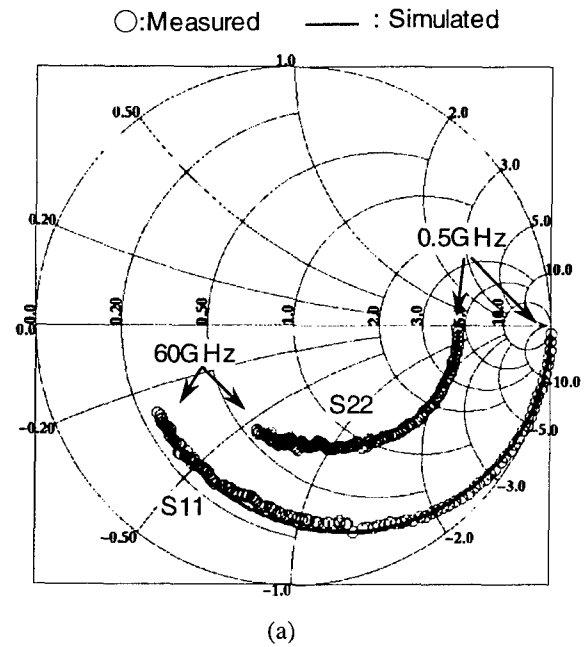

(a)

(b)

Fig. 3 Comparison between measured and simulated S-parameters under the hot bias state (VD=1V, ID=8mA) . (a) S11 and S22, (b) S21 and 10XS12.

rameters with cold bias states[6]. Figure 3 shows measured and modeled S-parameters under a hot bias state (VD=1V, ID=8mA). Good agreement is obtained over the band from 0.5 GHz to 60 GHz. This means that the extracted equivalent parameters, especially parasitic parameters, are valid
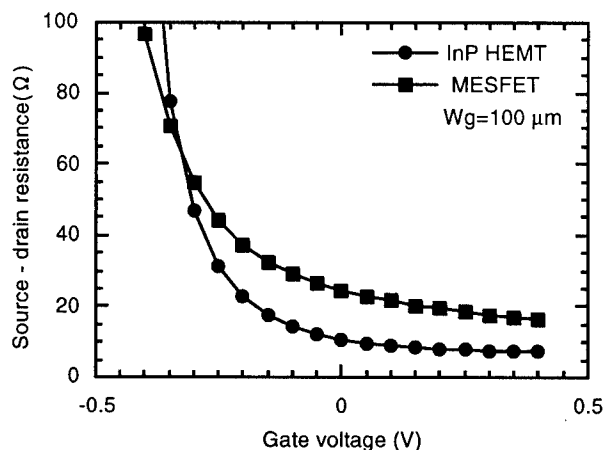
370

Fig. 4 Source-drain resistance dependent on the gate bias-Comparison between the InP HEMT and a conventional MESFET.
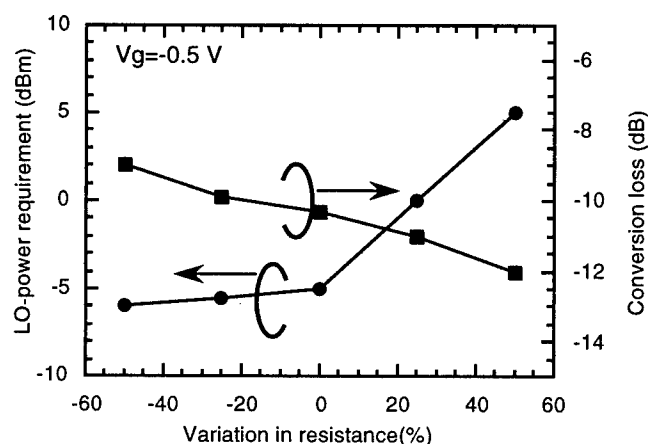

Fig. 5 Calculated the LO-power requirement and conversion gain vs the variation in parasitic resistance.

for the design of the MMIC mixer. The LO is applied to the gate with the negative gate bias and the LO port is matched to 50 Ω to reduce the LO-power requirement. The RF is applied to the drain through the 1/4 wavelength edge coupled line as the band-pass filter. The IF signal is obtained through the low pass filter that doubles as the drain bias line. The LO-power requirement for the mixer depends on the parasitic resistance, the variation of channel resistance by the gate bias and the gate capacitance. Figure 4 shows the differences between the InP HEMT and a conventional MESFET in source-drain resistance dependent on gate voltages. Both FETs have the same pinch-off voltage. The resistance of the InP HEMT is 10 to 15 Ω smaller

than that of the MESFET when biased at more than -0.2 V because of the narrow source to drain space. The resistance of the InP HEMT changes abruptly compared with FETs based on other material when the gate bias is smaller than -0.3 V. In addition, the InP HEMT has a small gate capacitance due to the very short gate length (0.15 μm). As a result, the InP HEMT resistive mixers can be operated with the low LO power at millimeter-wave frequencies. The LO-power requirement and conversion loss (when conversion loss is saturated) are simulated, utilizing a harmonic-balance simulator, as a function of parasitic resistance. As parasitic resistance increases, the LO-power requirement increases and conversion loss decreases as shown in figure 5.

Experimental results

The MMIC resistive mixer is tested by the millimeter-wave on-wafer measurement system. Figure 6 shows the measured conversion loss as a function of the RF frequency. The LO frequency is 54.6 GHz and the LO power is 0 dBm. The gate bias voltage of -0.5 V is the near pinch-off voltage and the drain voltage is 0 V. The conversion losses of 8.4 to 12.5 dB are obtained over the frequency range from 55 to 60 GHz. Figure 7 shows the measured conversion loss as a function of the LO power for LO at 54.6 GHz and RF at 55 GHz. The minimum conversion loss of 8.4 dB is achieved after the LO power reaches -2 dBm. This LO power level is comparable with the best data
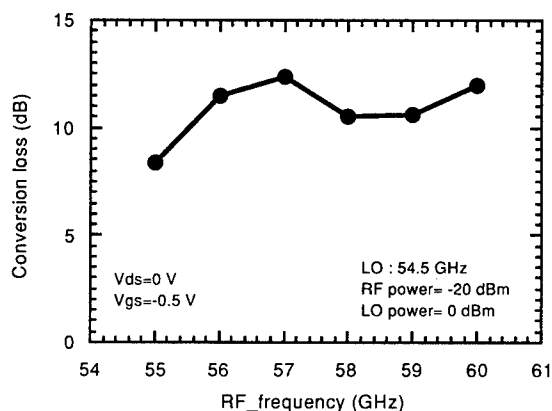

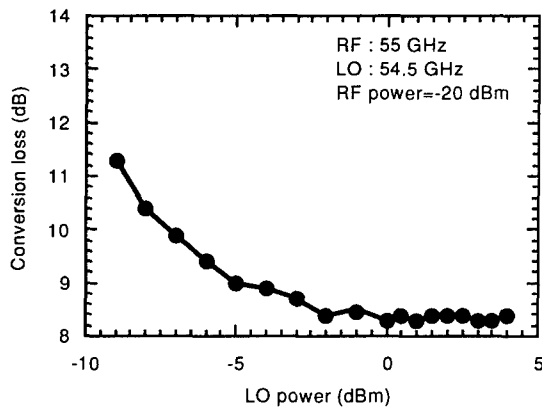Fig. 6 Measured conversion loss vs frequency.

371

Fig. 7 Measured conversion loss vs LO-power at RF frequency 55GHz and LO frequency 54.6 GHz.
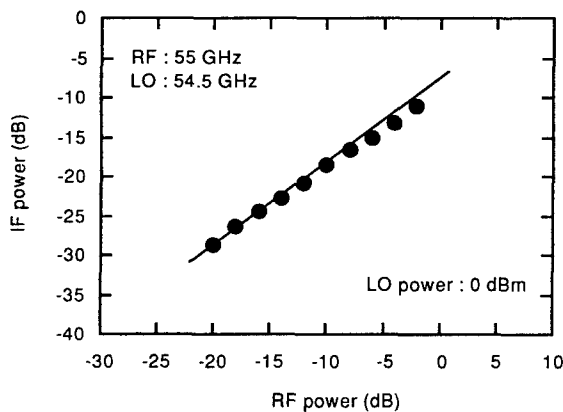

Fig. 8 Measured IF output characteristics as a function of the RF-power.

ever reported for millimeter-wave passive mixers and 10 dB lower than that of conventional diode mixers. Figure 8 shows the dependence of the IF output power on the RF input power at the LO power of 0 dBm. The compression level is about 0.5 dB at the RF power of -2 dBm. The input 1 dB compression level is expected to be around 0 dBm, comparable with the LO power. This level is also 10dB higher than that of conventional diode mixers. This performance promises wide dynamic range and a reduction in the number of stages in the millimeter-wave amplifiers.

Conclusion

A V-band InP HEMT based monolithic resistive mixer has been developed. This MMIC mixer is designed using CPW structure to reduced costs. The minimum conversion loss of 8.4 dB is achieved at 55 GHz RF frequency when the mixer is driven with LO power of -2 dBm. This LO power level is comparable with the best data ever reported for millimeter-wave passive mixers and very suitable for the millimeter-wave systems. The input 1 dB compression level is expected to be around 0 dBm, comparable with the LO power. This compression level increases as the LO-power increases. This performance promises wide dynamic range and a reduction in the number of stages in the millimeter-wave amplifiers.

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A NOVEL 3-D INTEGRATED RTD-HFET FREQUENCY MULTIPLIER

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INTRODUCTION

Resonant Tunneling Diodes (RTD) have demonstrated ultra high frequency capability [1]. They may exceed the frequency limits of 3-terminal devices which face the intrinsic limitation of feedback (e.g.[2]). On the other hand the RTD also faces constraints with respect to stability [3], impedance matching, and output power [4]. Most of these constraints are due to a necessary biasing in the negative differential resistance (NDR) regime. The combination of the RTD with three terminal devices [5,6] may avoid biasing the RTD in the NDR regime.

Frequency multiplication has been attained up to now by inserting the RTD in the input branch [5, 6] of a 3-terminal device. The RTD directly controls the 3-terminal device resulting in a negative transconductance with a large V_{ds} swing [6]. However, at this position the RTD acts as strong negative feedback which degrades the efficiency especially at extended microwave frequencies.

In this work we propose a frequency multiplier circuit where a RTD is inserted in the drain of a HFET to be used as a load. We will show that this approach results in a rectangular type of output voltage which is rich in odd harmonics. A demonstrator circuit will be presented and the potential of this approach up to submillimeter wave frequencies will be modelled.

I. Frequency multiplier circuit

The proposed circuit is shown in fig. 1. The common terminal, i.e. the drain/cathode of HFET/RTD, has to be accessible and acts as the output of the circuit.
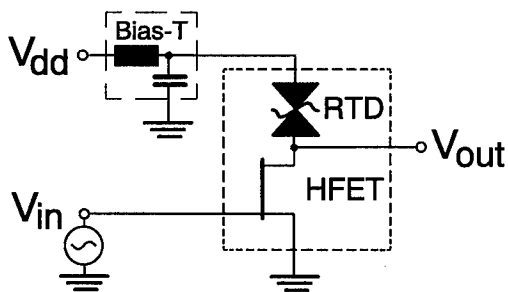

Fig.1: *RTD-HFET frequency multiplier circuit*

The area of the RTD anode and the width of the HFET gate has to be adjusted such that the peak current of the RTD is somewhat lower than the maximum saturation drain current of the HFET. Under this condition the load characteristic

exhibits a hysteresis for sinusoidal input voltage V_{gs} of sufficient amplitude (cf. fig. 2).
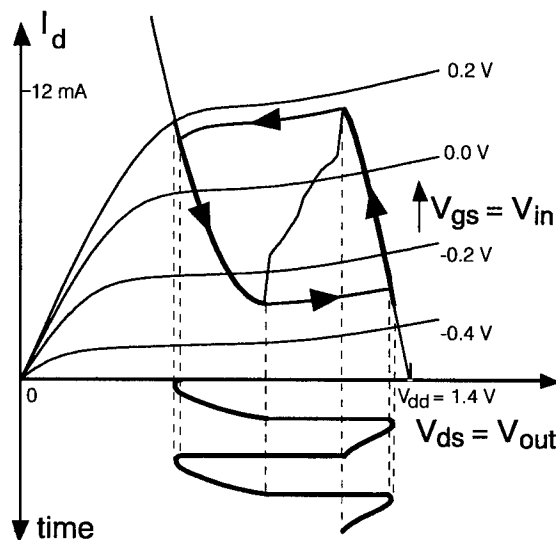

Fig.2: *The measured load characteristics of the InP-based device with a basic illustration for the generation of rectangular type output voltage*

The output voltage switches abruptly at both the peak- and valley voltage of the RTD load, respectively. The efficiency of the harmonics generation is defined as the voltage amplitude of the specific harmonic devided by the amplitude of the input voltage.

II. Modelling

The frequency multiplier circuit of fig. 1 was modelled using the HP-"Microwave Design System" circuit simulator (MDS). A combination of a one-port non-linear symbolic device model for the I-V-characteristic of the RTD and small signal elements for the parasitic device elements formed the large signal radio frequency RTD-model. The non-linear symbolic device contained a measured data set of a typical I-V-characteristic of a RTD. The parasitic elements were set to values derived from measured S-parameters of a RTD which was similar to the one in the demonstrator circuit which will be described later. We have carried out a time domain simulation of the output voltage V_{ds}. Results for an input frequency of 33.3 kHz and 33.3 GHz are presented in fig. 3. The spectrum of the output voltage V_{ds} is determined via a fourier transformation. A third harmonic voltage amplitude of 0.825 times the input amplitude for 33 kHz and 0.115 times the input amplitude for 33 GHz is obtained. The input amplitude had to be increased for 33 GHz to drive the load-RTD to the peak and the valley points.
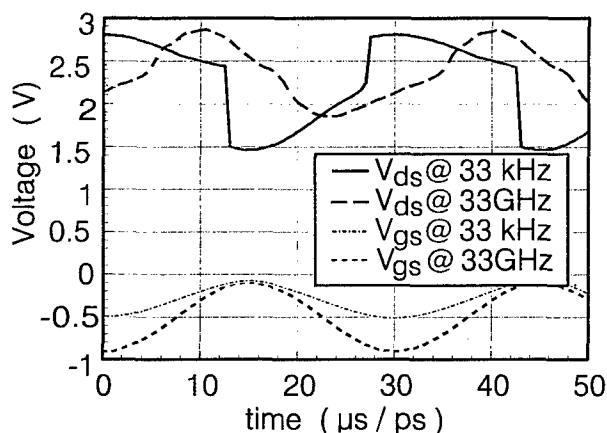

Fig. 3:   *Modelled output voltage vs. time for a RTD-HFET combination for 33kHz and 33GHz input frequency. For the lower frequency the time axis in is µs-units and for the higher frequenccy in ps-units.*

III. Frequency multiplier demonstrator

For highest integration-density, the double barrier RTD is grown in a single MBE run on an InP-based HFET-layer stack (cf. Fig. 4). The non-alloyed, self-aligned 1×90 µm² RTD-anode finger and gate finger electrode (1.4 µm × 70 µm) are defined by optical contact. The measured load characteristic is shown in Fig. 2
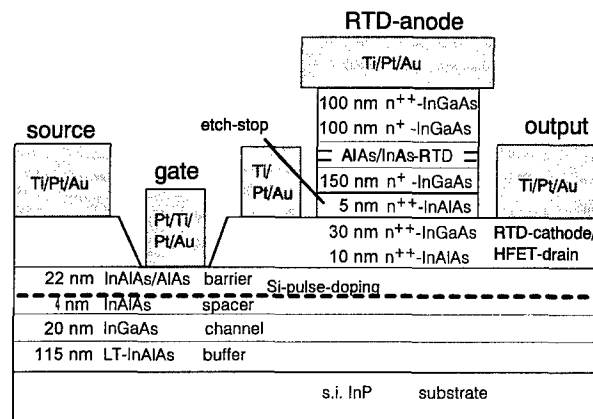

Fig. 4:   *One-step MBE-grown layer structure and self-aligned contacts*

For a first verification of the functionality of the RTD/HFET-circuit (cf. fig. 1), frequency multiplication was measured using a HP 8563A Spectrum Analyser with a frequency range from 9 kHz up to 26.5 GHz. The spectrum of the output-power (P_{out}) has been measured on wafer stimulated by a harmonic input-signal with a fundamental frequency $f_0 = 3$ GHz at an input-power of $P_{in} = -1$ dBm (fig. 5).
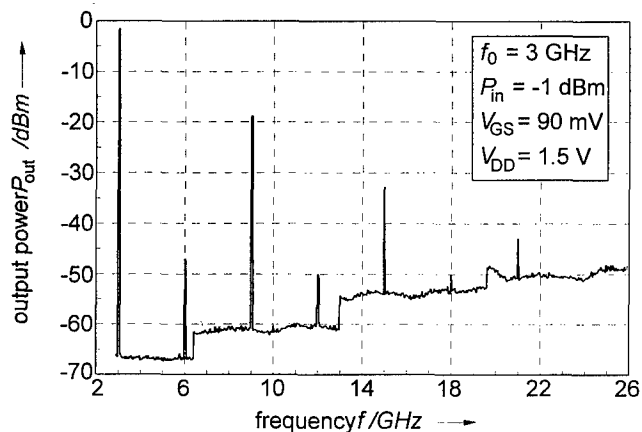

Fig. 5:   *Output-spectrum with a fundamental stimulation frequency of 3 GHz.*

The output-spectrum clearly demonstrates the preferred generation of odd harmonics. Under optimized conditions ($V_{gs} = 90$ mV, $V_{dd} = 1.5$ V), the power of the second and fourth harmonics is suppressed by more than -28 dB in comparison to the third one. The power-amplitude of the third harmonic is -19.3 dBm including all attenuations. The attenuation of the output-cabel and bias-Tee (HP 33150A) is estimated to be -3.2 dB at 9 GHz. In addition the bias supply was by no means optimized and the RF short was realised by an external capacitance. However, this result confirms the functionality of the RTD-HFET frequency multiplier at intermediate frequencies. A further optimization with respect to RTD-layer structure and circuit design is necessary and will rise the frequency up to the expected sub-millimeter wave operation

IV. Summary

A frequency multiplier circuit using a RTD as a load of a HFET is developed. Based on 3D-monolithic integration on s.i. InP-substrate a demonstrator is realised generating odd higher harmonics with high efficiency. The multiplier is highly compact and combines amplification of the fundamental frequency in the HFET with the high switching performance of the RTD. The Microwave Design System is used to evaluate its ultra high frequency potential predicting 0.115 times the voltage amplitude of the fundamental input signal for the third harmonic at 100 GHz. Optimization of the circuit design and the RTD-layer structure on top of the HFET with respect to the peak and valley parameters will increase the efficiency.

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Drain Resistance Degradation Under High Fields in AlInAs/GaInAs MODFETs

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Introduction

Lattice-matched AlInAs/GaInAs modulation-doped FETs (MODFETs) have demonstrated excellent high-frequency, small-signal performance [1]. However, high-power, large-signal applications of these devices may be limited. Impact ionization and tunneling reduce the breakdown voltage[2,3]. This limits the upper end of the output voltage swing, thus reducing the output power. Our results indicate that the lower end of the voltage swing (knee voltage) is also degraded by increased drain resistance when impact ionization occurs. Drain resistance (R_d) degradation from impact ionization has been observed in AlGaAs/GaAs[4] and AlGaAs/GaInAs[5] devices at rather high drain voltages. R_d degradation has been observed in AlInAs/GaInAs devices at low drain voltages[6]. In this work, we correlate R_d degradation in the AlInAs/GaInAs material system to the presence of impact ionization, which occurs at relatively low drain voltages because of the narrow bandgap of GaInAs.

Device Fabrication and Characteristics

AlInAs/GaInAs MODFETs were grown lattice-matched on (100) InP substrates by molecular beam epitaxy at 400 °C. The heterostructure consists of 100nm AlInAs, 10-period GaInAs/AlInAs superlattice, 12.5 nm GaInAs channel, 2nm AlInAs spacer, 8 nm AlInAs (8×10^{18} Si cm^{-3}), 10 nm AlInAs, 1nm GaInAs , 6 nm GaAs(6×10^{18} Si cm^{-3}), and 9.5nm GaInAs cap layer (1.2×10^{19} Si cm^{-3}). T-gate devices, with gate length of ~0.1 μm , were fabricated with a trilayer e-beam resist process as described in detail in ref. [7]. These devices have PtTiPtAu gates, non-alloyed ohmic contacts, and mesa isolation. Devices are coated with a silicon nitride layer. Typical FETs show maximum drain currents (I_{ds}) of 860mA/mm and maximum transconductance (g_m) of 930mS/mm. Source and drain resistance (R_s and R_d) were measured by the end resistance method.

These devices exhibit signs of impact ionization at a drain voltage of 2V (Fig.1). In particular, there is a negative peak in the gate I-V characteristics due to the collection of holes generated from impact ionization[8]. As the channel field increases with higher drain voltages, both the hole and the tunneling contributions of the gate current (I_g) increase (Fig. 1). As the V_{gs} is increased from pinch-off and carriers are introduced into the high field channel, the gate current increases to more negative values. However, as V_{gs} continues to be increased, the negative gate current is reduced mainly because of the onset of a positive gate current. Therefore, the gate I-V does not necessarily reveal the full gate bias range where impact ionization occurs [9].
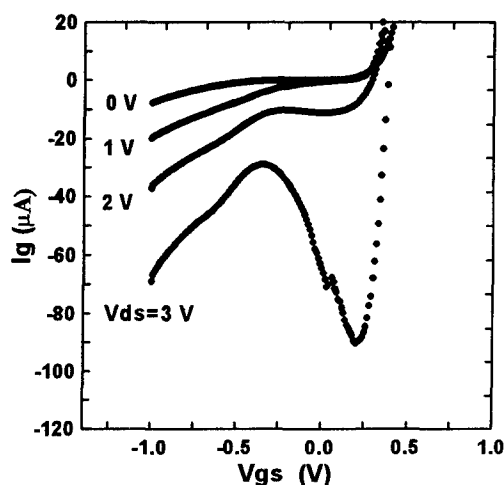

Fig. 1. Gate current measured at drain biases of 0 to 3V.

Bias Stress Conditions

Three methods of bias stress were performed. For all tests, the backside temperature was at room temperature. The first stress method was a constant-power bias stress at fixed drain voltages of 1 to 4V. The corresponding drain currents are listed in Table 1. During the stress the drain current was readjusted with the gate bias every 20 minutes to maintain a constant DC-power dissipation and channel temperature. Devices were stressed for a total of 20 hrs. Devices were stressed at $V_{ds}=1V$, where impact ionization was negligible, and at higher drain biases, where impact ionization becomes significant.

To determine the effect of drain current, a second set of stress tests was performed at drain currents ranging from 10 to 37mA at a fixed $V_{ds} = 3V$ for 1 hr. As the drain current was increased, the negative gate current increased. However, at the highest current studied, the gate was positively biased, and the current due to impact ionization was masked by the positive gate current.

The third stress method was a V_{gs} sweep at fixed V_{ds}. Devices were stressed by consecutively sweeping the gate, from pinch-off to saturation at a fixed drain bias. The gate is swept 5 times. Following each set of repetitive gate sweeps, the common-source characteristics were measured. The stress was continued by increasing V_{ds} for subsequent gate sweeps. Therefore, devices are subjected to the cumulative effects of drain bias, drain current, and channel temperature.

Degradation due to Bias Stress at Constant Power

Table I summarizes the change in a few key FET parameters after a constant DC-power stress of 700 mW/mm for 20 hrs. at various drain biases. The channel temperature was held constant, while V_{ds} was varied. At $V_{ds}=1V$ the impact ionization contribution to the gate current is negligible, and there is no measurable degradation. However, as the applied drain voltage increases, R_d increases, whereas the source resistance remains constant. Although the applied drain current is reduced, the current due to impact ionization is larger at the higher drain voltage. For example, as the drain bias is increased from 2V to 3V, the hole contribution of the gate current increases by a factor greater than 2 because of the increased channel field (Fig. 1). The R_d change increases from 7% to 22%. For an applied drain bias of 4V the R_d change is even greater. Therefore, although the channel temperature was held constant, the R_d degradation increases with the applied drain voltage.

The maximum drain current, measured at $V_{ds}=1.5$ V, also decreases as the applied stress bias increases. Fig. 2 shows typical FET transfer characteristics before and after bias stress at $V_{ds}=4V$. The reduction in maximum g_m and g_m at higher V_{gs}, as well as the reduction in maximum drain current, is clearly visible. I_{dss} does not significantly change, nor does the threshold voltage, V_{th}, suggesting that gate-sinking does not occur. Since the Schottky barrier also was unaffected, the doping under the gate presumably is unchanged. Degraded R_d and I_{ds} do not recover after annealing the devices for over 80 hours at 125°C.

Table 1. 2x30 μm FETs stressed at 700 mW/mm for 20 hrs.

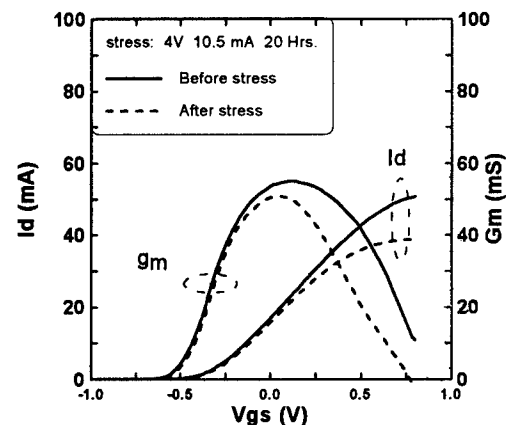| V_{ds} (V)	I_d (mA)	ΔR_d (%)	ΔR_s (%)	ΔI_d (%)	Δg_m (%)	ΔV_{th} (mV)
1	42	+1	-1	<1	<1	+3
2	21	+7	-1	-5	<1	-2
3	14	+22	+1	-11	-5	-2
4	10.5	+34	+1	-21	-8	-2

Fig. 2. Transfer characteristics for 2x30 μm FET before and after a stress of $V_{ds}=4V$ and $I_{ds}=10.5$ mA.

Degradation due to Drain Current at Fixed V_{ds}

To study the dependence of R_d degradation as a function of applied I_{ds} during stress, the change in R_d and R_s was measured for I_{ds} of 10 to 37 mA at $V_{ds}=3V$ for 1 hour. Fig. 3 summarizes the change in R_d and R_s with drain current stress. Although R_s is unaffected, R_d significantly increases. At drain currents less than 500 mA/mm, the impact ionization rate, as measured by the I_g/I_d ratio, is roughly independent of drain current and gate bias. Thus, the current due to impact ionization is roughly proportional to I_d, as is the change in R_d. At higher drain currents and more positive gate bias, we cannot observe a meaningful I_g/I_d ratio. As the applied current increases, the channel temperature significantly rises. The larger channel temperature may lead to an increased ionization rate due to bandgap shrinkage[10], or the larger drain current may lead to a decreased rate due to a reduction in peak channel field. It seems likely that the total current due to impact ionization increases with Id throughout the bias range that we studied for these devices. This increase in impact ionization probably contributes to greater R_d degradation. The magnitude of the I_d degradation also increases from 10 to 14% as the drain current is increased from 10 to 37mA.
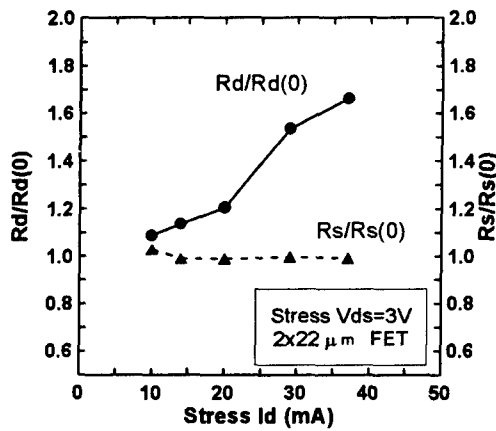
377

Fig. 3. Change in R_d and R_s as a function drain current stress. R/R(0) is the ratio of the final to initial resistance.

Fig. 4 shows the time dependence of the change in R_d and I_g of a device stressed at $V_{gs}=0V$ and $V_{ds}=3V$. I_g is the actual value measured at $V_{ds}=3V$ during the stress. The stress was momentarily stopped to measure R_d and then resumed. The drain current dropped from 21 to 19 mA during the stress. The rate of R_d degradation is initially high, and then decreases. I_g also follows a similar trend; I_g initially is high and rapidly decreases in magnitude. As there is less ionization current, the rate at which degradation occurs appears to be reduced. I_g is lowered partly due to the reduced field, corresponding to increased R_d and a wider depletion region, and partly due to the reduced drain current during the stress.
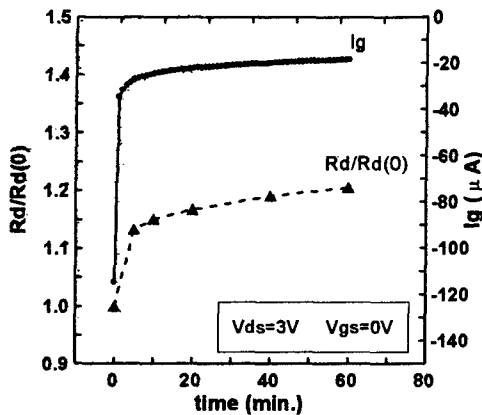
Fig. 4. Change in R_d and I_g with time, stressed at a fixed $V_{gs}=0V$ and $V_{ds}=3V$. $R_d/R_d(0)$ is the ratio of the final to initial R_d.

Degradation due to V_{gs} Sweep at fixed V_{ds}

R_d degradation is observed in devices stressed by sweeping V_{gs} at a fixed V_{ds}, equivalent to measuring the

transfer characteristics of the device. This test scans the entire range where impact ionization occurs, but it does not maintain a constant channel temperature or current. The final R_d change reflects a cumulative effect of these factors on degradation. Fig. 5 shows the change in R_d as a function of the applied drain bias during such stress. R_d rises, and R_s is constant during stress. Note that the rise in R_d with V_{ds} follows the trend of the calculated impact ionization integral with drain bias[3]. Notably, the integral rises significantly above zero at about the drain bias that causes the onset of R_d degradation. Devices with various MODFET structures and processing were also stressed. Devices with significant signs of impact ionization were more susceptible to degradation after sweeping the gate bias at a particular drain bias.
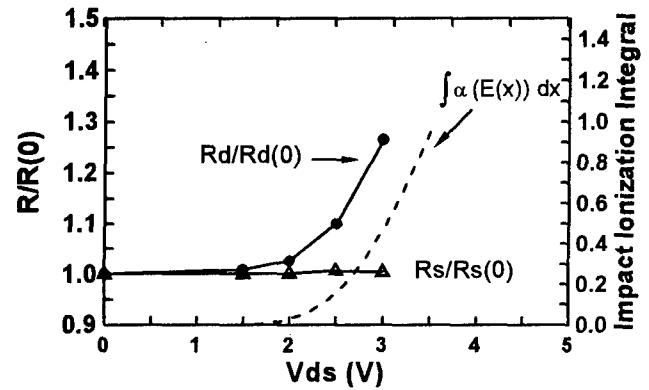

Fig. 5. Cumulative change in R_d and R_s after sweeping the gate voltage from pinch-off to saturation at a fixed V_{ds}.
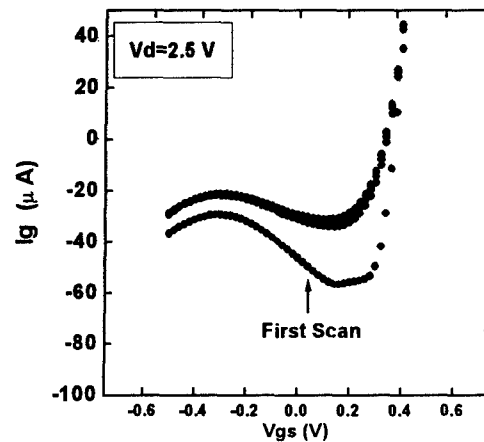

Fig. 6. Five repetitive sweeps of the gate current from pinch-off to saturation at $V_{ds}=2.5V$.

Fig. 6 shows how the negative peak in the gate current changes as the gate voltage is repeatedly scanned

378

at a constant V_{ds}. In all subsequent scans, this peak is dramatically less than in the first scan. Between the second and last scan, there is no observable change. This behavior begins at the onset of drain voltages that are sufficiently large to degrade R_d. Both the reduction in impact ionization and increase in R_d are consistent with a reduction in drain field and an increased gate-drain depletion region.

Discussion

For all types of bias stress, R_d degradation increases with increased applied drain bias, whereas R_s is unaffected. Degradation is observed when the gate IV characteristics indicate the presence of impact ionization at a particular value of V_{ds}. At $V_{ds}=1V$, where impact ionization is negligible, degradation was not observed. The extent of R_d and I_d degradation increases with the magnitude of impact ionization. Therefore, the drain voltage, the drain current during stress, channel temperature, and the length of time affect this degradation.

This increase in R_d, but not in R_s, indicates that there is increased depletion on the high-field drain side of the device, but not on the source side, after stress. This may be due to increased surface charge, or compensation or neutralization of the donor charge, on the drain side. This same effect limits the maximum drain current by creating a barrier to electron flow. There are several physical mechanisms that could explain this change in charge. Hot carriers could create defects as in the case of AlGaAs/GaAs MODFETs [10], or activate contaminants, introducing negatively charged traps that compensate the donors. A number of authors have suggested donor compensating contaminants, including fluorine[11] and oxygen[12]. These contaminants are particularly reactive with Al containing layers, and they could become charged traps when energetic carriers are present. Although the exact mechanism is not clear at this time, the correlation with the impact ionization current suggests that energetic carriers play a role in this degradation.

Degradation of R_d limits the operating range of the FET, and compromises its power capabilities. Other performance measures also suffer when R_d degrades. We have observed reduction in the current gain cutoff frequency, f_t, by as much as 30 GHz, when R_d degrades more than 50%. This reduction is attributed to an increased transit time because of the longer drain depletion region.

Conclusions

We have observed R_d degradation to occur when impact ionization is present. The magnitude of R_d degradation depends on the applied drain bias and drain current. These factors affect the degree of impact ionization, and thus the extent of the degradation. Since R_d increases and R_s does not, only the high field side of the FET is affected. This increase in R_d is attributed to a wider carrier depletion region between the gate and drain after stress, which results in reduced device performance.

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MODELING AND PERFORMANCE OF A ONE STAGE InP/GaInAs OPTOELECTRONIC HBT 3-TERMINAL MIXER

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Abstract

A high conversion gain 3-terminal heterojunction photo transistor optoelectronic mixer was demonstrated. The maximum obtained internal mixing efficiency was 11.3dB. The mixing performance was measured as a function of the DC bias of the device and local oscillator power level.. A SPICE based large signal model was employed to simulate the device. The main non-linear effects which contribute to the mixing process were the bias dependence of the dynamic emitter resistance, and the transition from the active to the saturation mode.

I. Introduction.

In optical subcarrier multiplexing (SCM) systems (1,2) the modulated laser beam is detected, down-converted, and amplified, to recover the original baseband information. The heterojunction photo transistors (HPT) is a natural candidate to carry out all three tasks simultaneously. The inherent non-linearity of 3-terminal InP/GaInAs HPTs, and their excellent high frequency performance as front end components (3), are very attractive for SCM systems.

In this publication, we report on the performance of a one stage InP/GaInAs HPT optoelectronic mixer (OEM). The obtained mixing performance at different bias conditions and local oscillator power levels is compared to a SPICE based large signal model. We believe this is the first report on modeling of an HPT-OEM. An intrinsic conversion gain (i.e., the ratio between the output IF power and the primary photogenerated RF input power) of 11.3dB was obtained. Due to a light coupling efficiency of only 15%, the extrinsic conversion gain is -5.1dB, which still compares favorably with previously reported results of -21.1dB, -26dB and -29dB for 3-terminal HBT, HEMT and JFET, OEMs (4). The origin of the various non-linear effects in HPTs is discussed as well.

II. HBT fabrication.

The epitaxial layers were grown on semi insulating InP substrates by a compact metalorganic molecular beam epitaxy system (5). Conventional wet etching and a self aligned Pt/Ti/Pt/Au one step metalization process were employed to fabricate the devices. Polyimide passivation and Ti/Au pads completed the fabrication process.

A schematic diagram of the device is shown in Fig.1. The optical window was located on the base mesa in order to minimize device dimensions. Current crowding effects (6) are also avoided because the light is absorbed in the extrinsic base collector junction. This configuration is basically similar to a separate PIN diode connected to the base terminal, except that the reverse bias of the PIN diode cannot be separately set.
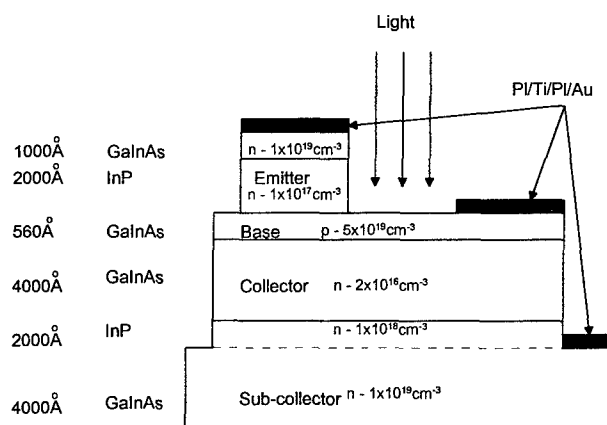

Figure 1 - Schematic diagram of layer structure and mesa structure of the HPT. Emitter and base dimensions are $3.3 \times 11 \mu m^2$ and $8.5 \times 22.5 \mu m^2$, respectively. Optical window (on the base mesa) size is $5 \times 6 \mu m^2$.

III. Large signal modeling

A large signal SPICE model was employed to simulate the mixing performance of the HPT. The model parameters were extracted from DC measurements and small signal on wafer RF measurements up to 40GHz (7). F_t and F_{max} of 65GHz and 35GHz, respectively, were measured at $I_C = 20mA$, $V_{CE} = 2V$. Table 1. lists the parameters used in the simulations..

Table 1. Large signal SPICE model parameters

REE	8Ω
RCC	3Ω
Rb	15Ω
Cbc(v=0)	120fF
Cbe(v=0)	32fF
Nf	1.1
Nr	1.2
Is	1fA
Ics	6nA
Beta	80
t_f	0.85ps
t_r	1ns

The schematic circuit diagram of the packaged HPT is shown in Fig.2. The voltage source, V_{lo}, represented the local oscillator. The current source, I_{ph}, represented the modulated primary photocurrent (RF signal). The input impedance of the spectrum analyzer was represented by a 50Ω load resistor, and the inductance of the bonding wires was included as well. The simulations were carried out using SPICE transient analysis and a subsequent Fourier transform. The results are presented in section V.
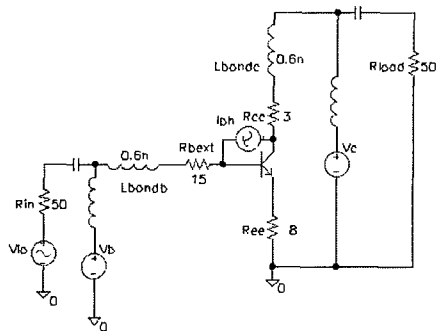
Figure 2 - A SPICE based large signal model of the HPT optoelecronic mixer.

IV. Electroptical Mixing Experiment

The experimental setup is shown in Fig. 3. The HPT was mounted onto 50Ω transmission lines. A current modulated distributed feedback laser generated the RF optical signal. The wavelength of the light was 1.55µm and the modulation frequency 3GHz. The laser average optical power was 0.37mW and the modulation index was 24%.

The base terminal of the HPT served as an input terminal for the local oscillator (LO) signal. The frequency of the (LO) signal was 3.1GHz. The 100MHz intermediate frequency (IF) output power at the collector was measured using a spectrum analyzer. Measurements were carried out as a function of the base-emitter voltage and collector-emitter voltage for different LO power levels.
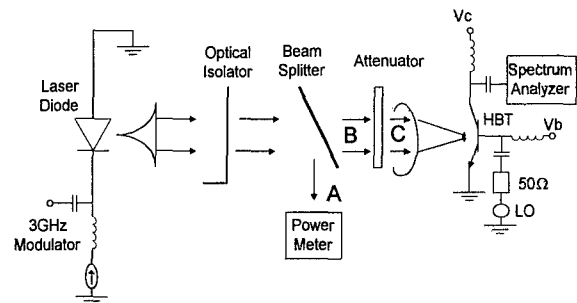

Figure 3. - Experimental setup.

V. Results and discussion

In Fig. 4 the measured and calculated IF power is plotted as a function of base emitter voltage for different LO power levels. The mixing efficiency exhibits a clear maximum at $V_{BE} = 0.8V$. The physical reason for the shape of the curve is the following. The HPT serves as a mixer and current amplifier simultaneously. The main non-linear effect in this bias range is the bias dependence of the dynamic emitter resistance, r_e, which determines the current gain of the HPT at high frequencies. At low values of V_{BE} r_e is large and the amplification level of the IF signal is low. For high values of V_{BE} r_e is small, and therefore the modulation of r_e modulates the current gain to a small extent only. The mixing efficiency is thus maximized at intermediate values of V_{BE}.

As evident by inspecting Fig.4 the simulations agree very well with the experimental results for low to moderate base emitter voltages. However, at high V_{BE}, and for moderate V_{BE} with large LO power, the simulations do not agree well with the measured data. We believe this discrepancy is due to high current density effects (8), such as the Kirk effect, which were not included in our model.
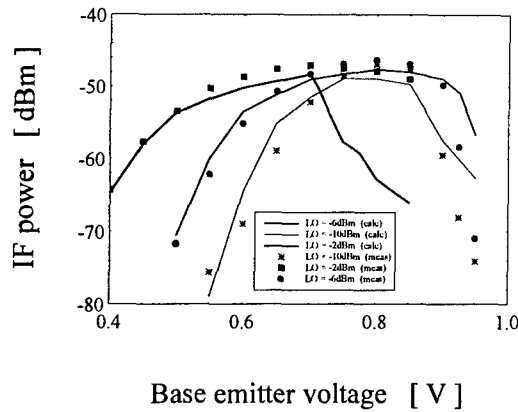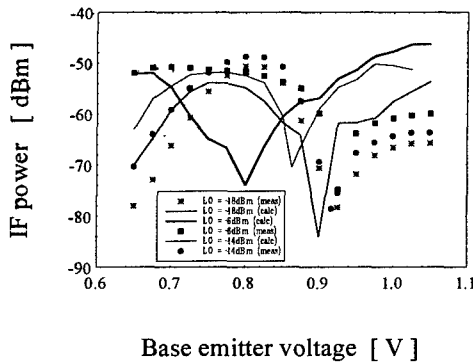
Figure 4 - Calculated and measured IF (100MHz) power as a function of base emitter voltage. Incident optical RF (3GHz) peak power is -10.5dBm. $V_{CE} = 1.5V$

An additional non linear effect in HBTs is the transition from the linear mode to the saturation mode. This effect is important at low values of the emitter to collector volatge. In Fig. 5 the measured and calculated IF power is plotted as a function of base emitter voltage with an emitter to collector voltage of 0.8V. Since V_{CE} is constant in this experiment, at low V_{BE} the base collector junction is reverse biased, and the HPT is in the active mode. At high values of V_{BE} the base collector junction is forward biased, and the HPT is in the saturation mode. A clear minimum in the measured and calculated IF power can be observed in the transition region between the linear and saturation modes. We believe this minimum is due to an opposite phase of the two non-linear effects resulting in a mutual cancellation of the IF signal.

Base emitter voltage [V]

Figure 5 - Calculated and measure IF (100MHz) power as a function of base emitter voltage. Incident optical RF (3GHz) peak power is -10.5dBm. $V_{CE} = 0.8V$

In the saturation mode a severe degradation of the IF current gain of the HPT takes place. However, the results

presented in Fig.5 demonstrate that reasonable IF power levels were obtained in the saturation mode as well. The strong non-linearity caused by the transition between the active and saturation modes generates the IF power levels obtained. The discrepancy between the simulations and experimental results in the saturation mode is an indication that our modeling in this range must still be improved.

In Fig. 6 the measured IF power is shown as a function of emitter to collector voltage with $V_{BE} = 0.8V$ and LO power of -6dBm. The best mixing results are achieved when the HBT is biased in the active mode. For $V_{CE} > 1.5V$ the IF power saturates because the high frequency response of the HBT and the non-linear effects depend weakly on V_{CE}.
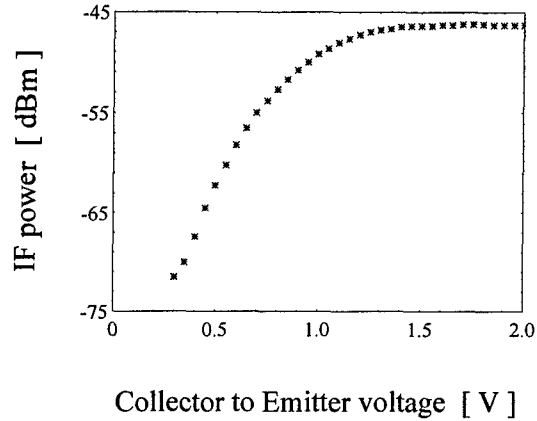

Collector to Emitter voltage [V]

Figure 6 - IF (100MHz) power as a function of collector to emitter voltage. $V_{BE} = 0.8V$ and LO (3.1GHz) power is -6dBm. Incident RF (3GHz) power is -10.5dBm.

VI. Mixing performance

The quantum efficiency η of the HPT was found to be 15%. It was obtained by measuring the DC primary photocurrent (base shorted to the emitter). This relatively low quantum efficiency is due to the total thickness of the base and collector layers which is about 3 times shorter than the absorption depth of the light.

We define the intrinsic conversion gain, G_{int}, as the ratio between the IF power delivered to the 50Ω load and the power delivered by the primary photocurrent RF power into a 50Ω load . The primary photo generated RF power was $P_{prime} = -52.3dBm$ in our experiments. The extrinsic (or system) conversion gain, G_{ext}, is defined as $G_{ext} = \eta^2 G_{int}$

The highest intrinsic conversion gain obtained in our experiments was 6.1dB. Since the base is connected to the LO source via a 50Ω line some of the primary photocurrent leaks

382

through the LO source to the ground. To rectify this, a 3-stub tuner was inserted between the LO source and the base and was adjusted to obtain maximum IF power. The intrinsic conversion gain improved in this manner by 5.2dB to 11.3dB. The insertion of the 3-stub tuner increased the RF output power by 4.1dB and the LO output power by only 0.4dB, indicating that the improvement of the conversion gain is due to a more efficient collection of the primary photocurrent into the base, and not due to a better matching of the LO network.

The obtained extrinsic conversion gain was -5.2dB using the 3-stub tuner. This result compares favorably with previously reported results of -21.1dB, -26dB and -29dB for 3-terminal HBT, HEMT and JFET, OEMs (4).

VII. Conclusion

The performance and modeling of a high conversion gain 3-terminal HPT OEM is reported as a function of the bias level and LO power level. The highest mixing efficiency is achieved when the HPT operates in the active mode. The largest non-linear effect which is responsible for the mixing process is the bias dependence of the dynamic emitter resistance. Further improvement of the mixing efficiency can be achieved by increasing the quantum efficiency (increasing the collector thickness), RF isolation of the base terminal, and reducing the collector load impedance.

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InP-InAlAs and InGaP-InAlAs mixed spacers
to reduce the gate leakage current in InAlAs/InGaAs/InP HEMTs

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Introduction

Due to its superior noise performances at high frequency, InAlAs/InGaAs/InP pseudomorphic HEMT is a very good candidate for high bit rate optical communications or millimeter-wave circuit applications. However this device suffers from a low breakdown voltage which impedes further applications requiring high power or low gate leakage current.

In the off-state, the gate leakage current is attributed to a two step process: first impact ionization in the small energy gap channel (In-rich InGaAs) creates electron-hole pairs, secondly, the resulting holes reach the gate where they are collected, thus generating an excess leakage current. Consequently, a way to reduce gate leakage current is to increase the barrier seen by holes in their path toward the gate, i.e. to increase the valence band offset between the channel and the spacer layers [1-4].

In this work, we propose a comparative study of the behaviour of three HEMT structures at high reverse bias: a reference structure (S1) whith a conventional InAlAs spacer, the second with an InP/InAlAs mixed spacer (S2) and the third with an $In_{0.5}Ga_{0.5}P$/InAlAs (S3) mixed spacer. We show a drastic decrease of the gate leakage current for the mixed spacer HEMTs, thanks to the large valence band offset between InP (or InGaP) and InGaAs. Moreover, Low Frequency Noise (LFN) measurements were performed to investigate the defects distribution in the three structures. The later help us distinguishing between the transport mechanisms which govern the gate leakage current.

I. Samples

Figure 1 described the cross section of the three structures. They were grown in a two step process: first, the buffer, the channel and the InP or InGaP part of the spacer were grown at CEMD in a gas source MBE, secondly, the rest of the structure (InAlAs part of the spacer, barrier and cap layer) was epitaxially regrown at LEAME in a solid source MBE.

Before the epitaxial regrowth, the surfaces of CEMD epitaxialy grown structures are cleaned by an UV-ozone oxidant treatment (1 minute) followed by an HF-ethanol chemical etching using a spinning technique. It is assumed that 10 Å of InP material is etched during this procedure. So, after the cleaning procedure, 30 Å of InP remain on the S2 surface, while no InP layer is expected on S1 and S3. As indicated by RHEED pattern during regrowth on S2 structure, the HF-ethanol spinning treatment is well adapted to InP surface. On the contrary, spotty RHEED pattern observed at the beginning of regrowth on S1 and S3 structures indicates that this treatment is not optimized for InGaAs and $In_{0.5}Ga_{0.5}P$ surfaces.

The HEMTs were processed using conventional optical lithography. After mesa etching for devices isolation, Ge/Au/Ni/Au contacts were evaporated and alloyed at 400°C/75s onto a hot plate. A Pd/Au recessed gate was then defined and evaporated. No passivation of the devices was realized. The three structures were processed in the same technological run to insure no technology induced effect.

S1			S2			S3		
Conventional InAlAs spacer			**Mixed InP/InAlAs spacer**			**Mixed InGaP/InAlAs spacer**		
InGaAs	5×10^{18}cm^{-3}	100 Å	InGaAs	5×10^{18}cm^{-3}	100 Å	InGaAs	5×10^{18}cm^{-3}	100 Å
InAlAs	nid	250 Å	InAlAs	nid	250 Å	InAlAs	nid	250 Å
InAlAs	5×10^{18}cm^{-3}	90 Å	InAlAs	5×10^{18}cm^{-3}	60 Å	InAlAs	5×10^{18}cm^{-3}	60 Å
InP	nid	10 Å	InP	nid	40 Å	InP	nid	10 Å
						$In_{0.5}Ga_{0.5}P$	nid	30 Å
InGaAs	nid	300 Å	InGaAs	nid	300 Å	InGaAs	nid	300 Å
InP	nid	2000 Å	InP	nid	2000 Å	InP	nid	2000 Å
InP	substrat S.I.		InP	substrat S.I.		InP	substrat S.I.	

Figure 1: Layer structures (the spacer layers are in grey tone, the double-line indicates the regrowth interface)

II. Hall measurements and simulations

Table 1 shows the results of Hall experiments on the three structures. As we can see, the carrier density in the channel (n_s) is very low (from $6 \times 10^{11} cm^{-2}$ for the S1 sample to $3 \times 10^{11} cm^{-2}$ for the S3 sample). Schrödinger-Poisson calculations indeed forecast a sheet carrier density of about $2 \times 10^{12} cm^{-2}$, common to the three structures. The discrepancy between measured and calculated data can be attributed to the defects associated with the epitaxial regrowth. To evaluate this effect, Schrödinger-Poisson calculations were performed, assuming a negative fixed charge density N_{it} located at the epitaxial regrowth interface.

	S1 InAlAs		S2 InP/InAlAs		S3 InGaP/InAlAs	
	300K	77K	300K	77K	300K	77K
n_s $\times 10^{11} cm^{-2}$	6.04	3.89	6.21	4.68	2.7	0.67
mobilité $cm^2 V^{-1} S^{-1}$	4600	9420	6460	15310	4280	5060

Table 1: Hall measurements

For the three structures, N_{it} was adjusted in order to obtain the measured n_s in the channel. Our results show a much larger charge density of interface defects for the structure S3 (figure 2).

As a matter of fact, the exact location of the defects induced by the regrowth is not known, and the deduced charge densities correspond to defects located either at the regrowth interface or in the layers above, or both.
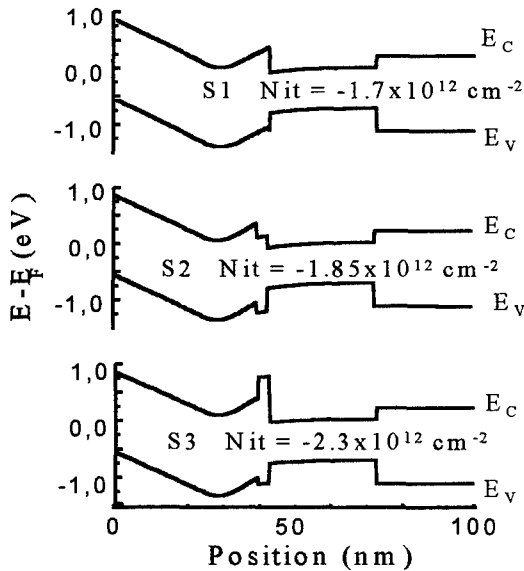
Figure 2: Simulated band diagrams with negative interface charges

III. Device operation

Table 2 summarizes the main static characteristics of $2\mu m$ gate length HEMTs fabricated on the three structures. Drain saturation current and maximum transconductance are surprisingly low for all transistors, especially for S3, in agreement with the presence of defects deduced from Hall characterization.

	Idss (mA/mm)	Gmmax (mS/mm)	$V_{Pinch-off}$ (Volt)
S1	30	60	-0.5
S2	36	58	-0.6
S3	20	20	-0.7

Table 2: Static characteristics of HEMTs

Then, we have focused our study on gate leakage current. First, we have checked the quality of schottky contacts: in forward bias high barrier height (0.7V) and good ideality coefficient (n=1.3) are obtained for the three structures. It allows us to expect a very low thermionic contribution to the reverse bias current. Figure 2 shows the gate leakage current of HEMTS for two different gate lengths and temperature measurements.

For small gate length and room temperature, the leakage current is drastically reduced for both mixed-spacer structures (S2 et S3), as compared with the classical one (S1). On the other hand, for large gate length or low temperature, the higher leakage current is obtained for structure S3, and structure S2 still exhibits the lower leakage current at reverse gate voltage.
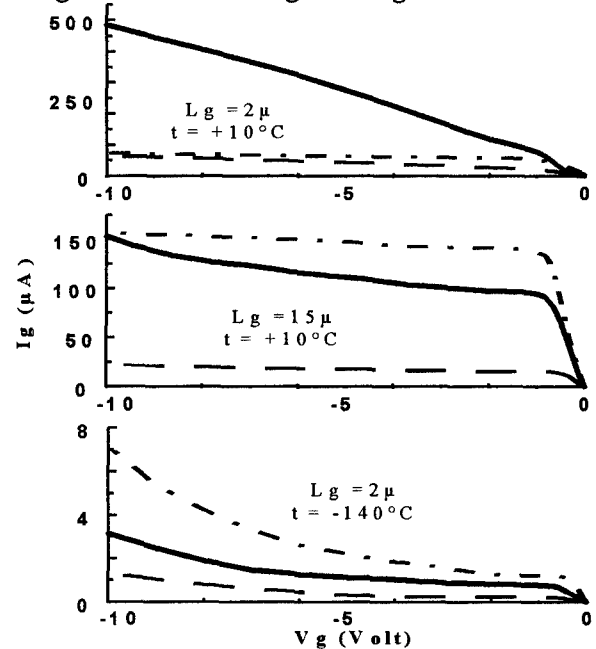

Figure 3: $I_G(V_G)$ characteristics of HEMTS ($V_D=V_s=0V$) (full: S1, dotted: S2, dashed-dotted: S3)

IV. Discussion

The previous results can be explained in terms of impact ionization in the channel and defect-assisted tunnelling. Figure 4 describes, on a schematic energy diagram, the different conduction processes which govern the gate leakage current.

Let us first remind the main influences of temperature and gate length on these processes:

- the shorter the gate, the stronger the impact ionization (large electric field).

- at low temperature, thermionic effects quickly decrease, thus tunnelling effects drive the clearing of energy barriers by free carriers

Moreover, concerning our structures, it must be point out that:

- the leakage due to holes generated by impact ionization should be reduced in mixed-spacer structures (S2 and S3), thanks to the large valence band offset between the InGaAs channel and the InP (or InGaP) spacer (figure 2).

- Tunnelling effects should be more important in S3, due to a larger defects density (this point will be confirmed in next part).
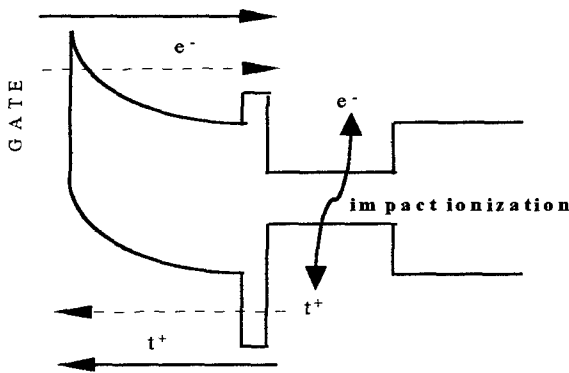
Figure 4: Sources of gate leakage current (full-line arrow:thermionic, dotted-line arrow:tunnelling)

Then we can easily explain the three graphs of figure 3. At room temperature and for a 2μ gate length, S1 has the highest leakage current due to the holes generated by impact ionization in the channel which reach the gate by thermionic effect over the valence band barrier. S2 and S3 have the same low current, thanks to a higher valence band barrier. For a 15μ gate length, impact ionization is lowered (the gate current is smaller than in the previous case) and the leakage current is partly governed by the schottky barrier. Thus, due to tunneling through defects located near the Schottky contact, the largest leakage is for S3. For S1, the excess leakage current, as compared to S2, is to be attributed to a higher impact ionization induced current. At low temperature and for 2μ gate

length, thermionic effects are lowered and the current is governed by tunneling effects; then, holes created by avalanche reach the gate by defect-assisted tunneling through the valence band barrier; thus, due to a larger density of defects near the channnel, S3 has the highest current.

V. Low Frequency Noise Measurements

Noise power spectra were recorded using an Advantest R9211B power spectrum analyser, and an EGG 5182 low noise pre-amplifier. Measurements were performed on gate free structures of different lengths (ranging from 5 to 160μm), with a TLM configuration, and on HEMT transistors, with gate lengths ranging from 0.8 to 10μm. The channel width is 200μm for the TLM structures and 50μm for the transistors.

Measurements were performed at room temperature (TLM) and from 80K to 380K (transistors).

The current noise spectrum S_i was derived from the noise voltage S_V through the relation :

$$S_i = G^2 S_v \qquad (1)$$

where G is the pre-amplifier gain (A/V)

TLM measurements :

Low Frequency Noise (L. F. N) spectra were recorded at room temperature in the frequency range 1Hz-100kHz. DC bias was applied to the sample using voltage sources supplied by low noise batteries.

From the current noise spectrum S_{ich} of the channel, we extract an equivalent defect density N_t ($cm^{-2}eV^{-1}$) which represents the noise index of the sole channel, and doesn't include the contacts contribution to the total noise [5] [6] [7]. The values of N_t are summarized in table 3.

Sample	S1	S2	S3
N_t ($cm^{-2}eV^{-1}$)	$3\text{-}6\times10^{10}$	$3\text{-}6\times10^{10}$	$1\text{-}2\times10^{11}$

Table 3: Noise index N_T of the channel

Transistors measurements :

Gate current noise spectra were recorded from 80K to 380K in the frequency range 1Hz-100kHz.

Figure 4 shows the normalized current noise spectra S_i/I^2 (Hz^{-1}) of the three samples at ambient temperature. The spectra are 1/f like with the addition of G-R features. It is shown that the normalized noise spectra of S1 and S2 are in the same order of magnitude, when S3 exhibits a higher current noise level, as suggested from the values of N_t extracted from the TLM structures.

Figures 5 and 6 represent the Arrhenius plots of G-R features measured for S1 and S3, and table 4 summarize the deduced energy levels.
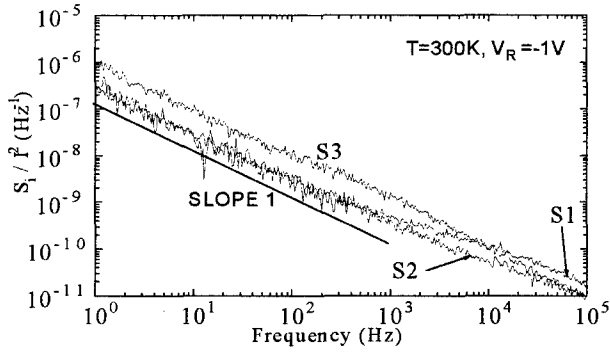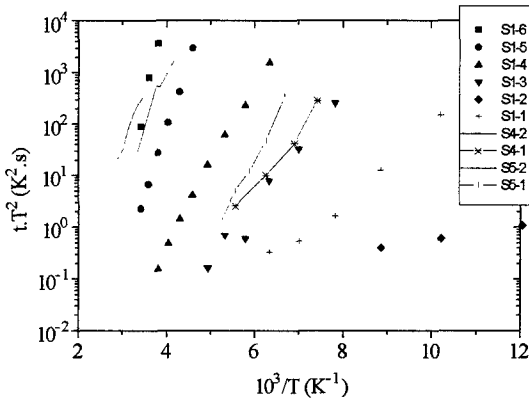
386

Figure 4: normalized current noise spectra

figure 5: Arrhenius plots for sample S1
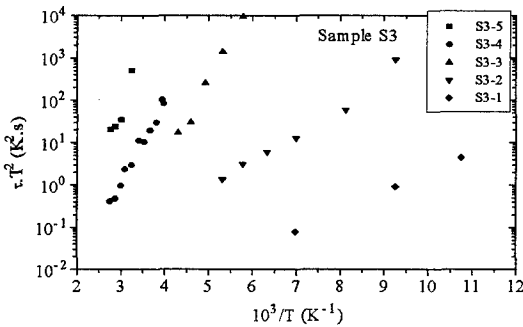(lines:samples S4 and S5, see text)

figure 6: Arrhenius plots for sample S3

Sample	S1	S2	S3
Energy (eV)	S1-1 : 0.05 S1-2 : 0.16 S1-3 : 0.22 S1-4 : 0.31 S1-5 : 0.52 S1-6 : 0.8	S2-1 : 0.16 S2-2 : 0.5	S3-1 : 0.09 S3-2 : 0.13 S3-3 : 0.38 S3-4 : 0.4 -0.45 S3-5 : 0.85-0.9

table 4: Energy levels extract from noise measurements

To confirm this, a comparison was carried out with HEMT processed the same way on lattice matched and pseudomorphic stuctures grown by Picogiga SA. S4 is a standard LM InAlAs/InGaAs/InP structure with a 420Å thick InGaAs channel and a 310Å InAlAs barrier. S5 is a standard PM InAlAs/InGaAs/InP structure with a 120Å thick InGaAs ([In]=0.7) and a 310Å InAlAs barrier. Both structures are epitaxially grown without growth interruption. As it can be seen on figure 5, these samples exhibit much less deep levels.

VI. Conclusion

We demonstrate in this paper that the use of a mixed InP-InAlAs or InGaP-InAlAs drastically reduces the gate leakage current due to impact ionization in AlInAs/InGaAs HEMTs.

On the other hand, it is seen that the defects induced by growth interruption lower the sheet carrier density in the channel. All in-situ growth should avoid this drawback and lead to high grade devices.

Moreover, we show that HEMT devices are very sensitive as test structures to study defects induced by a growth interruption. Such measurements can be very helpfull to optimize the technology of optoelectronic integrated circuits.

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Sample S2 contains much less levels as S1 or S3. This result is in good agreement with the values of n_s and μ_n of S2, which are the best of the three samples. As the regrowth procedure is more adapted to S2 sample (see section I), we can assume that the great number of deep levels in S1 and S3 are due to defects induced by the regrowth intteruption (S1 and S3) and/or to defects in the InGaP layer (S3).

THE SUPPRESSION OF SWITCHING IN InP HBTs

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Introduction

In this paper we examine the dc characteristics of InP/InGaAs double heterostructure bipolar transistors with differing collector designs. We show how the switching characteristics of devices with abrupt undoped InGaAs/InP heterojunctions in the collector, although providing an interesting device physics, can almost be eliminated by using dipole doping at the collector heterojunction. The high frequency performance is also improved with the dipole doping.

I. Background

In InP heterostructure bipolar transistors (HBTs) the narrow bandgap of the lattice-matched InGaAs can lead to the device having breakdown voltages which are only a few volts. To address this problem a thick InGaAs collector layer can reduce the electric fields in the collector of the device to enhance the breakdown performance, but possibly at the expense of the high frequency performance. Alternatively a composite-collector structure incorporating InP can be used - in this case the energy barrier at the InGaAs/InP heterojunction in the collector can degrade the dc performance at high current densities, and also cause switching behavior [1,2]. The collector barrier blocks electron flow when it extends above the base conduction band, for the case of ballistic electrons and also when the electrons are thermalized.

The switching arises from a complicated competition between tunneling and thermionic emission of electrons across the heterojunction in the collector. The switching is, in general, related to the existence of S- or N-shaped negative differential conductivity (NDC) and leads to hysteresis in a voltage-controlled experiment. In this case it is S-shaped NDC. The effect is best seen in common-base characteristics. There are various approaches to reducing the effects of the energy barrier at the InGaAs/InP interface, including δ-doping [3] and grading of the junction [4]. Here we show how dipole-doping [5] at the InGaAs/InP interface can eliminate the switching and improve the dc characteristics.

II. Epitaxial wafer structure

Table 1 shows the details the epitaxial layer structure, grown by gas-source MBE by Tutcore Ltd., that was used for the normal double HBT devices. InGaAs is the lattice-matched alloy $In_{0.53}Ga_{0.47}As$. The emitter design is similar

Table 1. Epitaxial layer structure

Material	Thickness (μm)	Doping	Density (cm^{-3})
InGaAs	0.10	n (Si)	2×10^{19}
InP	0.06	n (Si)	2×10^{19}
InP	0.09	n (Si)	3×10^{17}
InGaAs	0.01	undoped	-
InGaAs	0.05	p (Be)	2×10^{19}
InGaAs	0.05	n (Si)	5×10^{15}
InP	0.30	n (Si) or dipole - doped	5×10^{15}
InP	0.008	n (Si)	5×10^{18}
InGaAs	0.45	n (Si)	5×10^{18}
InP	substrate	SI (Fe)	-
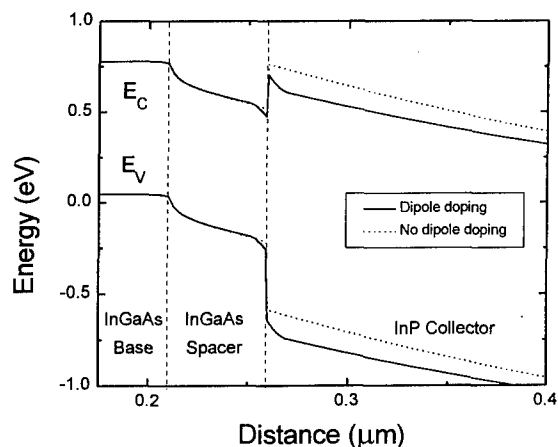
Fig. 1. Band diagram (from base to collector) for the 2 layer structures, showing how the dipole doping at the collector heterojunction alters the barrier to electrons.

to that for normal high performance InP HBTs. Similar comments apply to the choice of base width and doping. The collector structure incorporates a spacer layer of InGaAs between the base and the InP in the collector. It is known that narrow layers of acceptors and donors placed close together, a configuration called dipole doping [5] can increase the electric field over a thin layer and narrow the energy barrier at a heterojunction. The two layer designs only differ in the doping at the InGaAs/InP heterojunction in the collector. In one wafer, referred to as "undoped collector" below, the collector was uniformly doped to 5×10^{15} cm^{-3}. In the other, referred to as "dipole-doped", extra doping was added near the InGaAs/InP interface. The last 10 nm of InP before the InGaAs/InP interface was n-doped to 10^{18} cm^{-3} (producing an areal density of 10^{12} cm^{-2}), and the first 10 nm of InGaAs after the interface was p-doped to the same level.

As the calculated band diagram (Fig. 1) shows the dipole doping at the InGaAs/InP interface narrows the barrier to the point that electrons should be able to tunnel through the top part of it.

III. Results and Discussion

Using these wafers described in the previous section we fabricated large-area devices, which had a triple-mesa structure and Ti-Pt-Au metallized contacts. They were probed directly. The emitter areas were typically in the range 50 x 50 to 70 x 90 μm^2.

In Fig. 2 we show Gummel plots for large-area devices with identical emitter areas, made from the two different epitaxial structures. The results are almost identical for these room temperature characteristics, showing that the emitter and base structures are essentially the same and that
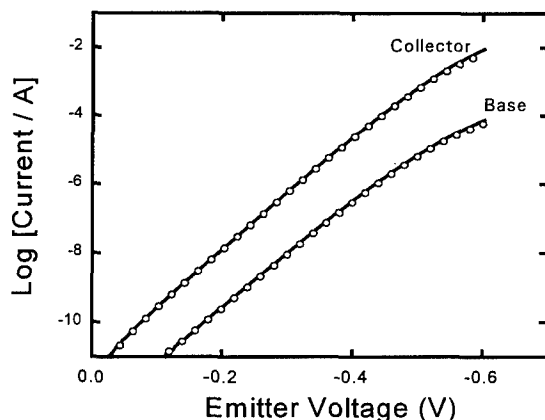
the device fabrication was reproducible. The dc gain at V_{BE} = 0.5 V was ~ 90. For these measurement V_{CB} was 0 V. For both layer designs the breakdown voltages at room temperature exceeded 8V - this shows the normal improvement in breakdown voltage by using a double heterostructure design.

As the devices are cooled down the characteristics for the undoped collector change dramatically. For instance the common-base characteristics at 100 K for the undoped collector structure shows the switching behavior which has been referred to above. At low V_{CB} the collector current I_C is significantly smaller than its ultimate value of $\alpha_0 I_E$. This reduction is due to the blocking effect of the collector heterojunction [6]. Electrons reaching the potential barrier in the collector are more likely to diffuse back into the base than to cross the barrier into the wide-bandgap InP. As V_{CB} increases, I_C increases, finally reaching $\alpha_0 I_E$ in a small jump. If V_{CB} is ramped down to 0 V from an initial value of 1.5 V the curves show the hysteresis which is the result of the underlying S-shaped nature of the I-V characteristic, which can be seen in a collector-current-controlled experiment [2]. The hysteresis is produced by the competition of the tunneling though the barrier and thermionic emission of hot electrons over the barrier in the collector [1]. The decrease of I_C with decreasing V_{CB} reflects both the increasing height and increasing width of the potential barrier in the collector. At the voltages where the vertical changes in I_C are seen (Fig. 3) the device is in a metastable state due to the competing mechanisms for electron transmission across the collector heterojunction. At voltages below the steps in these experiments the collector current does not follow the emitter current, as in a normal device, since here the emitter acts as a current source but the actual collector current is determined primarily by V_{CB}.
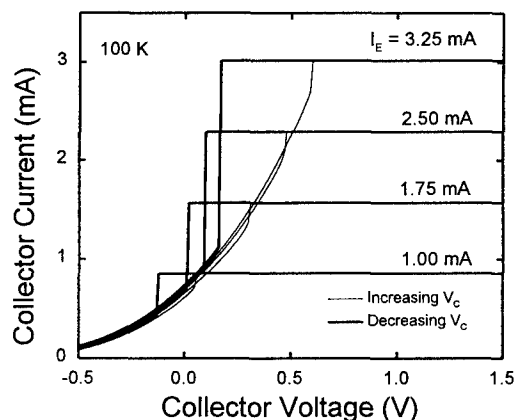

Fig. 2. Gummel plot at 295K for 50 x 50 μm^2 emitter devices with an undoped (line) or dipole-doped (points) collector structure.

Fig. 3. Common-base characteristics at 100 K for the device with the undoped collector structure, for various emitter currents.
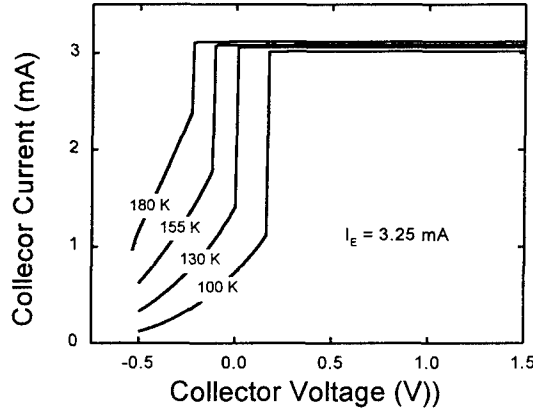
389

Fig. 4. Temperature dependence of common-base characteristics for the same device as in Fig. 3. Experiments done with decreasing V_C.

The switching and hysteretic behavior is observable over a large temperature range, extending to greater than 200 K. Fig. 4 shows the temperature dependence of the common-base characteristic for cases where V_{CB} decreases from 1.5 V to 0 V. The reduction in the current step suggests the increasing importance of thermionic emission. For a given barrier height and width the tunneling contribution is, to a first approximation, not temperature dependent whereas the thermionic contribution should increase as T increases. However the contribution from the tunneling may indeed not be temperature independent, since the shape of the band diagram near the collector heterojunction does not stay the same.
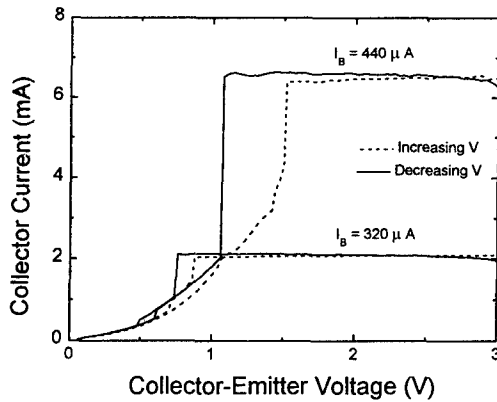
Fig. 5. Common-emitter characteristics at 100 K for the device with the undoped collector structure.

The common-emitter characteristics at low temperatures also show steps in the collector current but the results are often noisy (Fig. 5). This most probably occurs because the base-emitter voltage is not constant during a common-

emitter sweep. This implies that the base-collector voltage is not controlled which could lead to the collector blocking effect being slightly unstable.

The effect of the dipole doping on the common-base characteristics can be seen in Fig. 6. Here, for a range of temperatures from 100 to 295 K, the shape of the curves is similar, and there is no evidence of the current-blocking, switching and hysteresis as seen for the previous device. The common base gain α_0 increases with increasing temperature, as in the undoped devices at larger biases. The knee in the common-base curves at $V_{CB} < 0$ V is related to the diode characteristic of the base-collector junction. At zero emitter current the common-base characteristic is the diode characteristic for the base collector. Thus from Fig. 6 we see that the turn-on voltage for the base-collector diode, when forward biased, increases with decreasing T, which is to be expected.
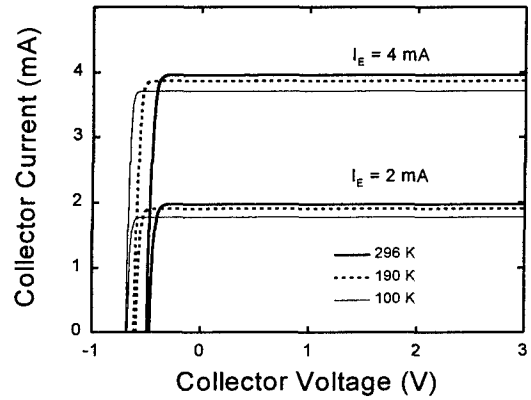
Fig. 6. Common-base characteristics for a device with the delta-doped collector structure.
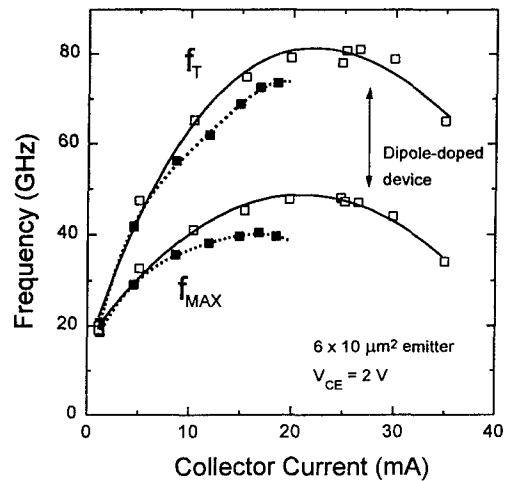
Fig. 7. Collector current dependence of f_T and f_{MAX} for the devices with undoped and dipole-doped collectors.

390

When composite-collector HBTs show switching or current blocking because of the collector heterojunction the high speed performance can be compromised. As a result of the current blocking, a large concentration of electrons builds up in the potential well formed at the barrier in the collector [4]. This extra stored charge will increase the charging time of the device and so reduce its high frequency performance. Fig. 7 compares the variation of f_T and f_{MAX} for devices with and without the dipole-doped collector structure. Devices with dipole doping perform well achieving a maximum in f_T of approximately 80 GHz for a 6 x 10 μm^2 device. Moreover the values of f_T at a given collector current are above the corresponding value for the device without dipole doping, showing that the dipole doping reduces the stored charge in the collector.

IV. Conclusions

We have demonstrated how interesting switching behavior found in composite-collector DHBTs can be eliminated by dipole-doping at the collector heterojunction. This leads to better dc and high frequency performance.

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NUMERICAL MODELING AND DESIGN OF Pnp InAlAs-InGaAs HETEROJUNCTION BIPOLAR TRANSISTORS

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Abstract

Pnp InAlAs/InGaAs heterojunction bipolar transistors have been studied using a two dimensional, numerical approach based on a commercial simulator. Initial simulation results have shown good agreement with the available experimental data. This paper examines the effects of the epitaxial layer parameters and optimization of the transistor's multi-layer epitaxial structure. Due to the small hole diffusion length, base widths approaching 30 nm are needed to achieve significant current gain (> 100) and large f_T (> 10 GHz). The high majority carrier electron mobility in the base allows the base resistance to remain small as the base width and doping are reduced so that an f_T greater than 20 GHz and an f_{max} greater than 30 GHz are possible.

I. Introduction

InP-based Pnp heterojunction bipolar transistors (HBTs) have recently been demonstrated operating at microwave frequencies (1,2). The devices are of interest for incorporation with Npn HBTs in complementary HBT-based circuits where the Pnp can serve as an active load device (3), in push-pull amplifiers (4) and for power applications where the device's low base resistance reduces emitter current crowding effects (5). To date, there have been few attempts at modeling of these devices (6,7).

In this work Pnp InAlAs/InGaAs heterojunction bipolar transistors have been studied using a commercial simulator based on a drift-diffusion model (8) in order to investigate their design and performance optimization. Device analysis was achieved by self-consistent numerical solution of the Poisson, carrier continuity and current density equations in two dimensions subject to the device's geometry and boundary conditions imposed by the device's contacts and biasing. Physical models incorporated in the simulation include the effects due to carrier degeneracy and generation-recombination mechanisms (SRH, optical, Auger and surface). For the carrier mobilities, an empirical model for the doping dependence following Caughey-Thomas (9) was used and fit to the available experimental data (7). Velocity saturation effects were also included. Similarly, the effects of doping on the minority carrier lifetime in the base were incorporated (7). The presence of light and heavy holes was taken into account by assuming a single type of hole with an effective mass given by the density of states effective mass. Contact resistances were included for the

device contacts using a contact resistivity of $1x10^{-7}$ Ωcm^2 for n-type contacts and $4x10^{-7}$ Ωcm^2 for p-type contacts (1). For devices with quaternary layers, the layer properties were estimated from the ternaries using Vegard's Law.

II. Simulation Results

Initially, the accuracy of the model was tested by comparing the simulation results with experimental measurements reported earlier on prototype devices where the epitaxial structure was that shown in Figure 1 (1). For simulation purposes, in place of the graded layer at the emitter-base interface, a set of two quaternary layers of intermediate compositions (40 and 60% GaAs) were employed with thicknesses of 15 nm each and dopings of $8x10^{17}/cm^3$ and p and n-type, respectively. Good agreement of the simulation results was found with the available experimental data for the current gain, cutoff frequency f_T and maximum frequency of oscillation f_{max} as a function of the collector current density as reported earlier (6).

In this paper, the design of the epitaxial structure for the Pnp HBT is examined. In particular, the effects of the base doping and width and collector doping on the current and power gain and microwave performance are examined. Shown in Figure 2 are the current and power gain as a function of the base width for a $2x10$ μm^2 emitter device biased at a collector current density of $1.1x10^4$ A/cm^2 for a fixed base doping of $8x10^{17}/cm^3$. The remainder of the device structure is the same as that shown in Figure 1. As can be seen, the small signal

GHz as the base width decreases from 65 to 32 nm as the base transit time decreases. Over the same range of base widths, the f_{max} is nearly constant near 26 GHz until it begins to drop abruptly for base widths less than 35 nm, which is due to an increase in the base resistance.
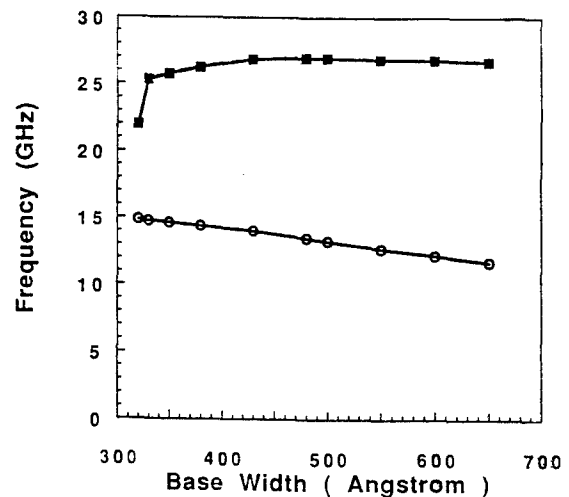
p+ InGaAs	$1x10^{19}$	0.135 u	Emitter Contact
p+ InAlAs	$2x10^{18}$	0.05 u	Emitter
p InAlAs	$8x10^{17}$	0.11 u	Emitter
p-n InGaAlAs		0.03 u	Graded Layer
n+ InGaAs	$7x10^{18}$	0.033 u	Base
p- InGaAs	$1x10^{17}$	0.25 u	Collector
p+ InGaAs	$5x10^{18}$	0.7 u	Subcollector
I InGaAs			Buffer
I InP			Substrate

Figure 1 Epitaxial structure of Pnp InAlAs/InGaAs HBT with quaternary emitter-base graded layer after Stanchina et al. (1).

current rises sharply as the base width decreases from 65 to 32 nm. Because of the low hole mobility and diffusion length in the base, base widths a factor of two or smaller than for the Npn device are needed. The power gain for the Pnp is large (30 dB) and nearly constant independent of the base width because the large majority carrier electron mobility in the base keeps the base resistance small which reduces current crowding (5). No self-heating effects were included in this analysis, which may reduce the power gain from this projection.

Figure 3 Calculated cutoff frequency (O) and maximum frequency of oscillation (■) as a function of base width for a fixed base doping of $7x10^{18}$/cm^3.

The effects of base doping on the device performance were also investigated. Shown in Figure 4 are the small signal current and power gain as a function of the base doping for a fixed base width of 33 nm. The current gain falls dramatically as the base doping increases from $2x10^{18}$/cm^3 to $7x10^{19}$/cm^3 due to the degrading effects of heavy doping on the hole mobility and minority carrier lifetime, and hence the diffusion length, in the base. As before, the power gain is large and nearly constant at 30 dB.

Figure 2 Calculated small signal current gain (O) and unilateral power gain (■) as a function of base width for a fixed base doping of $7x10^{18}$/cm^3.

Seen in Figure 3 are the cutoff frequency f_T and maximum frequency of oscillation f_{max} for the Pnp as a function of the base width for the same constant base doping and collector current density as above. At this high J_c ($1.1x10^4$ A/cm^2), the emitter and collector charging times are small, so the base transit and collector delay times dominate. The f_T increases steadily to 15

Figure 4 Calculated small signal current gain (O) and unilateral power gain (■) as a function of base doping for a fixed base width of 33 nm.

Seen in Figure 5 are the f_T and f_{max} for the Pnp HBT as a function of the base doping. The f_T decreases slightly as the base doping increases, but the f_{max} increases by nearly 50 % at the larger base doping levels. Since the f_T is nearly constant, the increase in f_{max} is due to a reduction in the base resistance.
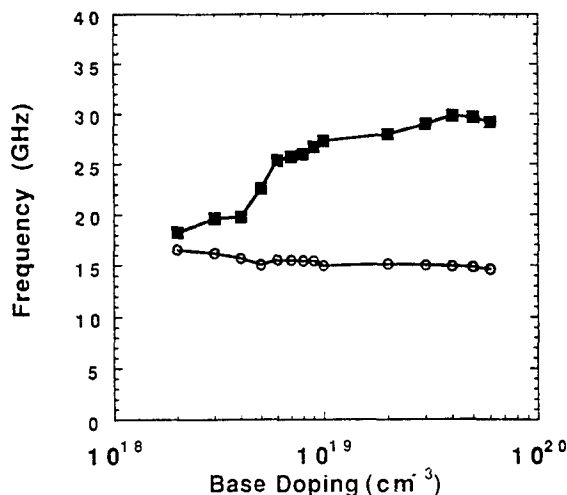

Figure 5   Calculated cutoff frequency (O) and maximum frequency of oscillation (■) as a function of base doping for a fixed base width of 33 nm.

The collector doping is also known to influence the high frequency performance of the device since it affects the collector series resistance and delay time. Shown in Figure 6 are the current and power gain as a function of collector doping for a fixed collector width of 250 nm and a collector current density of 1.1×10^4 A/cm^2. As the collector doping increases, the current gain rises more
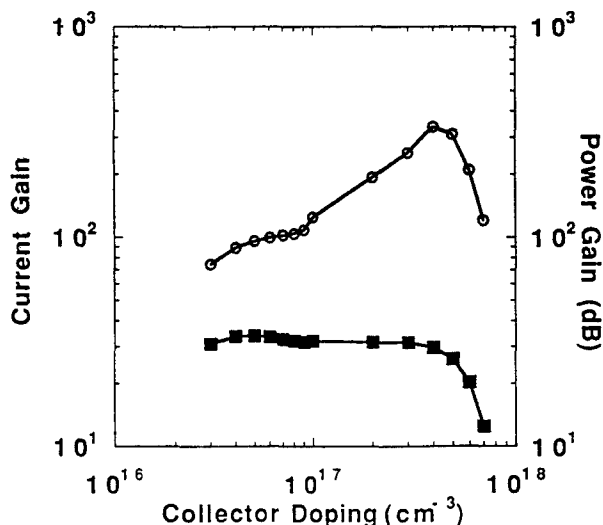
Figure 6   Calculated small signal current gain (O) and unilateral power gain (■) as a function of collector doping for a fixed collector width of 250 nm.

than fourfold from 75 at 5×10^{16}/cm^3 to a maximum of 335 at 4×10^{17}/cm^3 before falling off at higher doping levels. Due to the hole's smaller mobility, these results suggest that collector series resistance may be limiting the gain at the lower collector doping level. The power gain is relatively constant near 32 dB until it decreases sharply above 5×10^{17}/cm^3.

The effects of the collector doping on f_T and f_{Max} can be seen in Figure 7 for the same fixed collector width and collector current density. As the collector doping is increased, f_T increases nearly 35% from 12.5 GHz at 3×10^{16}/cm^3 to 17.5 GHz at 5×10^{17}/cm^3. For this device, the collector delay time is significant so the increase in collector doping produces a reduction in the base-collector space charge region width that results in a reduction in the collector delay time. At the same time, f_{Max} decreases dramatically from 29 GHz at a small collector doping to less than 3 GHz at 7×10^{17}/cm^3 as the collector capacitance increases.
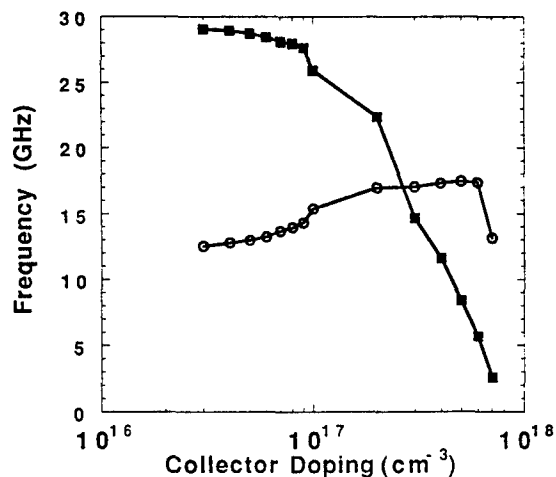
Figure 7   Calculated cutoff frequency (O) and maximum frequency of oscillation (■) as a function of collector doping for a fixed collector width of 250 nm.

III. Discussion and Conclusions

The above described results demonstrate that InP-based Pnp HBTs can provide current and power gain comparable to Npn HBTs and to that of GaAs-based Pnp HBTs at microwave frequencies. For power applications, the Pnp may offer advantages over the Npn since the electron's high mobility keeps the base resistance small and reduces emitter current crowding (5).   The power gains reported here are comparable to those reported recently for AlGaAs/GaAs Pnp HBTs (10) and InP/InGaAs double heterojunction NpN HBTs (11).

Device analysis shows that minority carrier hole transport across the base is an important factor limiting

394

high frequency performance. The hole mobility is dramatically lower (by a factor of about 40) than that for electrons at the same doping level and so the hole diffusion constant in the base is corresponding smaller. Hence, a reduced base width (< 50 nm) is needed to get sufficient current gain and microwave performance. For the Pnp HBT, the high majority carrier electron mobility in the base allows a reduction in the base doping from $5 \times 10^{19}/\text{cm}^3$ to $2 \times 10^{18}/\text{cm}^3$ without increasing the base resistance excessively, which helps to compensate for the low hole mobility and diffusion constant.

What is somewhat surprising for the Pnp HBT is that the low hole mobility does not preclude significant current gain for the device. For the device of Stanchina et al. (1) whose structure is seen in Figure 1, the base width is 33 nm, which is only a factor of 2 to 3 less than typically employed in Npn InP-based HBTs. Given that the hole mobility is so much smaller than that for the electron, the hole diffusion length is expected to be correspondingly smaller. However, the hole diffusion length is not proportionally as small (only a factor of about 2 smaller than the electron's) because it is also a function of the minority carrier lifetime as given by

$$L_p = \sqrt{D_p \tau_p} = \sqrt{\frac{k_B T}{q} \mu_p(N_D) \tau_p(N_D)}$$

(1)

where both the mobility and lifetime are functions of the doping. Similar to the doping dependence of the lifetime for holes described above, the electron lifetime in the p^+ base for Npn transistors can be modelled as a function of doping. In the electron's case, the fit parameters are $\beta = 12.6$ and $\gamma = 0.73$ for $N_A > 8 \times 10^{17}/\text{cm}^3$; for lower doping levels, the lifetime is a constant at 0.3 nsec (12). Based on the hole lifetime model presented earlier, for a base doping of $1 \times 10^{19}/\text{cm}^3$, the hole lifetime is found to be significantly larger than that for electrons, 0.40 nsec versus 0.05 nsec, respectively. As a consequence, the hole diffusion length in the base is not as severely reduced as might be expected by the smaller hole mobility. For the base doping of $1 \times 10^{19}/\text{cm}^3$ considered above, the hole diffusion length is only approximately a factor of two smaller than that for the electron, 0.30 μm versus 0.70 μm, respectively. Hence, assuming the above described mobility and lifetime models are accurate, Pnp HBTs with a reasonable gain comparable with that for the Npn can be expected for devices with base widths approxi-mately a factor of two smaller than typically used in Npn HBTs. The experimental results achieved by Stanchina et al. (1) and Lunardi et al. (2) for prototype devices support this conclusion.

Acknowledgment

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High-Power High-Speed $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ Doped-Channel FET's

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Introduction

The *first* $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ ($0 \le x \le 0.22$) doped-channel FET's (DCFET's) grown by GSMBE exhibiting excellent dc and microwave characteristics were successfully fabricated. A high g_m of 306 mS/mm, a high f_t of 21.7 GHz and a high f_{max} of 53.4 GHz were achieved at 300 K for a $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET with a 1 μm-long gate. This device also showed a very high maximum current density (630 mA/mm) and a very high drain-source operating voltage (13 V). These values were quite high compared with other works of InGaAs channel DCFET's and HEMT's with same gate length. Moreover, wide and flat characteristics of g_m, f_t and f_{max} versus drain current (or gate voltage) were attained for all DCFET's. Power performance of $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET's, $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ DCFET's and HEMT's were calculated. It is found that $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET's provides the largest power among the three devices. These results demonstrate that high transconductance, high linearity, high speed and high output-power could be achieved by using $In_xGa_{1-x}As$ and $Ga_{0.51}In_{0.49}P$ as the channel and insulator materials, respectively.

I. Background

High electron mobility transistors (HEMT's) have demonstrated excellent performance in low-noise applications[1]. As for high-power applications, the heterostructure FET's (HFET's) based on an InGaAs pseudomorphic channel have shown extremely good power performance at millimeterwave frequencies due to high-current handling capability, high transconductance (g_m), and good electron confinement by the potential well [2],[3]. It has been demonstrated that the current-drivability and g_m of metal/i-AlGaAs/n-InGaAs/i-GaAs quantum well MISFET's with doped InGaAs channel were higher than those of metal/i-AlGaAs/i-InGaAs/n-GaAs quantum well MISFET's with undoped InGaAs channel [3]. Therefore, we would like to study the performance of the metal/i-GaInP/n-InGaAs/i-GaAs doped-channel FET's (DCFET's). There are several advantages by using the GaInP/InGaAs/GaAs material system compared with AlGaAs/InGaAs/GaAs system : 1) the etching selectivity between $Ga_{0.51}In_{0.49}P$ and GaAs is very high and therefore gate recess will stop at the undoped $Ga_{0.51}In_{0.49}P$ layer automatically and exactly, which means high uniformity and yield [4]; 2) the reliability should be better since $Ga_{0.51}In_{0.49}P$ has very low

reactivity with oxygen [4],[5]; and 3) the 1/f noise is lower due to smaller surface recombination [6]. Hence, in this paper, we report the peformance of the $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As/GaAs$ DCFET's and compared them with other works of InGaAs channel DCFET's and HEMT's.

II. Experimental Details

The $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ DCFET structure shown in Fig. 1(a) was grown by GSMBE. First, a 5000 Å undoped GaAs buffer layer was grown on a (100) GaAs semi-insulating substrate, followed by a 150 Å $In_xGa_{1-x}As$ n channel layer (3×10^{18} cm^{-3}, Si doped). Then a 200 Å undoped $Ga_{0.51}In_{0.49}P$ insulator layer was grown on top of the active channel. Finally, a 400 Å n$^+$ GaAs cap layer was grown. Conventional optical lithography and mesa type wet etching technique were used to fabricate the $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ DCFET's [7]. After the GaAs cap layer was selectively etched, 1 μm-long, 150 μm-wide Ti/Pt/Au (500 Å /500 Å / 6000 Å) traditional gates were evaporated and defined by a lift-off process. The recess length between gate-drain and gate-source were 2 μm and 1 μm, respectively, as shown in Fig. 1(a). Fig. 1(b)

is the schematic conduction-band diagram of the $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET's. Because the gate is sitting directly on the *undoped* high bandgap $Ga_{0.51}In_{0.49}P$ insulator layer (1.92 eV) with reasonably high Schottky barrier (0.87 eV) [8] and conduction band discontinuity at the $Ga_{0.51}In_{0.49}P$ /$In_{0.2}Ga_{0.8}As$ heterojunction is also large (~ 0.36 eV) [8],[9], higher gate turn on voltage, breakdown voltage and current drivability, as compared to MESFET's and HEMT's, can therefore be expected. The measured gate turn on voltage of $Ga_{0.51}In_{0.49}P$ /$In_{0.2}Ga_{0.8}As$ DCFET's was 1.05 eV. This value is comparable to that (1.0 eV) of $Al_{0.3}Ga_{0.7}As$ /$In_{0.2}Ga_{0.8}As$ DCFET's and better than that (0.65 eV) of $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ HEMT's [10].

Source   Gate   Drain
AuGeNi $L_g = 1$ μm   AuGeNi

(a)

(b)
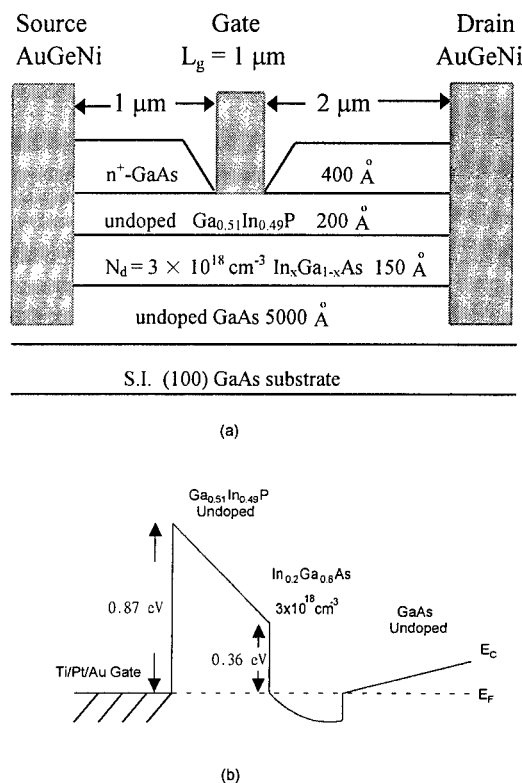
Fig. 1(a) Device cross-section of $Ga_{0.51}In_{0.49}P/$ $In_xGa_{1-x}As$ DCFET's and (b) conduction band diagram of the $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET's.

III. Results and Discussions

A. DC Characteristics

I-V characteristics of $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ ($0 \leq x \leq 0.22$) DCFET's were measured with an HP4156 precise semiconductor parameter analyzer. Typical drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) characteristics of an

x=0.20 DCFET is shown in Fig. 2(a). Note that the device could be operated up to I_{ds} = 630 mA/mm and V_{ds}=13 V at V_{gs}=1V. This is attributed to the high-quality *undoped* high-bandgap $Ga_{0.51}In_{0.49}P$ insulator layer, which could sustain a very high breakdown field at the gate edge nearest to the drain. A peak g_m of 306 mS/mm was also achieved at V_{ds} = 3 V. The output conductance (g_{ds}) at V_{gs}= 0 V was 2.1 mS/mm and therefore a high dc gain ratio (g_m/g_{ds}) of 147 was obtained. The I_{ds} dependence of g_m for $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET's and $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ DCFET's and HEMT's [11] were shown in Fig. 2(b). As can be seen clearly, the characteristics curve of g_m versus I_{ds} for $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET's and $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ DCFET's extended not only to higher I_{ds} values but also exhibited flatter g_m characteristics with wider drain bias current conditions, namely, 365 mA/mm for $Ga_{0.51}In_{0.49}P$ /$In_{0.2}Ga_{0.8}As$ DCFET's and 360 mA/mm for $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ DCFET's in contrast with 150 mA/mm for $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ HEMT's. The " width " of flat region was defined as the difference of two current densities corresponding to 10% drop from the maximum g_m. The above results demonstrated that doped-channel MIS-like structure indeed could achieve higher current drivability and better linearity [7],[11].

Due to the high etching selectivity between GaAs cap layer and $Ga_{0.51}In_{0.49}P$ insulator layer, the standard deviation of the threshold voltage of our fabricated DCFET's was low to 50 mV. This value was comparable to that (60 mV) of GaInP/AlGaAs/InGaAs HJFET's fabricated by selective wet etching and less than one sixth of that of the conventional AlGaAs/InGaAs HJFET's [12], indicating great potential in using a highly-selective etching technique for high-uniformity and high-yield device production. Recent reports have shown that GaInP/GaAs devices guarantee a mean time to failure (MTTF) of 10^8 hours (at a junction temperature of 125 °C) [4] and at least 10^6 hours at a junction temperature of 200 °C [5], which is enough for a 25-year lifetime requirement of a practical system and suggests high reliability of GaInP/GaAs devices. From the above results, $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ material system should be a good alternate to AlGaAs/InGaAs system.

Table I summarizes the dc characteristics of $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ ($0 \leq x \leq 0.22$) DCFET's with 1.0 μm-long gate at room temperature. We observed an enhancement of $g_{m,ext}$ from 180

397

(a)

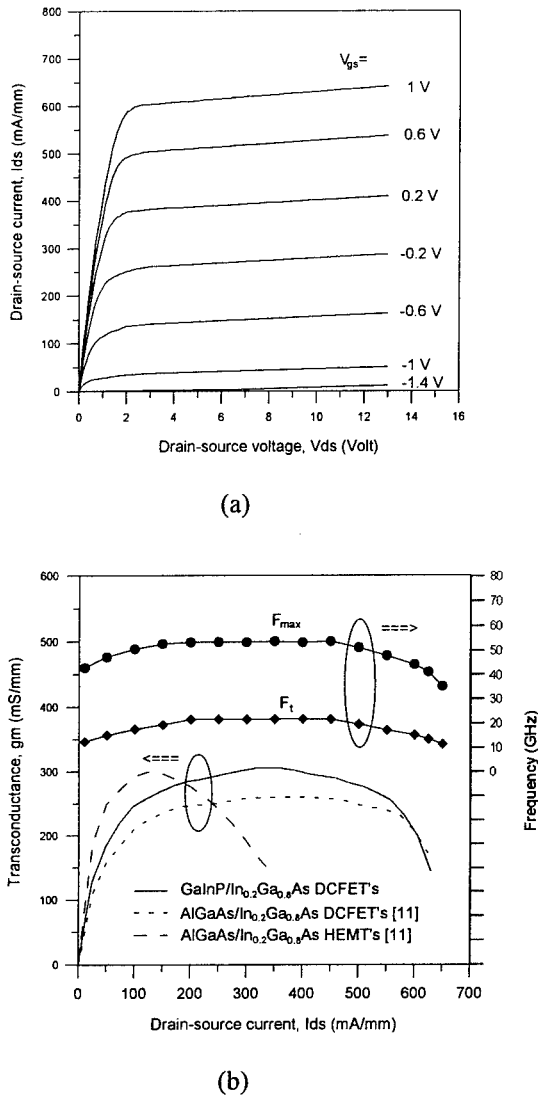(b)

Fig. 2(a) Typical I_{ds} v.s.V_{ds} characteristics of the $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET and (b) g_m, f_t and f_{max} v.s. I_{ds} characteristics of $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET's.

Table I
DC characteristics of $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ ($0 \leq x \leq 0.22$) DCFET's with 1.0 µm-long gate.

In content	x=0	x=0.15	x=0.20	x=0.22
$g_{m,ext}$ (mS/mm)	180	350	306	275
$I_{ds, max}$ (mA/mm)	465	575	630	585

mS/mm for x=0 - 350 mS/mm for x=0.15 DCFET's. However, $g_{m,ext}$ values dropped to 306 mS/mm for x=0.20 and 275 mS/mm for x=0.22 DCFET's. The

optimum performance of $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ DCFET's is obtained with the x value ranging between x=0.15 and x=0.20 for 150 $\overset{\circ}{A}$ thick $In_xGa_{1-x}As$ channel layer and 200 $\overset{\circ}{A}$ thick $Ga_{0.51}In_{0.49}P$ insulator layer.

B. Microwave Characteristics

Microwave on wafer S-parameters, for 1.0 µm-long gate $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ ($0 \leq x \leq 0.22$) DCFET's were measured from 45 MHz to 26.5 GHz with an HP8510C network analyzer. Fig. 3 shows the current gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) of x = 0.20 $In_xGa_{1-x}As$ channel DCFET's were 21.7 and 53.4 GHz respectively under the bias conditions of V_{ds} = 3 V and V_{gs} = 0 V. The f_t (21.7 GHz) of $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET's was higher than those of $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ DCFET's (12 GHz) and HEMT's 14.5 (GHz) with 1.0 µm-long gate [10]. Moreover, the f_{max} (53.4 GHz) of our $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET was comparable to those of $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ DCFET's (50 GHz) and HEMT's (50 GHz) with 1.0 µm-long gate [10]. The higher f_t performance of our $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET versus $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ DCFET (with same insulator thickness 200 $\overset{\circ}{A}$) was mainly attributed to higher g_m due to higher mobility (3090 cm²/V-sec for our DCFET versus 1810 cm²/V-sec for $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ DCFET) [10]. The mobility difference could be due to different growth techniques used. Though the mobility of our $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET was lower than that (3800 cm²/V-sec) of $Al_{0.3}Ga_{0.7}As$ /$In_{0.2}Ga_{0.8}As$ HEMT, the g_m of our DCFET's was still larger than its due to the higher product of mobility and sheet charge density. Moreover, the lower gate-source and gate-drain capacitances of our $Ga_{0.51}In_{0.49}P/In_{0.2}Ga_{0.8}As$ DCFET (C_{gs} = 2023.2 fF/mm and C_{gd} = 157.8 fF/mm versus C_{gs} = 3030 fF/mm and C_{gd} = 190 fF/mm of $Al_{0.3}Ga_{0.7}As$ /$In_{0.2}Ga_{0.8}As$ DCFET and C_{gs} = 2850 fF/mm and C_{gd} = 250 fF/mm of $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ HEMT) also benefit the high f_t performance.

Table II summarizes the RF characteristics of the $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ ($0 \leq x \leq 0.22$) DCFET's with 1.0 µm-long gate at room temperature. The optimum performance of f_t's and f_{max}'s both occured when the x value ranging between x=0.15 and x=0.20 for 150 $\overset{\circ}{A}$ thick $In_xGa_{1-x}As$ channel layer and 200 $\overset{\circ}{A}$ thick $Ga_{0.51}In_{0.49}P$ insulator layer.

398
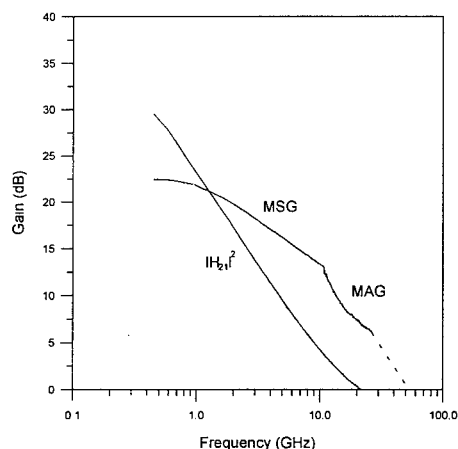
Fig. 3 Microwave characteristics of $Ga_{0.51}In_{0.49}P/$ $In_{0.2}Ga_{0.8}As$ DCFET's with 1 μm-long gate.
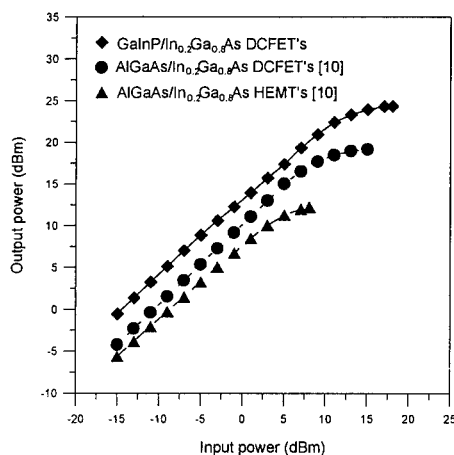
Fig. 4 Power performance of $Ga_{0.51}In_{0.49}P/$ $In_{0.2}Ga_{0.8}As$ DCFET's, $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ DCFET's and HEMT's at 2.4 GHz. (gate dimension: 1×100 μm^2)

Table II
RF characteristics of $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ ($0{\leq}x{\leq}0.22$) DCFET's with 1.0 μm-long gate.

In content	x=0	x=0.15	x=0.20	x=0.22
f_t (GHz)	17.6	23.3	21.7	19.1
f_{max} (GHz)	34.9	50.8	53.4	46.8

IV. Conclusions

In summary, the $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ DCFET's ($0{\leq}x{\leq}0.22$) grown by GSMBE were fabricated successfully and easily because of the high etching selectivity between $Ga_{0.51}In_{0.49}P$ and GaAs. Due to superior transport properties of

$In_xGa_{1-x}As$ ($0.15{\leq}x{\leq}0.2$), high-quality *undoped* high bandgap $Ga_{0.51}In_{0.49}P$ insulator layer, large Schottky barrier and $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ conduction band-offset, high g_m, high current drivability, high operating voltage, high output-power and high-speed were achieved. Therefore, $Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As$ ($0.15{\leq}x{\leq}0.2$) DCFET's will be very promising candidates for microwave power application.

Acknowledgement

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DRAIN ENGINEERING IN AlInAs/GaInAs HEMTs
FOR HIGH f_τ AND f_{max}

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Introduction

We propose a novel lateral bandgap engineering technique to improve electron transport in the channel of an AlInAs/GaInAs HEMT. Electrons are launched at the source with higher velocity by a launcher (higher bandgap AlInAs source) and collected at the drain by a heterojunction collector (lower bandgap InAs drain). The resulting device, a **Lateral Bandgap Engineered HEMT (LBE-HEMT)**, is analyzed using DAMOCLES, a 2-D Ensemble Monte Carlo and Poisson Simulator. Electron velocity profiles in the GaInAs channel are generated using DAMOCLES. Effect of band gap engineering on the electron velocity and its variation with drain bias is discussed. It is observed that the ensemble velocity of electrons in the channel is increased and velocity degradation at high drain biases (which are required to achieve a high f_{max}) is minimized. Thus the f_τ, f_{max} tradeoff in conventional FETs can be alleviated using lateral bandgap engineering,.

I. F_τ, F_{max} Tradeoff in FETs

Advances in materials and processing technology have made possible the fabrication of HEMTs with f_τ as high as 340 GHz (f_{max}=250 GHz) [1] and f_{max} as high as 600 GHz at Vds=2 V(f_τ=160 GHz at Vds=1 V) [2]. However it is difficult to simultaneously obtain a high f_τ and f_{max}. This is because a high f_τ requires a self-aligned FET structure which reduces the transit time in the gate-drain depletion region, however the reduced gate-drain separation increases the gate-drain capacitance C_{gd} which reduces the f_{max}. In a conventional HEMT in order to achieve a high f_{max} a high Vds is required which degrades the f_τ. High f_{max} can be achieved in self-aligned FET structure if the velocity in the channel is further increased to compensate the increase in C_{gd} and the velocity degradation with the increase in drain bias is reduced. In this paper we present a novel drain engineering technique which achieves the above objective alleviating the f_τ, f_{max} tradeoff in conventional HEMTs.

II. Lateral Bandgap Engineering

Figure 1 shows the schematic diagram of a conventional HEMT and a lateral-bandgap engineered
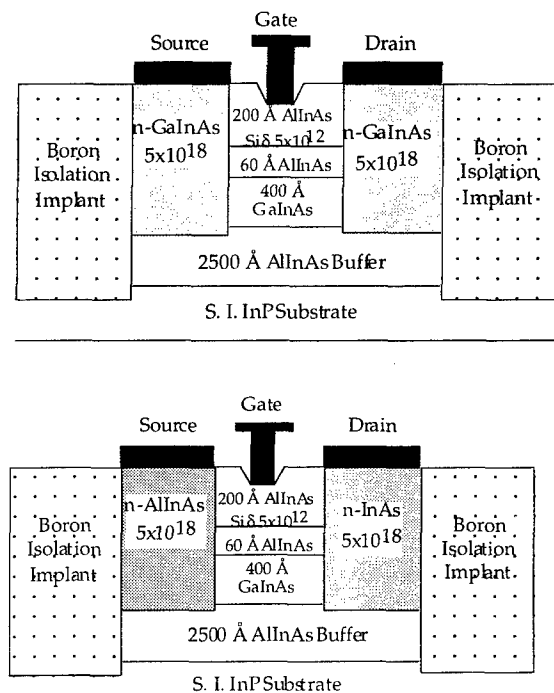

Fig. 1 Schematic diagram of conventional and LBE-HEMT.

HEMT (LBE-HEMT) which uses lateral band gap engineering to improve electron velocity in the channel. The AlInAs source acts as hot electron launcher and the InAs drain serves as a ideal collecting boundary. An ideal collecting boundary generated using an electric field step is shown to increase the ensemble velocity of electrons in the region before the step by Littlejohn et.al [3]. Figure 2 shows the band-diagram along the channel of a conventional and drain engineered HEMT, the band discontinuity between InGaAs and InAs at the channel-drain interface serves a better collection barrier than the conventional GaInAs drain. This improves the ensemble velocity of carriers under the gate and in the gate-drain depletion region. Also the InAs drain influences the electron transport in the gate-drain depletion region as discussed later in this paper.
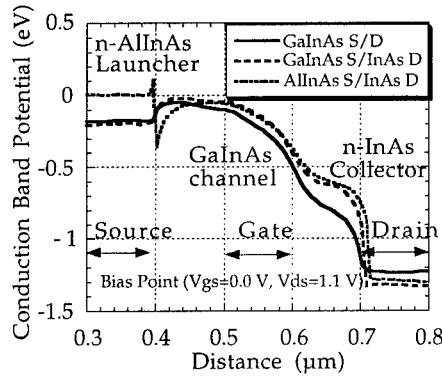
Fig. 2 Comparison of band diagram for conventional and LBE-HEMTs

The AlInAs source acts as a hot electron launcher. Thus it is possible to launch electrons at a higher velocity into the channel and further reduce the transit time. A hot electron launcher is ideally suited for the AlInAs/GaInAs HEMT (compared to GaAs-based HEMT) as the effective launching energy (0.25 eV) is less than the Γ-L separation (0.53 eV) in GaInAs. This ensures that the electrons do not undergo intervalley scattering before they reach the gate.

III. Monte Carlo Simulation Using DAMOCLES

Electron velocity profiles for conventional AlInAs/GaInAs HEMTs and AlInAs/GaInAs LBE-HEMTs were obtained by simulating the device structure (as shown in Figure 1) using DAMOCLES [4]. The total time for simulation at each bias point is 1.2 ps. The total number of electrons used for simulation is 10000 and Monte-Carlo time step is 0.9 fs. The gate length is 0.1 μm. The gate source

separation L_{gs} is 0.1 μm and the gate drain separation L_{gd} is 0.1 μm. In this study the parabolic band model was used to reduce the simulation time for each bias point. The velocity profiles were averaged over the simulation time of 1.2 ps. The scattering mechanisms used are phonon-scattering and electron-electron scattering.

IV. Effect of Lateral Bandgap Engineering on Electron Velocity in the channel

Figure 3 compares the velocity profiles in the channel for a conventional AlInAs/GaInAs HEMT with GaInAs source and drain (GaInAs S/D) and two LBE-HEMT structures one with AlInAs source and InAs drain (AlInAs S/InAs D) and the other with GaInAs source and InAs drain (GaInAs S/InAs D) at a bias of Vds=0.7 V and Vgs=0.0 V. It can be seen that the electron velocity under the gate is same for all the
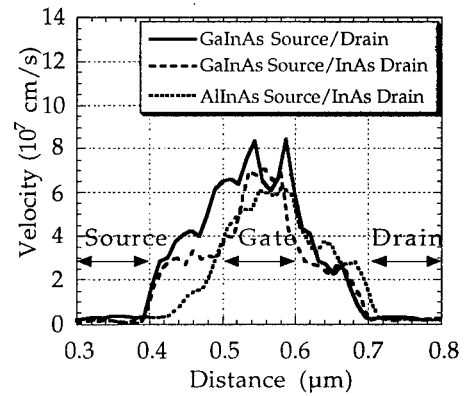

Fig. 3 Comparison of Velocity profiles at Vds=0.7 V, Vgs=0.0 V for conventional and LBE-HEMTs

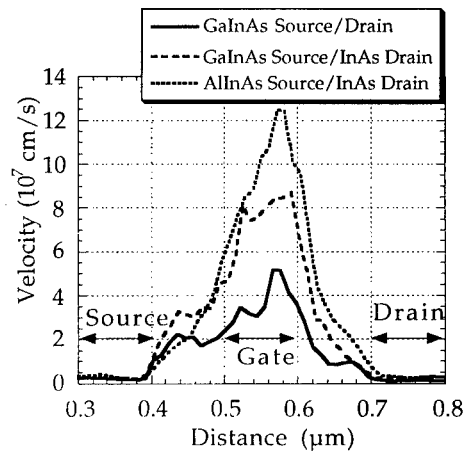*Fig. 4 Comparison of Velocity profiles at Vds=2.1 V, Vgs=0.0 V for conventional and LBE-HEMTs.*

three structures. However the velocity is higher in the gate-drain depletion region for LBE-HEMTs. Figure 4

compares the velocity profiles for the same structures at a drain bias of 2.1 V. It can be seen that electron velocity under the gate has reduced for the conventional FET.On the other hand the peak velocity under the gate has increased for the LBE-HEMT.

V. Variation of Velocity Profiles with Drain Bias.

Figure 5 shows the variation in the electron velocity in the channel as a function of drain bias for the conventional AlInAs/GaInAs HEMT. It can be seen that the electron velocity initially increases with drain bias due to the increasing electric field under the gate.

Fig. 6 Variation of electron velocity with drain bias for AlInAs Source/InAs Drain LBE-HEMT

Fig. 5 Variation of electron velocity with drain bias for conventional GaInAs/AlInAs HEMT

For a larger drain bias the electron velocity in the channel reduces due to intervalley scattering. Figure 6 shows the variation in the electron velocity as a function of bias for AlInAs/GaInAs LBE-HEMT. It can be seen that the electron velocity increases with drain bias. Figure 7 shows the electron velocity as function of bias for a LBE-HEMT with GaInAs source and InAs drain. The electron velocity under the gate is lower compared to LBE-HEMT with AlInAs launcher. In this case also the electron velocity increases with the drain bias.

The variation of electron velocity with drain bias in LBE-HEMTs shows a completely opposite trend when compared with conventional FETs. This explained by examining the manner in which the InAs drain changes the potential profile in the gate drain depletion region.

VI. Effect of InAs Drain on Electric Field in the Gate-Drain Depletion Region

It is evident from the velocity profiles in the channels that lateral bandgap engineering causes the electron velocity to increase with drain bias. Also it is
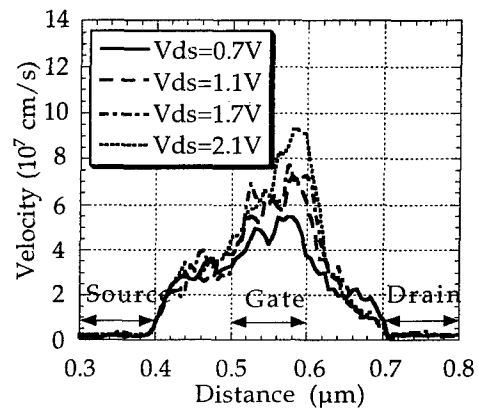
Fig. 7 Variation of electron velocity with drain bias for GaInAs Source/InAs Drain LBE-HEMT

observed that this effect is prominent at higher carrier velocities as seen when comparing LBE-HEMTs with and without AlInAs launchers in the source. The effect of InAs drain is understood by studying the potential and electric field profiles in the gate-drain region. Figure 8 shows the variation of potential in the gate drain region at a drain bias of 2.1 V and gate bias of 0.0 V for conventional and LBE HEMTs. It can be seen that the potential profiles under the gate are similar for the conventional and LBE-HEMTs. However in the case of LBE-HEMT with a InAs drain the potential drop in the gate-drain depletion region is concentrated near the GaInAs channel/InAs drain interface. The reduced potential drop in the gate-drain depletion region reduces the probability of intervalley scattering. The concentration of the potential drop near the channel drain interface and the band discontinuity at the channel-drain interface improves the electron transport in the gate-drain depletion region in three ways. First the
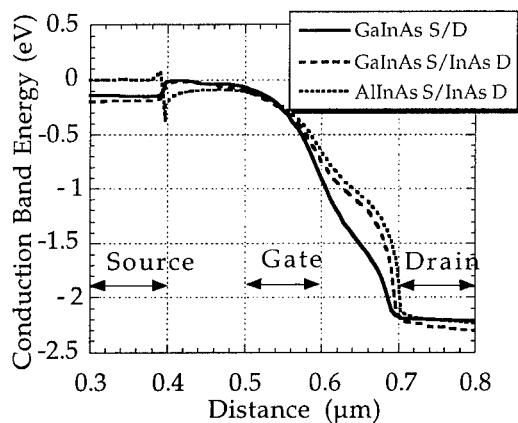
Fig. 8. Variation of Potential Profile in the channel at Vds=2.1 V.

barrier to backdiffusion of electrons in the channel is higher for the InAs drain HEMT. This also enables efficient collection of electrons by the drain. Also the electric field at the drain contact is higher resulting in increased velocity before the drain contact due to the ensemble effect as described before. This is evident from the electric field profiles as shown in Fig. 9.
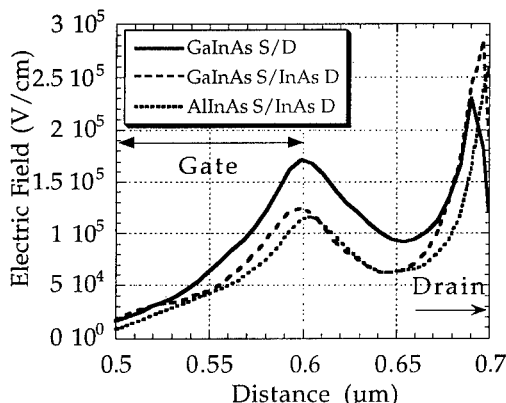

Figure 9. Variation of electric field in the gate-drain depletion region at Vds=2.1 V.

The electron velocity enhancement maintained even when the gate-drain separation is increased to 0.2 μm to reduce C_{gd} as seen in Figure 10. This modification of potential profile in the gate-drain region which results in the gradual accelaration and efficient collection of electrons is similar to the i-p$^+$-n collector structure in AlGaAs/GaAs HBTs as proposed by Ishibashi et.al. [5].

VII. Conclusions

We have demonstrated a novel lateral bandgap engineering technique to alleviate the f_t, f_{max} tradeoff in conventional FETs. Lateral bandgap engineering is achieved in a AlInAs/GaInAs HEMT by having a high
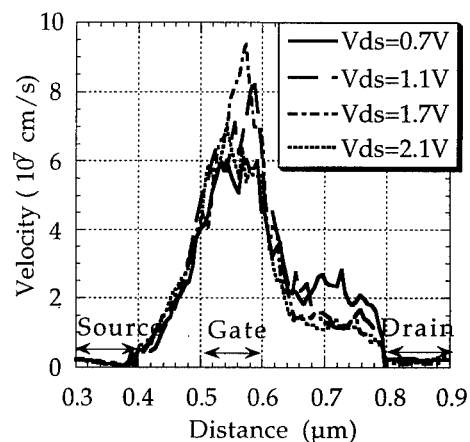
Fig. 10 Variation of electron velocity with Vds for AlInAs Source/InAs Drain LBE-HEMT(Lgd=0.2 μm)

bandgap AlInAs source acting as a launcher and a lower bandgap InAs drain acting as collector. The resulting structure causes the electron velocity to increase with increasing drain bias by modifying the potential profile in the gate-drain depletion region of the FET. This concept can be extended to other material systems like Si MOSFET with SiGe drain, as only a drain with lower bandgap than the channel is required.

Acknowledgement

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Semi-Insulating InP through Wafer Annealing

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ABSTRACT

Recent investigations in various affiliations opened a possibility for preparation of semi-insulating (SI) InP with extremely low Fe concentrations through wafer annealing procedures. In this paper, these investigations are reviewed including the latest data on 75mm diameter SI InP, and possible mechanisms of the SI behavior after wafer annealing are discussed.

1. Introduction

SI InP is becoming more and more an important material, not only for high frequency devices such as high-electron-mobility transistors (HEMTs) and hetero-bipolar-transistors (HBTs), with cut-off frequencies exceed 60GHz surpassing GaAs-based devices [1], but also for optical devices such as laser diodes (LDs) and photodetectors, whose transmission rates exceed several tens Gb/s[2].

SI InP had been industrially produced only by Fe doping with high Fe concentrations exceeding $10^{16}cm^{-3}$ (>0.2ppmw). This high Fe concentration will not be preferable because of lower crystal yield for limited Fe concentrations[3], low activation efficiency for ion implantation[4], a possibility of Fe atom diffusion from substrates into epitaxial layers[5,6], slip-like defect formation in epitaxial layers [7,8] and the formation of defects such as bright spots [7].

Undoped or extremely low Fe-doped SI InP was therefore desired. It is however known that undoped SI InP can not be achieved. In fact, for realizing SI InP without any native deep levels for pinning the Fermi-level, it is necessary that the residual carrier concentration be less than 10^7cm^{-3}, the purity of which is too high to realize by the-state-of-the-art technology. Since no native deep levels such as EL2 in GaAs are found in the case of InP, undoped SI InP seems to be impossible to prepare.

2. Preparation of SI InP by Wafer Annealing of Undoped Conductive InP

This belief has been however reconsidered after high resistive and SI InP could be obtained by annealing undoped conductive InP wafers as reported by various authors [9-21], especially after the first achievement of SI InP by Hofmann et al. [11]. In fact, 50mm diameter undoped SI LEC-InP could be obtained by annealing at 900°C under 15 atm phosphorus overpressure in our laboratory[12]. Fig. 1 shows a high pressure furnace for such wafer annealing under phosphorus overpressure.
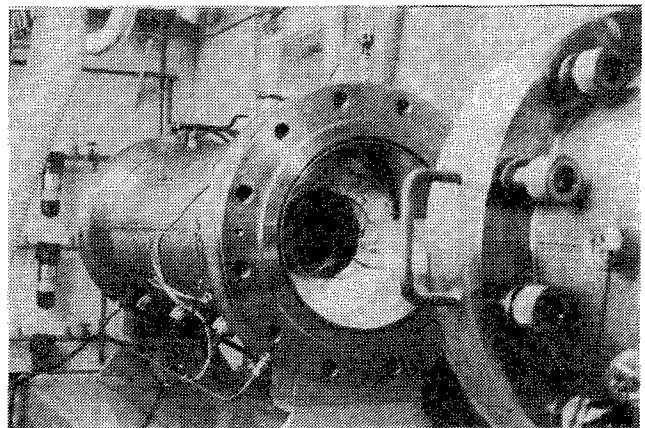
Further precise investigations clarified various facts.

Fig. 1. High pressure furnace for wafer annealing

(1) The purity of starting material largely affects the achievement of SI properties[11,13].

(2) Slight Fe contamination occurs during wafer annealing[13,19].

(3) There is hardly any effect of phosphorus over-pressure on the SI behavior [14].

(4) The reproducible preparation of SI InP is difficult when contamination by Cr and Ni is not prevented (Fig. 2) [19,20].

(5) Reproducible preparation of SI InP was achieved by annealing in vacuum [16-18].

(6) Hydrogen in InP can be removed by annealing [21].

Taking account of these facts, it became possible to prepare SI LEC-InP reproducibly by annealing InP wafers with extremely low Fe concentrations under low phosphorus vapor pressure [22-24]. A typical example is shown in Fig. 2 and Fig. 3. Hirt et al. also showed that wafer annealing could be successfully applied for converting conductive VGF-InP to SI [25].

3. Mulitple-step Wafer Annealing (MWA) Process for Uniformity Improvement

The SI InP thus prepared, however, does not have satisfactory resistivity uniformity [20]. In order to overcome this disadvantage, the Mulitple-step Wafer Annealing (MWA) process

Fig. 3. The relationship between resistivities and Fe concentrations

which has been first developed for GaAs [26] was applied to 50mm diameter InP by Uchida et al. [24,27]. The process consists of two-step wafer annealing, the first-step annealing for converting conductive InP wafers to SI and the second step annealing for improving the resistivity uniformity. By increasing the phosphorus overpressure up to 30atm during the second-step annealing, it
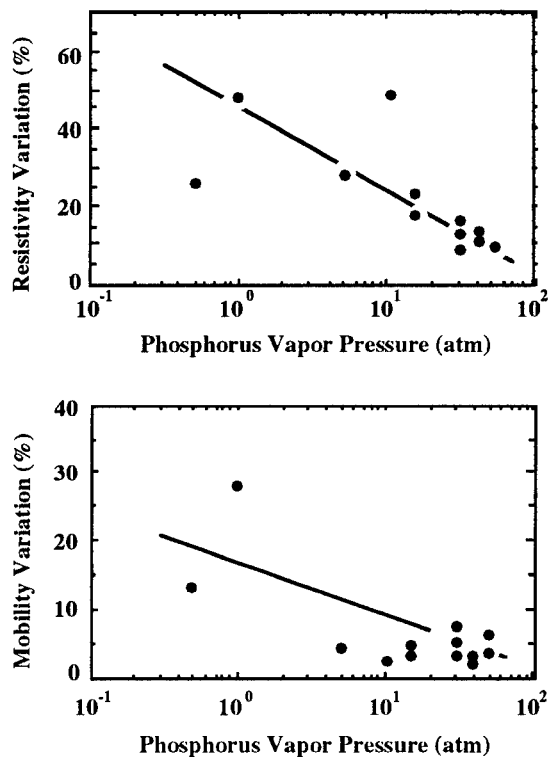

Fig. 2. Reproducible preparation of undoped SI InP

Fig. 4. Variations of electrical properties as a function of phosorus vapor pressure during the second-step annealing

was found that the resistivity and mobility uniformities could be largely improved (Fig. 4).

This MWA process has been applied even for 75mm diameter InP and it was found that the SI behavior and satisfactory uniformity can be obtained (Fig. 5).

4. Photoluminescence Examination

It was first found that annealing has an effect to give highly resolved spectra in the wavelength region of 870-1000nm[28]. Annealed InP also shows very interesting features. Makita et al. [29] and Yoshinaga et al. [30-31] reported that the resolution of photoluminescence spectra can be improved as the Fe concentration decreases. In their data, very strong peak due to phosphorus vacancies can be clearly seen. Uchida et al. [32] found that by MWA process, this line peak due to phosphorus vacancies is largely decreased after the second step annealing (Fig. 6). This implies clearly that wafer annealing at lower temperatures has an effect in reducing phosphorus vacancies.

5. Possible Mechanism of SI Behavior after Wafer Annealing

The mechanism of SI behavior has been extensively studied by various methods such as Hall effect [11], TSC[33], DLTS[34,35] and PL measurements [13,14]. The following three mechanisms have been proposed.

(1) Slight amount of Fe is activated by annealing and the concentration of shallow donors which may be mainly native defects such as phosphorus vacancies is decreased to the level less than the concentration of activated Fe [13, 19, 36].

(2) Shallow donors due to the complex defects (hydrogen-indium vacancy) can be eliminated by annealing to the extent less than the concentration of residual Fe [21].

(3) Indium related defects which act as shallow acceptors are created by low phosphorus vapor pressure annealing and they compensate residual shallow donors [17,18].

Among these mechanisms, the most probable one would be the activation of residual Fe and the reduction of phosphorus vacancies which act as
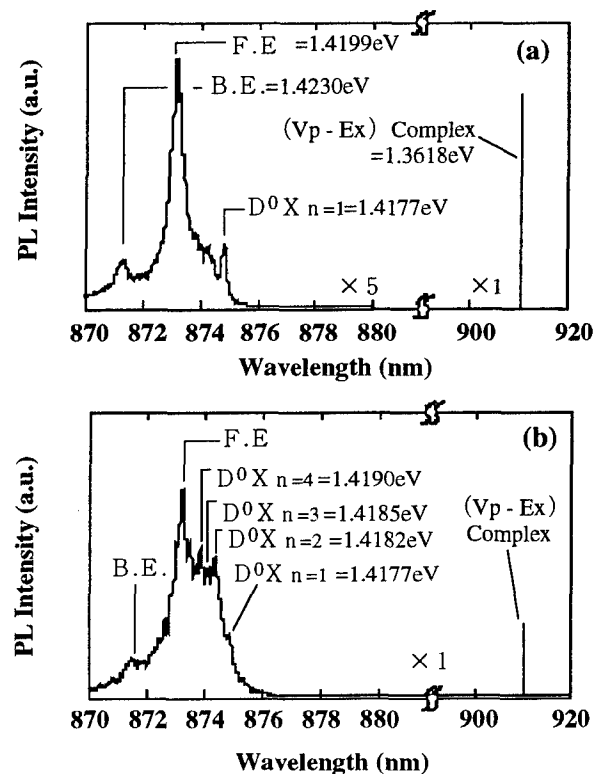

Fig. 5. Uniformity of electrical properties of SI InP after MWA process

Fig.6. Photoluminescence spectra of SI InP (a) after the first-step wafer annealing and (b) after the second-step wafer annealing

406

shallow donors. This mechanism is strongly supported by the latest finding of the change in PL spectra by wafer annealing [32]. Other possibilities are not yet excluded and further investigations are desired.

6. Conclusions

Continuous and steady work on SI InP by wafer annealing for this one decade clarified many facts dominating SI properties after wafer annealing and reproducible preparation of SI InP with extremely low Fe concentrations became possible. Since rapid developments of high frequency electronic devices and high speed photonic devices need high-quality SI InP, these investigations are now going to flower in substrate production for these device applications.

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Annealing Behavior of the Hydrogen-Related Defect in LEC Indium Phosphide

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In the quest for semi-insulating undoped InP material, we have investigated the role of hydrogen in reducing free electron concentrations by the process of high temperature annealing. Hydrogen has previously been shown to form the defect V_{In}-H_4 in InP, and it has been suggested that this defect acts a donor. In order to elucidate the effect of H on the electrical properties of InP, we have performed annealing experiments on both undoped and Fe doped crystals. Samples were annealed at 900 °C for 3 days with a phosphorus overpressure of 5 atmospheres. The samples were studied using infrared absorption spectroscopy, which can be used as a direct measure of the concentration of both the Fe impurities and V_{In}-H_4 defects, and Hall effect. In the undoped samples, annealing results in a reduction of the electron concentration accompanied by an increase in the 77 K mobility. Due to the observed increase in the mobility of the samples, it is apparent that this decrease is not due simply to a change in the concentration of compensating acceptors. In the Fe-doped samples, a decrease in the ratio $[Fe^{2+}]/[Fe^{3+}]$ is observed after annealing, again indicating a reduction in the number of donors in the sample. In all samples, the changes in the donor concentration upon annealing are accompanied by the complete disappearance of the LVM peak due to V_{In}-H_4. Taken together, these results confirm the role of hydrogen in the reduction of free carriers during the annealing of bulk InP material.

I) Introduction

Doping with iron is the standard method used to produce semi-insulating indium phosphide substrates. Iron is a deep acceptor which compensates the residual shallow donors in the material. The neutral state of the iron acceptor is Fe^{3+}, while it converts to the Fe^{2+} state when it compensates a donor. For crystal growth of high quality semi-insulating InP, there are reasons to control the iron concentration at as low a level as possible. First, iron diffusion from the substrate into the epitaxial layers affects device performance. Second, because of the small iron distribution coefficient ($\approx 10^{-3}$), the iron concentration near the tail of the crystal may exceed the solubility limit (10^{17} cm^{-3}). Many attempts have been made to find a substitute for iron, or to grow semi-insulating undoped InP. It has been reported that an alternate method of producing semi-insulating indium phosphide is to anneal undoped material at 900 °C for a period of two to three days [1,2]. While this results in a dramatic reduction in the free carrier concentration in the material, the cause of this decrease is not well understood. It was initially thought that some unknown deep level defect was responsible for compensating the residual shallow donors in this material. It is now apparent, however, that to be effective this annealing technique still requires a small amount of Fe to be present in the sample [3]. Regardless of the identity of the compensating species, it is clear that the free carrier concentration in the sample has decreased after annealing. We will show that this decrease is not simply due to a change in the number of compensating species, and propose that at least a partial explanation for this behavior is that the annealing process removes hydrogen from

the material. Hydrogen has been shown to form a complex with an In vacancy in which hydrogen atoms saturate all four dangling bonds, and it has been suggested that this defect acts as a donor [4]. Previous work has demonstrated that the local vibrational mode at 2316 cm^{-1} can be identified with the V_{In}-H_4 complex [5]. We have carried out annealing studies on both iron-doped and undoped LEC InP to determine the electrical nature of the V_{In}-H_4 complex by assessing whether the changes in the H concentration can be correlated with the change in the free carrier concentration in the material.

II) Experimental

The samples used in this study were grown at the Rome Laboratory by the magnetic liquid encapsulated Kyropoulos method. Samples were annealed in sealed silica ampoules at 900 °C for three days at a phosphorus overpressure of five atmospheres, and then cooled at a rate of 50 °C/hr. Since we were interested in the bulk properties of the material, a minimum of 50 microns of material was removed after the annealing to insure that any surface contamination did not affect our results. Infrared absorption measurements were performed in a Bomem DA-8 Fourier transform spectrometer at 10 K to measure the absorption due to the V_{In}-H_4 complex in all samples and the Fe^{2+} concentration in the Fe-doped samples. The Fe^{3+} concentration was measured using a Cary 2390 spectrometer according to the method described in [6]. The concentration of Fe^{3+} was found to be unchanged after the annealing.

III) Results and Discussion

In Figure 1 we see a typical result of the absorption spectrum of Fe^{2+} before and after annealing. The change in Fe concentration for two iron-doped samples was calculated using the calibration determined in [4] and the results are listed in Table 1. The annealing results in a decrease in the concentration of compensated Fe^{2+} in the iron-doped samples, thus implying a decrease in the number of donors in the sample. For both of the samples listed in Table 1, the change in the compensated donor concentration in the material was roughly 2×10^{15} cm^{-3}. In Table 1 we also list the absorbance in the H peak before annealing.
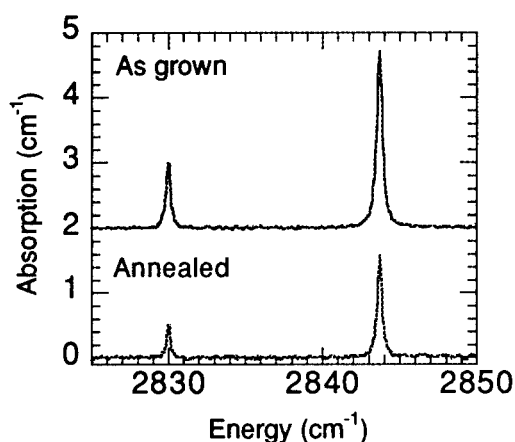
Fig. 1   Reduction in the concentration of Fe^{2+} after high temperature anneal as shown by the decrease in the strength of the Fe^{2+} intracenter absorption peaks. Spectra offset vertically for clarity.

Table 1. Effect of annealing on Fe-doped InP samples.

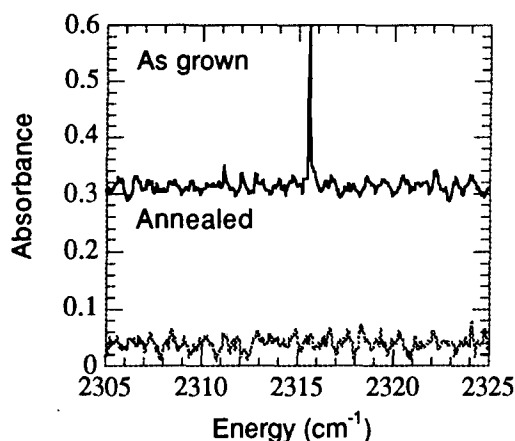| Sample	[Fe^{2+}] as grown (cm^{-3})	[Fe^{2+}] annealed (cm^{-3})	Δ[Fe^{2+}] (cm^{-3})	Integrated absorption of 2316 cm^{-1} H peak (cm^{-2})
4057	3.3×10^{15}	1.5×10^{15}	1.8×10^{15}	.089
4041	3.3×10^{15}	1.7×10^{15}	1.6×10^{15}	.097

Fig. 2 Disappearance of the local vibrational mode of the V_{In}-H_4 complex after high temperature anneal. Spectra offset vertically for clarity.

Since the LVM absorption peak completely disappears after the annealing, as we see in Figure 2, we relate this change in Fe^{2+} concentration to the change in absorption by the H donor complex absorbance, which was about 0.1 cm^{-2} in both samples. By averaging the data for these two samples, we can derive a calibration factor for the absorption by the V_{In}-H_4 defect, which is $[V_{In}$-$H_4] = 1.8 \times 10^{16}$ cm^{-1} x Absorbance (cm^{-2}). We note that the calibration factor we used is somewhat different than the calibration factor proposed by Alt, which would predict Fe^{2+} concentrations which are a factor of 2.8 larger [7]. Taking both of these calibrations into account, we therefore state that the multiplicative factor for measuring H defect concentrations by absorption should fall in the range 1.8-5×10^{16} cm^{-1}. This result is similar to a calibration carried out for the P-H bond

concentration in hydrogen passivated InP:Zn [8].

We also examined the change in the free carrier concentration in undoped samples of InP. The results of these measurements are given in Table 1. For both samples, we see a drop in the free carrier concentration accompanied by the disappearance of the H peak. To differentiate between the possibility that we were simply introducing new acceptors into the material, we compared the mobilities of the samples before and after annealing. If the drop in the free carrier concentration was merely due to the presence of additional compensating impurities, then we should observe a decrease in the mobility of the samples. However, we actually observe an increase in the mobility of the samples, which is consistent with the fact that we have simply decreased the number of donors in the sample. Again, since the LVM peak due to the V_{In}-H_4 complex has completely disappeared after annealing, this data is consistent with the explanation that the donors removed from the samples are due to the H defect.

We now consider whether the calibration suggested by the absorption data on the Fe-doped samples is consistent with the results of the change in free carrier concentration in the observed undoped samples. For sample 569, a change in concentration of $n=1.5 \times 10^{15}$ corresponds to a change in the [H] absorption peak of 0.034 cm^{-2}, while for sample 4066 the changes are $\Delta n = 2.3 \times 10^{15}$ and Δ(absorbance) = .048 cm^{-2}. Averaging these values gives a calibration of $[V_{In}$-$H_4] = 4.6 \times 10^{16}$ cm^{-1} x Absorbance (cm^{-1}). We see that this falls within the range found by studying the

Table 2. Effect of annealing on undoped InP samples.

Sample	n(77 K) as grown (cm⁻³)	μ (77K) as grown (cm²/Vs)	n(77 K) annealed (cm⁻³)	μ (77K) annealed (cm²/Vs)	Absorption of 2316 cm⁻¹ H peak (cm⁻²)
569	2.8×10^{15}	26500	1.3×10^{15}	39900	.034
4066	5.4×10^{15}	26500	3.1×10^{15}	30000	.048

change in Fe^{2+} absorption in the Fe-doped samples, thus confirming the donor nature of H in bulk InP.

IV) Conclusion

In conclusion, we have studied both Fe-doped, semi-insulating and undoped LEC grown bulk InP crystals to determine the electrical nature of the hydrogen defect. By comparing changes in absorption of the hydrogen defect with changes in the Fe^{2+} absorption in the Fe-doped crystals and changes in the free electron concentration in the undoped samples, we were able to simultaneously confirm the donor nature of the H defect and propose a calibration factor for determining its concentration. These results confirm the important role played by hydrogen in determining the properties of bulk InP and its conversion to semi-insulating material.

Acknowledgments

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CARRIER TRAPPING DUE TO Fe^{3+}/Fe^{2+} IN InP

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Introduction

Time-resolved photoluminescence studies were performed on epitaxially grown InP either doped with iron or codoped with iron and sulphur to gain information on carrier trapping characteristics of Fe^{3+}/Fe^{2+}. The carrier trapping time was found to be dependent on iron concentration in InP:Fe and both, iron and sulphur concentrations in InP:Fe,S. From the measured trapping times in both InP:Fe and InP:Fe,S the electron and hole capture cross sections of the Fe deep levels are determined as $\sigma_e = 1\times10^{-15}$ cm² and $\sigma_h = 6\times10^{-15}$ cm², respectively. From the derived capture cross sections and the measured trapping times, the concentration of the different iron species is calculated in both, InP:Fe and InP:Fe,S. It reveals that the active iron concentration (Fe^{3+}) exceeds 1×10^{18} cm⁻³ for the highest total iron doping concentrations in InP:Fe.

I. Background

Iron in InP is a deep acceptor for electrons, and hence imparts the semi-insulating (SI) properties to InP. The origin of the carrier trapping mechanism is the neutral iron state, Fe^{3+}, which after trapping an electron becomes ionized to Fe^{2+}. It can regain its Fe^{3+} state by trapping a hole, thus the Fe^{3+}/Fe^{2+} level acts as a recombination centres for carriers. The study of the lifetime of photogenerated carriers in InP provides information about the iron impurities, since the trapping mechanism involved causes a reduction in the carrier lifetime. So far, carrier trapping due to Fe^{3+}/Fe^{2+} has been mainly studied in bulk InP. Regardless of a extensive use of epitaxial semi-insulating InP:Fe for current blocking, integration and reduction of parasitics, certain basic parameters such as the capture cross sections, are not well known. According to the literature, the capture cross section for electrons ranges from 1×10^{-15} to 4×10^{-14} cm² for the bulk material (1-5). The capture cross section for holes is even more uncertain and ranges from 1×10^{-16} to $\sim3\times10^{-14}$ cm², also determined for the bulk material (4-6).

In the present work, the trapping characteristics in InP:Fe and InP:Fe,S were studied to obtain the electron and hole capture cross sections of the Fe deep levels, in addition, the concentration of the different iron species involved was determined. To this end we used a contact-less time-resolved photoluminescence (PL) technique with a capability to measure very short trapping times. It is a most direct method to study the carrier trapping since the decay of the luminescence measured at the band gap energy is determined by the carrier transfer from the extended band states to the localized states in the trapping centers. This method alone cannot distinguish between the capture of electrons from that of holes. But, by a proper choice of the studied materials we show that the capture cross section of both, electrons and holes, can be determined.

II. Experimental

Two types of samples were considered in this investigation: I) InP:Fe with different iron concentrations and II) InP:Fe,S with a constant iron concentration and varying sulphur concentration. Introducing sulphur into InP:Fe changes the $[Fe^{3+}]/[Fe^{2+}]$ ratio since sulphur, being a shallow donor, ionizes Fe^{3+} to Fe^{2+}, which affects the carrier trapping process. Both types of samples were grown on (100) n-doped InP:S substrates by hydride vapour phase epitaxy (HVPE) at 685°C under 1 atm pressure. The layer thickness was 2 μm. The dopant concentrations were measured by secondary ion mass spectroscopy (SIMS). The Fe concentrations in type I samples were 2.5×10^{16}, 6×10^{16}, 1.5×10^{17}, 3×10^{17}, 1×10^{18}, 2×10^{18}, 5×10^{18} and 1×10^{19} cm⁻³. In type II samples, the Fe concentration was 2×10^{18} in all the samples and the sulphur concentrations were 7×10^{16}, 2×10^{17}, 5×10^{17}, 9×10^{17} and 3×10^{18} cm⁻³. It should be noted that at high Fe concentrations FeP precipitation is likely (7), and hence the total Fe concentration will not correspond to that of the Fe^{3+}/Fe^{2+} centres as at low Fe concentrations.

The PL transients were measured using a self-mode-locking Ti:sapphire laser with a central wavelength of 800 nm, a pulse duration of 100 fs and a repetition frequency of 96 MHz for excitation. For signal detection, an upconversion technique, providing a temporal resolution of 150 fs, was used. The excitation pulse was focused on a spot of 60 μm

diameter with average intensities of 10 to 80 mW. The probing depth of the PL into the layer calculated from the absorption coefficient is ~0.3 μm. All PL transients were measured at room temperature at the emission energy of 1.35 eV corresponding to the band gap transitions in InP.

To investigate the semi-insulating properties, a current-voltage (I-V) analysis were performed on the samples to ascertain the resistivity.

III. Derivation of the capture cross sections

The measured PL transients for the InP:Fe samples for various iron concentrations (type I) are shown in Fig. 1. The PL decay, which is of a single exponential type, describes how fast the photoexcited carriers disappear from the conduction and valence bands and can be used to determine the carrier trapping times. The inset in Fig.1 shows the PL decay time (trapping time) dependence on the total iron concentration. The decay time decreases from 530 down to 8.3 ps when the iron concentration is increased from 2.5×10^{16} to 1×10^{19} cm^{-3}. The decay time exhibits almost a linear dependence on the iron concentration up to a certain limit, namely, [Fe] ~ 2×10^{18} cm^{-3}, thereafter a tendency for saturation of the decay time is observed. The decrease of the decay time for increasing total iron concentration implies that the concentration of traps also increases.

It is imperative to quantify the contributions from electron and hole trapping due to Fe^{3+} and Fe^{2+}, respectively, since the PL transients describe the trapping of both electrons and holes. The concentration of Fe^{2+} is solely due to the ionization of Fe^{3+}, caused by the residual shallow donors, which remains constant at ~2×10^{15} cm^{-3} in all the InP:Fe samples. Thus, the concentration of Fe^{2+} cannot exceed 2×10^{15} cm^{-3} for different Fe doping concentrations.

In a highly SI material, $[Fe^{2+}] \ll [Fe^{3+}]$, according to previous theoretical and experimental investigations (8), which holds in our case as well. Thus, in the InP:Fe samples the decrease of the decay time for increasing iron concentration can only be due to an increased concentration of the Fe^{3+} trapping centers. It should be noted that intrinsic defects can also influence the decay time, however, these defects are the same in all samples and their contribution to the decay time is probably small compared to that from the Fe deep levels, since we observe a clear dependence of the PL decay time on Fe concentration.

The relation between the decay time and the trap concentration is described by

$$\frac{1}{\tau} = v_e \sigma_e \left[Fe^{3+} \right] + v_h \sigma_h \left[Fe^{2+} \right], \qquad (1)$$

where the terms τ, v and σ are the decay time (trapping time), thermal velocity and capture cross section, respectively, and their subscripts e and h denote their association to electrons and holes. For low total iron concentrations ($\leq 1 \times 10^{17}$ cm^{-3}) the precipitates can be assumed to be absent (7). Thus, the total iron concentration is described by [Fe] = [Fe^{3+}] + [Fe^{2+}], which substituted in Eq. (1) yields

$$\frac{1}{\tau} = v_e \sigma_e \left[Fe^{3+} \right] + \left(v_h \sigma_h - v_e \sigma_e \right) \left[Fe^{2+} \right], \qquad (2)$$

where the latter term is constant for the InP:Fe samples. The difference of the reciprocal decay time in Eq. (2) of the two samples containing the lowest Fe concentrations gives the electron capture cross section since $v_e = 3.85 \times 10^7$ cm/s. For [Fe] = 2.5×10^{16} and 6×10^{16} cm^{-3} with the corresponding decay times of 532 and 260 ps, respectively, one obtains $\sigma_e = 1 \times 10^{-15}$ cm^2.

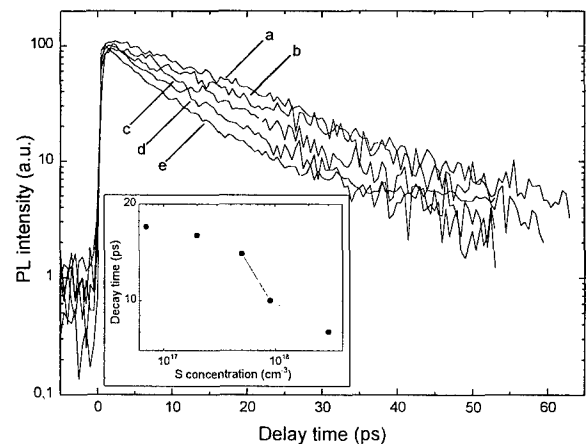**Fig. 1.** Photoluminescence transients for InP:Fe samples (type I) for various Fe concentrations (in cm^{-3}): a) 2.5×10^{16}, b) 6×10^{16}, c) 1.5×10^{17}, d) 3×10^{17}, e) 1×10^{18}, f) 2×10^{18}, g) 5×10^{18}, h) 1×10^{19}. The inset shows the decay time dependence on the total Fe concentration in the InP:Fe samples, derived from the transients.

Fig. 2. Photoluminescence transients for InP:Fe,S samples for various S concentrations (in cm^{-3}): a) 7×10^{16}, b) 2×10^{17}, c) 5×10^{17}, d) 9×10^{17}, e) 3×10^{18}. The Fe concentration was constant in all the samples at 2×10^{18} cm^{-3}. The inset shows the decay time dependence on the total S concentration in InP:Fe,S samples, derived from the transients.

413

Compared to the literature, Look extracted $\sigma_e = 1\times10^{-15}$ cm² by fitting a model to photoconductivity measurements (3). Valley et al. obtained 1×10^{-14} cm² from measurements of photorefraction (4). From DLTS, Bremond et al. (1) and Tapster et al. (2) obtained 3.5×10^{-14} and 4×10^{-14} cm², respectively. Asada et al. used $\sigma_e = 3\times10^{-15}$ cm² also derived from DLTS, in their modelling work (5).

Fig. 2 presents the PL transients of the InP:Fe,S samples. The transients are single exponential, just like for the InP:Fe samples. The decay time decreases from 17 down to 8 ps when the S concentration is increased from 7×10^{16} to 3×10^{18} cm⁻³ as shown in the inset of Fig. 2. This behaviour can only be due to the effect of S on the Fe deep centers, since S itself does not reduce the carrier lifetime (the PL decay time in InP:S with [S] = 3×10^{18} cm⁻³ was over 600 ps), and the iron content is constant in all the InP:Fe,S samples. Thus, the change in decay time is mainly due to the change of Fe^{2+} and Fe^{3+} concentrations, since sulphur ionizes Fe^{3+} to Fe^{2+}. Hence, unlike in InP:Fe samples, where the electron capture is the main event, in InP:Fe,S both electrons and holes are involved in the capture process, which makes it possible to extract the hole capture cross section of Fe^{2+}.

If it is assumed that all the incorporated S is active, the sum of $[Fe^{2+}]$ and $[Fe^{3+}]$ should remain constant. Besides, for low S concentrations, the density of FeP precipitates (if any) is assumed to remain constant between the samples with different S concentration. Thus, from Eq. (1) the difference between the reciprocal decay time of two samples, say, sample 1 and 2, can be written as

$$\frac{1}{\tau_2} - \frac{1}{\tau_1} = v_e\sigma_e\left([Fe^{3+}]_2 - [Fe^{3+}]_1\right) + v_h\sigma_h\left([Fe^{2+}]_2 - [Fe^{2+}]_1\right), \quad (3)$$

where the subscripts 1 and 2 indicate samples 1 and 2, respectively. Here $[S]_2 > [S]_1$. The law of mass conservation suggests that

$$[Fe^{3+}]_2 - [Fe^{3+}]_1 = [S]_1 - [S]_2 \quad (4)$$

$$[Fe^{2+}]_2 - [Fe^{2+}]_1 = [S]_2 - [S]_1, \quad (5)$$

since S is responsible for ionizing Fe^{3+} to Fe^{2+}. Putting $\Delta[S] = [S]_2 - [S]_1$ and substituting (4) and (5) into Eq. (3) gives

$$\sigma_h = \left[\left(\frac{1}{\tau_2} - \frac{1}{\tau_1}\right) / \Delta[S] + v_e\sigma_e\right] / v_h. \quad (6)$$

By using v_e, v_h (= 1.33×10^7 cm/s) and $\sigma_e = 1\times10^{-15}$ cm² in Eq. (6) for the InP:Fe,S samples containing the lowest S concentrations, 7×10^{16} and 2×10^{17} cm⁻³, we obtain $\sigma_h = 6\times10^{-15}$ cm². The same value is obtained by using the next two InP:Fe,S samples. As far as the σ_h values available in the literature are concerned, the only experimental value of σ_h is that of Valley et al., which is 3×10^{-16} cm² obtained from the measurements of photorefraction (4). In their modelling work, Asada et al. (5) used a value of $\sigma_h = 1\times10^{-16}$ cm². From modelling, Iverson et al. (6) obtained $\sigma_h \sim 3\times10^{-14}$ cm².

Contrary to an earlier assumption by Asada et al. (5) two experimental facts support our result that $\sigma_h > \sigma_e$, very clearly. First, the second term on the right hand side of Eq. (2) has a positive value in the InP:Fe samples, which implies that $\sigma_h/\sigma_e > v_e/v_h \approx 2.8$, which in fact is the case, our $\sigma_h/\sigma_e \approx 6$. Secondly, the PL decay time in the InP:Fe samples does not change with increasing excitation intensity. This can only occur if the photoionized Fe^{2+} state rapidly returns to the neutral Fe^{3+} state by capturing a hole.

IV. Quantifying various Fe species

The concentration of Fe^{3+} in the InP:Fe samples which may contain FeP precipitates ([Fe] > 1×10^{17} cm⁻³) can be derived by using the electron capture cross section derived from samples devoid of precipitates. For these samples the total Fe concentration is described by [Fe] $\approx [Fe^{3+}] + [Fe^{2+}] + [Fe]_{FeP}$, thus, the concentration of Fe_{FeP} (Fe atoms in the FeP precipitates) can also be derived, since the total Fe concentration is known from SIMS, and $[Fe^{2+}]$ is equal to the residual donor concentration, as argued before. Fig. 3 presents the calculated concentrations of Fe^{3+} and Fe_{FeP} in the InP:Fe samples for various total Fe concentrations, where also the resistivity data are included. The $[Fe^{3+}]$ increases with [Fe] until a tendency for saturation is reached at [Fe] $\approx 2\times10^{18}$ cm⁻³, due to formation of FeP precipitates at high Fe concentrations. Up to the point of intersection of the two curves, $[Fe^{3+}] > [Fe]_{FeP}$, thereafter $[Fe]_{FeP}$ being dominant, while $[Fe^{3+}]$ remains almost constant. This behaviour, a constant increase of $[Fe^{3+}]$ followed by a tendency for saturation for increasing [Fe], is in agreement with the resistivity measurements, which show an increasing resistivity with increasing Fe concentration, and exhibits a maximum resistivity for [Fe]$\approx2\times10^{18}$ cm⁻³, see Fig. 3.
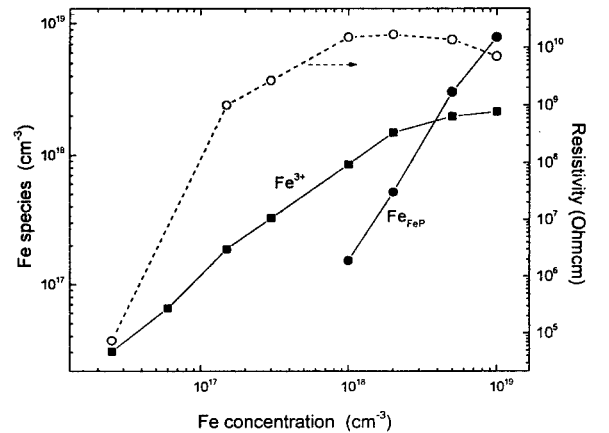

Fig. 3. The Fe^{3+} and Fe_{FeP} dependence on the total Fe concentration in InP:Fe (type I) samples. Also included, the resistivity dependence on the total Fe concentration.

It should also be mentioned that for low Fe concentrations the calculated Fe^{3+} concentrations are slightly higher than those of the total Fe, due to an uncertainty in the measured total Fe concentrations by SIMS.

For InP:Fe,S (type II samples) the different iron species, i.e. Fe^{3+}, Fe^{2+} and Fe_{FeP}, can be quantified in a similar way as with the InP:Fe (type I) samples. The concentration of Fe^{2+} is equal to that of S, if all the S donors ionize the neutral Fe^{3+}. The concentration of Fe^{3+} can be derived by exploiting Eq. (1). Two cases appear, (i) for samples with [S] < [Fe], $[Fe^{2+}]$ = [S] and (ii) for samples with [S] > [Fe], $[Fe^{3+}] \approx 0$. The first case yields $[Fe^{3+}]$ and the second $[Fe^{2+}]$. In Fig. 4 the various calculated Fe species and the resistivity are plotted as a function of the S concentration. From Fig. 4 the following can be inferred: (i) The substitutional Fe concentration $[Fe^{3+}]$ + $[Fe^{2+}]$ and $[Fe]_{FeP}$ remain constant up to [S] $\approx 5\times10^{17}$ cm^{-3}. At this point $[Fe^{3+}]$ + $[Fe^{2+}]$ starts to increase, but $[Fe]_{FeP}$ decreases. This fact is in agreement with the SIMS investigations on the same samples which show that the accumulation of Fe near the interface is suppressed at [S] $\approx$ 5×10^{17} cm^{-3} (9). (ii) with increasing S concentration $[Fe^{3+}]$ decreases and Fe^{2+} increases until at [S] $\approx 5\times10^{17}$ cm^{-3}, $[Fe^{2+}]$ outweighs $[Fe^{3+}]$. This suggests that the material will be less semi-insulating as the amount of S is increased, and at [S] $\approx$ 5×10^{17} cm^{-3} the SI properties are completely destroyed, since $[Fe^{2+}]$ > $[Fe^{3+}]$. This fact is confirmed by the I-V characteristics of InP:Fe,S (9).

Finally, by an additional experiment, we show that the influence of the FeP precipitates on our results is negligible. First, we have measured the PL decay for the heavily Fe-doped InP:Fe samples at different depths of the epitaxial layer. This was achieved by chemically etching the samples between the subsequent PL measurements. The SIMS measurements show that the total Fe concentration increases towards the interface at which an accumulation of the precipitates is likely (7). The PL trapping times are identical for carriers throughout the epitaxial layer suggesting that even if the precipitates trap the carriers, they do it with a much lower efficiency than the Fe^{3+}/Fe^{2+} levels. In addition, investigations of InP with metallic CuIn precipitates in InP shows much longer PL decay times compared to the present measurements (10).

V. Conclusions

In conclusion, carrier trapping characteristics due to the Fe^{3+}/Fe^{2+} level in epitaxial InP have been studied by time-resolved photoluminescence for the first time. The electron and hole capture cross sections have been experimentally determined as σ_e = 1×10^{-15} cm^2 and σ_h = 6×10^{-15} cm^2, respectively. The concentration of the different Fe species in both InP:Fe and InP:Fe,S have been quantified.

Fig. 4. The Fe^{3+}, Fe^{2+}, Fe_{FeP} and (Fe^{3+} + Fe^{2+}) dependence on the S concentration in the InP:Fe,S (type II) samples. Also included is the resistivity dependence on the total S concentration.

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CRYSTAL GROWTH OF BULK InP FROM MAGNETICALLY STABILIZED MELTS WITH A CUSPED FIELD

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Introduction

Crystal growth of bulk InP using a cusped magnetic field has been investigated. A vertical arrangement of two Helmholz coils with opposite polarity provides the configuration for a cusped field. A comparison between growth of InP under an aligned axial field and a cusped field shows that turbulent melt flow is damped by the former but not by the latter. By use of IR transmission images, it was determined that each magnetic configuration has a different effect on interface shape, facet formation, and striation frequency. Although the cusped field produced a crystal with a flatter melt-solid interface, overall process control was enhanced only by growth from an axial magnetic field.

I. Background

Magnetic field configuration is an important aspect of process control in the growth of semiconductor crystals from the melt. A vertical axial field has been reported[1] in Czochralski growth of InP, Si, and GaAs, with the principal aim of damping buoyancy driven turbulent flow. The melt becomes more stable so that better doping uniformity is achieved, both on short range striae and long range seed to tail variation. Transverse magnetic fields have been used for Czochralski growth of silicon to reduce the oxygen incorporation from the silica crucible wall into the silicon melt. The transverse field allows horizontal transport of oxygen along the melt surface parallel to the field, but inhibits flow at the crucible wall, reducing oxygen incorporation. Use of a cusped field has been reported for silicon crystal growth[2] but not for other semiconductors. A cusped field, with vertical opposed solenoids above and below the crystal-melt interface, allows radial fluid transport along the free surface and also inhibits vertical flow along the crucible wall[3]. Unlike the transverse magnetic field, the cusped field is axisymmetric.

Growth of InP from an axial magnetic field has advantages; melt stability contributes to reduced incidence of twinning and dopant uniformity improves[4]. On the other hand, the radial temperature gradient is increased by an axial magnetic field because convective heat transfer in the melt is reduced. The resulting convex crystal-melt interface contributes to large hoop stresses during crystal growth which, in turn, cause dislocation generation and propagation. If a cusped magnetic field is employed, the radial thermal gradients are predicted to be flatter, since the non-uniform field will not affect radial fluid flow near the surface[5]. Flattening the melt isotherm should reduce the dislocation density of InP crystals.

The purpose of this work is to evaluate InP bulk crystal growth in a cusped magnetic field, and to determine if there are advantages in terms of process control which could flatten the interface shape and reduce thermoelastic strain.

II. Experimental

Materials for these experiments are obtained from commercial sources in 6N or 7N purity. Red phosphorus (260g), boric oxide encapsulant (160g), and indium (800g) are loaded into a 4-inch diameter silica crucible in a 112mm diameter graphite susceptor, heated by a 160mm diameter 10 turn 1/4" copper coil, powered by an 50KW RF generator operating at 450kHz. Tin (99.99% purity) is used to dope the crystal to $2 \times 10^{18} cm^{-3}$. Silica fixtures are GE 214 grade. The furnace is evacuated to less than 100 millitorr before it is filled with nitrogen to 600 psig. Two torroidal magnet coils provide an axial magnetic field up to 4000 gauss at the center of the hot zone (see Figure 1). A silica injector ampoule loaded with phosphorus is lowered until the 75 mm transfer tube 16 mm· in diameter extends into the encapsulated liquid Indium to within 1 to 5 mm of the crucible bottom. Injector heating is controlled by the depth of immersion in the melt. The injector is partially insulated on the top and sides to retain heat and diminish gradients within the ampoule. The injector temperature rises at 5° to 15°C per minute until it reaches 600°C, at which point the synthesis of the InP melt is essentially completed.
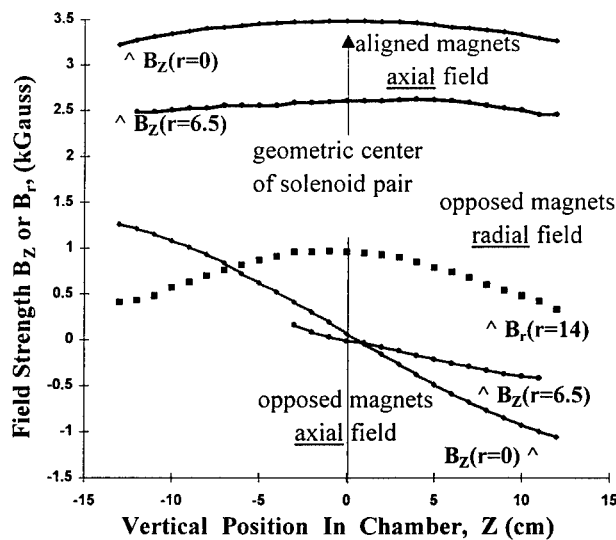
Fig. 1. Measured Magnetic Field Strength vs. Position

Thermal fluctuations in the InP melt are measured with and without an applied magnetic field to determine the effect of the magnet configuration on turbulent flows. Temperature measurements are made using an Accufiber optical thermometer immersed in the melt. A 1 kg charge of InP is melted with standard a 160 g B_2O_3 encapsulant layer. Both type K thermocouples and a sapphire optical thermometer (Accufiber model M100-C) are suspended in the melt. The sensors are enclosed in tight fitting silica tubes, and held at constant position to record transient melt behavior when the magnetic field is changed.
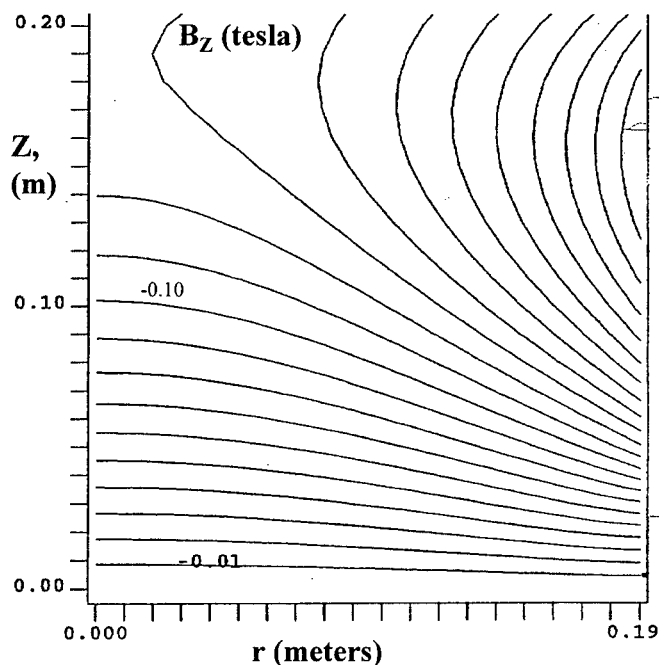
Fig. 2a Calculated axial isofield lines for cusped field

Evaluations of the interface shape and the microstructure of striations are performed by inspection of axial slices from the crystal center. These slices are lapped and polished on both sides for IR transmission microscopy at 1μm. The interface shape is detected with an IR camera with a narrow band-pass filter at 3μm wavelength.

The axial and radial magnetic field strengths are measured at various points throughout the crystal growth chamber with a Gauss meter. Fig. 2 a&b show constant field lines calculated for both the axially aligned and cusped field configurations for a total magnet power of 30KW. The measured values are in close agreement with these calculations.
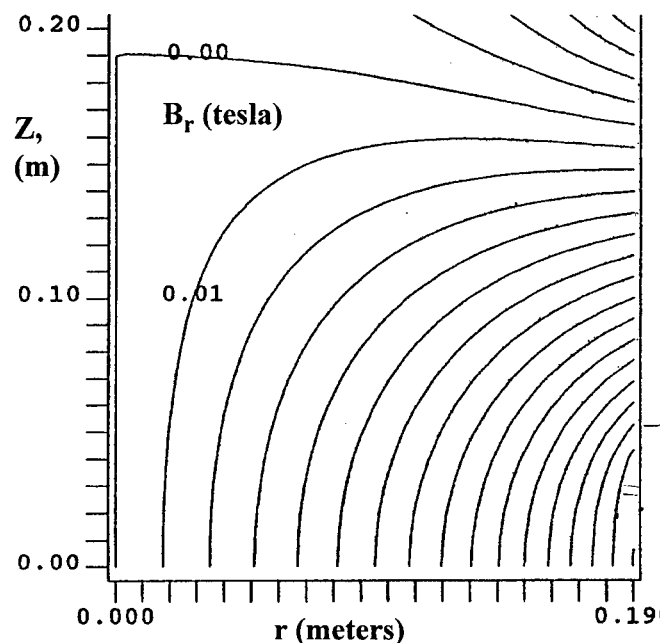
Fig. 2b Calculated radial isofield lines for cusped field

III. Results and Discussion

Stabilization of InP melts with two aligned magnets is a practical technique for growth of twin-free InP crystals. An applied magnetic field of 2kG is sufficient to suppress random oscillatory flow, which causes unstable growth at the seed-melt interface under normal conditions. The uniform axial magnetic field prevents rapid regrowth and melt-back near the seed junction, where the twinning probability is high. Because of this stability, a wide growth angle from the seed can be sustained, and so an MLEK crystal can be shaped with a flat top. The increased melt stability and perpendicular growth angle also reduce facet formation near the (111) planes. Such (111) edge facets are a characteristic feature of typical InP cones grown without a magnetic field, but they are not observed on the periphery of MLEK crystals. Note the regular striations and absence of

417

facet formation in Fig. 3, an IR transmission micrograph of the MLEK top section.

For InP growth in a cusped field, the magnetic stabilization effect is much weaker. Since the two magnets are opposed, much of the field strength is canceled, and in fact the field goes to zero at the center. Although the radial component of the magnetic field within the crucible is about 1/4 kG, this is not strong enough for convective damping. Without a strong applied magnetic field, random oscillatory flow exists in the melt, and flat top growth is not possible. Attempts to grow out perpendicular to the seed were frustrated by twin formation or dendritic growth. In order to obtain a single crystal under these conditions, the crystal must be pulled as in LEC growth, i.e. with a 60-75° cone angle from the vertical seed axis. A few crystals were

successfully grown in this fashion, but with occasional twin formation. The appearance of facets forming on (111) planes at the crystal periphery was observed in IR transmission micrographs, as seen in Fig. 4.

Temperature fluctuations recorded with the sapphire optical thermometer and two thermocouples revealed the effect of magnetic field configuration on turbulent flow. For these measurements, the sensors were placed near the center of the melt at 2mm and 12mm from the crucible bottom (total InP depth approximately 31mm), with zero crucible rotation. After the temperature reached steady state the magnet power was turned on and remained at 30kW. Figures 4 and 5 show the transient thermal behavior for both the aligned and cusped fields. In Fig. 5 (aligned) the temperature drops rapidly to a 20°C lower level and remains steady without fluctuations. Fig. 6 (cusped) shows almost no effect on turbulence at the moment when the magnet is turned on. The fluctuations continue at the same frequency and amplitude as before, but with a slight shift in average temperature.

Fig. 3 IR micrograph at 1um of MLEK grown in axial field.
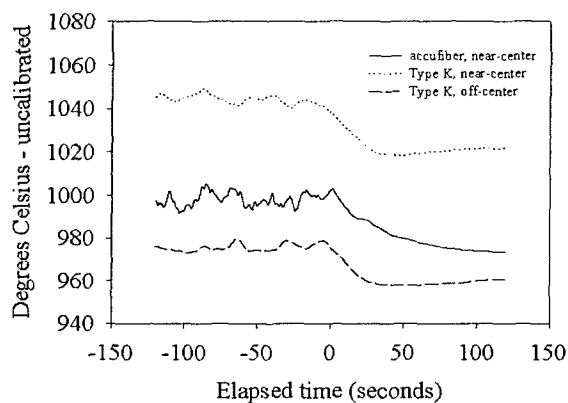
Fig. 5 off to axial magnet transition at 12mm from bottom

Fig. 4 IR micrograph at 1um of MLEK grown in radial field.
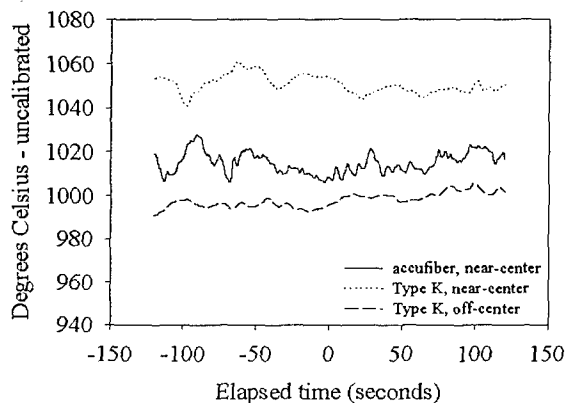
Fig. 6 off to cusped magnet transition at 12mm from bottom

Examination of the growth striations by IR transmission microscopy revealed some interesting differences between the axial and cusped magnetic fields. For crystals grown under axial field conditions, regular striations were observed which appeared to follow the rotational frequency. Dividing the growth rate by the rotation rate gives V/R = 50μm, as the calculated growth length per period. The observed striations showed an approximate spacing corresponding to 50 μm. No facets were observed at the top of the crystal. On the other hand, the crystal grown in a cusped field exhibited a random striation pattern, with spacings as small as 30μm and as large as 150μm. A large variation from center to edge was also observed indicating that the interface shape was changing on the microscale. Edge facets were observed near the top surface of the crystal on (111) planes, coinciding with the plane of twin formation.

The interface shape was examined with infrared transmission images taken with the IR camera for the two different magnetic configurations. For axial field growth the interface was convex at the seed end (radius of curvature r = 7 cm.), becoming flatter near the tail. As the melt height is reduced, heat transfer becomes dominated by conduction from the flat bottom of the crucible, flattening the radial temperature gradient. For crystals grown with a cusped field, as shown in Fig. 7, the interface shape is sigmoidal, i.e. convex with deflected edges. This shape is very similar to the shape observed in non-magnetic InP bulk growth. The convex portion of the interface has a radius of curvature r = 9 cm.
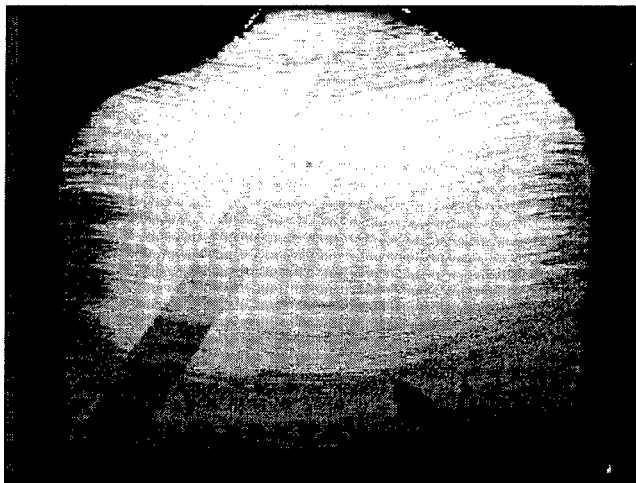
Fig. 7 IR camera image at 3um for growth in cusped field

IV. Summary

Crystal growth under two different magnetic field configurations was investigated. Axial field growth enhances melt stability, but increases the radial thermal gradient. This configuration contributes to crystal growth control and reduces twin formation. The axial field strength is strongest in the center of the growth chamber, where the crucible is located. On the other hand, for a cusped configuration, the radial component of the field is stronger than the axial component in the mid-section. However, because of the large inside diameter of the magnet coils required for our thick wall high-pressure growth chamber, the cusped field is too weak to stabilize the melt. Crystals grown in the cusp configuration resemble those grown without any applied field. The melt-solid interface shape is convex for both configurations, but slightly flatter for growth in a cusped field. Given the small effect of this field configuration, there was no observable improvement in crystal growth resulting from the application of a cusped magnetic field.

V. Acknowledgments

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IMPROVEMENT OF THE SURFACE QUALITY OF POLISHED InP TuC5 WAFERS

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Introduction

Indium phosphide wafers are nowadays more and more used as epi ready wafers, as customers do not want to do any pre-treatment before introducing the wafers into their reactors. In the case of microelectronics applications and especially for MOVPE grown structures, the electrical conduction at the interface between the semi insulating substrate and the epitaxial layer is a crucial issue and must be eliminated in order to control the condution in the Field Effect Transistor canal [1]. It has been demonstrated that silicon contamination is the origin of the interface conduction [2]. This contamination present on the surface of the substrate is very low ($10^{11} \sim 10^{12}$ at/cm^2) and is below the detection limit of standard surface analysis measurement such as XPS. We demonstrate that TOF-SIMS is a very powerful technique to characterise the surface and investigate any contamination at the interface such as the low silicon content. TOF-SIMS analysis has been performed after various chemical preparation at InPact and will be presented. It allows us to detect all the elements and molecules present on the surface, even in very low concentration (10^{10} at/cm^2). Thanks to these results we are now able to produce wafers with very clean surface in a reproducible way. Futhermore the TOF-SIMS results explain the conductive buffer layer obtained by MOCVD epitaxy.

I. Experimental.

Two kinds of experiments have been carried out in order to characterize this silicon on the surface of the wafers.

First one : An epitaxial layer was grown by MOCVD. Growth was carried out in an AIX - 200X horizontal reactor with gas foil rotation (AIXTRON) at 640°C, 20 mbar reactor pressure and 0.9 m/s gas velocity. The standard source compounds TMIn and PH3 were carrried to the reactor with purified (SAES Getters) nitrogen as the carried gas.The growth rate was 2 µm/h. Before growth, substrats were deoxidized in PH3 for 6 minutes at growth temperature. A layer of 2 µm of InP was grown on each wafer.This epilayer was mesured by Hall effect at room temperature and at liquid Nitrogen temperature.

Second one : TOF-SIMS. This newly developed SIMS kind of apparatus is very powerful to analyse the top-surface of samples. The composition of the first monolayer can be determined with high accuracy and very quickly (about one minute). The TOF-SIMS usually removes only a fraction of the first monolayer.

These two ways of characterization have been performed on wafers with different final treatments.

1) We analysed wafers prepared with the old InPact treatment (0InP). These wafers, after mechanical-chemical polishing have been surface prepared with some etching, cleaning and U.V. oxidization-process.

2) Then some wafers, were processed for comparision with the usual H2SO4 recipe before rinsing at room temperature. The etch rate is 75 Å.mn^{-1}. This is applied for 5 minutes before rinsing.

3) Other wafers went through the standard 5 : 1 : 1 (H2SO4 : H2O2 : H2O) etchant. This gives an etch rate of 125 Å.mn^{-1} at room temperature and is applied for 5 minutes before rinsing.

4) The influence at the U.V. oxidization on these 3 kinds of wafers (0InP, H2SO4, 5:1:1) was studied.

5) Wafers from other suppliers were also analysed (A, B, C, D). The carrier concentration can be specified either considering the volume (n in cm^{-3}) or the surface, as the sheet carrier concentration (Ns in cm^{-2}). Ns = 2 x 10^{-4}.

6) Taking into account results of the TOF-SIMS technique, InPact has developped a new process of etching /cleaning/ and packaging the InP substrate (NInP as the code name).

II. Results

A. Epitaxial layers

A 2 μm thick InP, not intentionally doped, layer is grown on the substrate. As the wafer is used as epi ready, no treatment is done before introducing the wafer into the reactor.

Table I : Hall effect results on different epi layers

PROCESS		n (RT) 10^{15} cm^{-3}	μ(RT) cm^2/VS	n(77K) 10^{15} cm^{-3}	μ (RT) cm^2/VS	Ns 10^{11} cm^{-2}
OInP(U.V.)		10.8	1 940	2.3	22 900	21.6
OInP(U.V.)		11.7	1 730	2.4	16 090	13.4
OInP(U.V.)		8.8	2 000	1.6	21 800	17.6
OInP(U.V.)		8.5	2 000	1.6	20 800	17
H2SO4		2.0	2 680	0.5	47 220	4.0
H2SO4		1.9	2 790	0.4	47 730	3.8
5:1:1		1.4	2 630	0.4	58 550	2.8
5:1:1		2.1	1 860	0.5	37 250	4.2
5:1:1		1.9	2 770	0.4	65 370	3.8
5:1:1		2.5	2 640	0.5	60 890	5
Supplier	A	1.4	3 170	0.4	47 240	2.8
	A	1.1	3 600	0.4	62 000	2.2
	A	1.8	3 030	0.5	51 080	3.6
Supplier	B	3.9	2 800	0.9	33 000	7.8
	B	5.7	2 400	1.2	26 600	11.4
Supplier	C	2.3	3 200	0.6	65 400	4.6

Table I shows that OInP wafers could not fit the new microelectronic requirements. The conduction layer at the interface is above 10^{12} cm^{-2}. Using H2SO4 or 5 : 1 : 1 etching, the conduction layer is reduced to Ns = 2 ~ 5 x 10^{11} cm^{-2} which better fits the specifications. A first conclusion is that the chemical treatment and etching play a key role. Furthermore, we check the influence of the U.V. oxidization. This step was usual on OInP wafers.

Table II: Results on epi layers without and with U.V. oxidization

PROCESS	n (RT) 10^{15} cm^{-3}	μ(RT) cm^2/VS	n(77K) 10^{15} cm^{-3}	μ (RT) cm^2/VS	Ns 10^{11} cm^{-2}
InPact process (intermediate) without U.V.	4.1	2 200	0.7	45 600	8.2
InPact process (intermediate) with U.V.	6.2	1 540	1.1	30 740	12.4
H2SO4 without U.V.	2.0	2 680	0.5	47 220	4
H2SO4 without U.V.	2.9	2 420	0.6	37 230	5.8
5:1:1 without U.V.	1.4	2 630	0.4	58 550	2.8
5:1:1 without U.V.	2.2	2 600	-	-	4.4

Table II shows clearly that the U.V. treatment increases by at least 50 % the silicon concentration. A second conclusion is that, in addition to the chemical treatment, the air, too, generates silicon. From these results, we have perfected a new process for chemical treatment, cleaning and packaging. No U.V. oxidization is performed in this new process.

Table III : Results with NInP wafers

PROCESS	n (RT) 10^{15} cm^{-3}	μ(RT) cm^2/VS	n(77K) 10^{15} cm^{-3}	μ (RT) cm^2/VS	Ns 10^{11} cm^{-2}
NInP	2.8	2 520	0.6	54 430	5.6
NInP	1.2	2 600	0.2	82 000	2.4
NInP	0.9	2 890	0.4	61 610	1.8

Table III gives the results obtained with this NInP (New InPact Process).

Ns values as low as 2 x 10^{11} cm^{-2} can be reached as well as very high mobility at 80 000 cm^2/V.s. at nitrogen temperature. The state of the art requirements from the microelectronics world are now met. Also please note that an extra etching, depeveloped by Hardtdegen et al (4) just before loading the reactor gives very impressive results with a mobility of 170 000 cm^2/V.s. and Ns = 2.6 x 10^9 cm^{-2} (table IV).

TABLE IV : Results with NInP wafers + etching developed by (4).

PROCESS	n (RT) 10^{15} cm^{-3}	μ(RT) cm^2/VS	n(77K) 10^{15} cm^{-3}	μ (RT) cm^2/VS	Ns 10^{11} cm^{-2}
NInp +5:1:1	0.08	4 600	0.3	107 000	0.16
NInP +5:1:1+HF	0.4	3 910	0.3	81 710	0.8
NInP + HF	0.24	4 500	0.19	98 000	0.5
NInP +5:1:1+HF	0.013	4 700	0.10	170 000	0.026

B. TOF - SIMS

The TOF-SIMS technique gives 2 kinds of fingerprint spectra : the positive ion and the negative ion spectra. The positive ion spectrum (fig 1) shows mainly the hydrocarbon content CHx, C2Hx, C3Hx, C4Hx, C5Hx ... and one peak of interest at mass 28 including Si, CO, C2H4. The positive spectra issued on many of our wafers and on some of the other suppliers are quite similar except for the silicon peak (see below). However, the spectra of supplier A routinely shows a large sodium contamination.
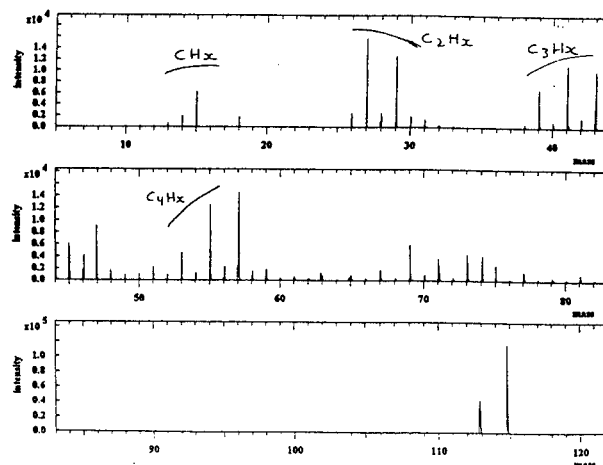
Fig. 1 : TOF-SIMS positive ion spectra.

The negative ion spectra shows different behaviours from sample to sample:

- Peak O(16) and OH(17) are always there ;
- Peaks chlorine (35 and 37) are always present on all InPact samples and on all other supplier samples at the same level ;
- Phosphate peaks (PO2 (63), PO3(79), PO4(95)) are always seen ;
- Sulfate peaks (SO2(64), SO3(80), SO4(96) appear time to time ;
- Hydrated phosphate peaks can also be sometimes identified : PO2H2(65), PO3H2(81), PO4H2(97), PO2H(64), PO3H(80), PO4H(96) ;
- Two peaks, not yet identified and intense can also be there : 59 and 101.
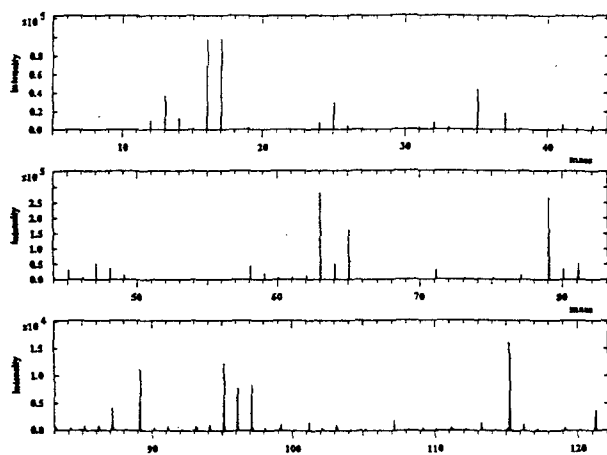
Fig. 2 : TOF-SIMS negative ion spectra (samples without U.V.
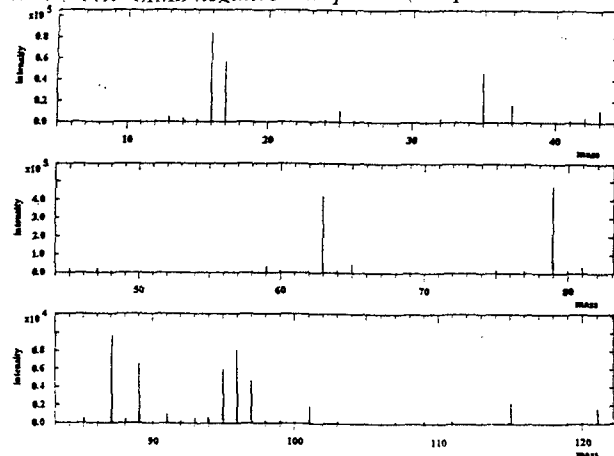
Fig. 3 : TOF-SIMS negative ion spectra (sample with U.V. oxidization)

Fig. 2 shows a standard old InPact processed wafer without U.V. oxidization and Fig. 3 with U.V. oxidization. One can notice the main effect of oxidization ie the drop of the hydrated phosphate peaks. PO2H2 and PO3H2. The peak of Indium (115) decreases with oxidization too. When etching with

H2SO4, the sulfate peaks (SO2, SO3, SO4) come up. When etching with 5:1:1, the sulfate peaks, appear as well as the two non identified and intense peaks (59 and 101). In the case of H2SO4 or 5:1:1 etching, if U.V. oxidization is performed the hydrated peaks (PO2H2, PO3H2) strongly decrease, as well as the Indium peak. TOF-SIMS gives a « signature » for each etching process.

Silicon, as Si⁺, is detected at mass 28 on the positive spectrum.
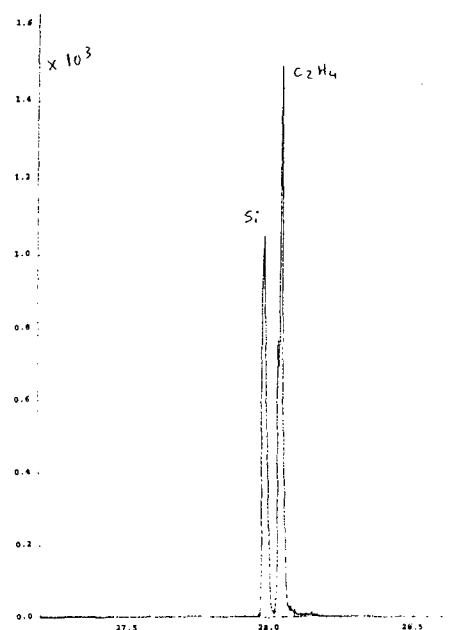
Fig. 4 : TOF SIMS positive ion spectra at mass 28 (Old Inpact Process)
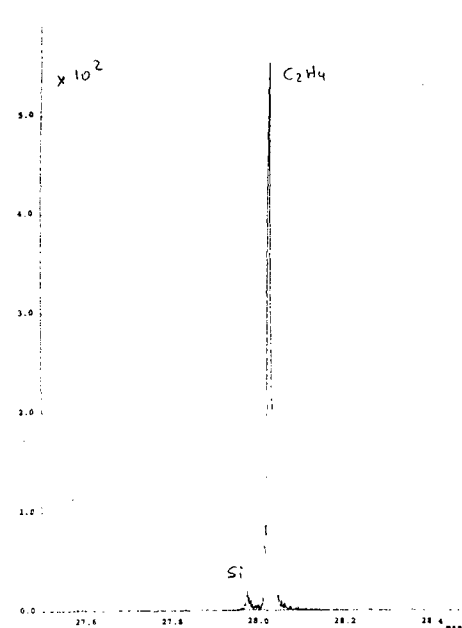
Fig 5 : TOF SIMS spectra of mass 28 (new InPact Process)

422

Fig. 4 gives the silicon spectrum on old InPact processed wafer and Fig. 5 on new InPact processed wafer. At the mass 28, Si, CO,C2H4 and CH2N can be discriminated. We have studied in detail the silicon concentration.

TABLE V : Relative value of silicom for different wafers.

SAMPLE	Silicon concentration
OInP (with U.V.)	1 000 ~ 2 500
H2SO4	310
5:1:1	350
Supplier A	35 ~ 200
Supplier B	70
supplier C	120
NInP (without U.V.)	20 ~ 135

Table V gives the silicon value on differents wafers. The value is relative, but can be compared from one sample to another. However we estimate that « 100 » means an Ns of about a low $10^{11} cm^{-2}$. The detection limit being around « 10 », it means that the low $10^{10} cm^{-2}$ for Ns or ~ 10^{-5} monolayers can be detected. This shows the power of this TOF-SIMS characterization. With TOF-SIMS, we confirm the detrimental action of U.V. oxidization (Table VI).

TABLE VI : Relative value of for different samples without and with U.V. oxidization

PROCESS	InPact Process (intermediate)	H2SO4	5:1:1	New Process (intermediate)
without U.V	360	310	350	20 ~ 135
with U.V.	750	850	690	-

Considering the TOF - SIMS results, as well as the epitaxy results, we offer now a new etching, cleaning, packaging procedure without any U.V. oxidization. Wafers processed with this new InPact process (NInP) show values of silicon in the range 20 ~ 135 wich is very good.

III. Discussion

The basic advantage of the TOF-SIMS comes from its low detection limit which is unique and can not be obtained with Auger or XPS techniques. We performed a large number of MOCVD epitaxial runs and of TOF-SIMS measurements. And we are quite pleased with the accuracy and reproductibility of the results. Thanks to this experimental compaign InPact introduces a new final surface treatment process with a very low silicon content targeted to the microelectronics applications.

An additionnal diagram (fig. 6) entrances the data reliability of this study and the confidence we
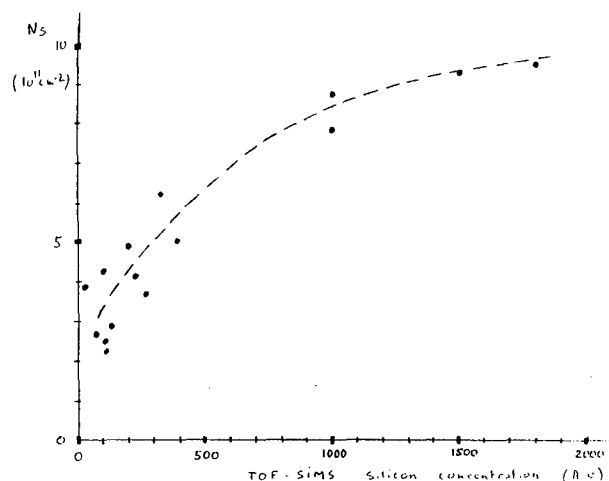
Fig.6 Relation beetwen Ns as measuremed after epitaxy by hall effect versus TOF-SIMS measured silicon concentration.

place into it. On this graph, we plot the Ns concentration (after epitaxy) and the corresponding TOF-SIMS value. Each point represents a couple of wafer (one for TOF - SIMS, one for epitaxy growth) near each other and processed the same way. While the old wafers (OInP) exhibit a TOF-SIMS value of 1000 - 2000, the new wafers (NInP) show a value of ≤100. There is a rather good correlation between these two parameters.

IV. Conclusion

We have pioneered the TOF-SIMS measurement as the state of the art technique for surface analysis. In junction with MOCVD epitaxial runs, we have been in a position to get direct information on the silicon content at the InP substrate epilayer interface. We confirm the clear correlation between the silicon on the surface and the conductive layer after epitaxy. This contamination depends on the chemical treatment and is definitely higher with U.V. oxidation. Thanks to this study, InPact offers a now etching, cleaning, packaging process which is better controlled and reproducible and meets the microelectronics requirements.

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MOVPE GROWTH OF InGaAsP/InP-BASED VERTICAL CAVITY STRUCTURES FOR WAFER-FUSED VCSELS

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Abstract

We have successfully grown InGaAsP/InP-based vertical cavity structures with precisely adjusted resonant-cavity wavelength by metalorganic vapor phase epitaxy (MOVPE). These structures have been used to create vertical cavity surface emitting lasers (VCSELs) that emit at exactly 1.55 μm by wafer-fusing to GaAs/AlAs distributed-Bragg-reflectors (DBRs). In such growths, high lateral uniformity and reproducibility of the InGaAsP layer thickness and composition are essential for obtaining well-defined resonant-cavity and MQW PL peak wavelengths.

I. Introduction

InP-based vertical cavity surface emitting lasers (VCSELs) can emit light whose wavelengths match those of optical fibers (1.55 and 1.3 μm). They have the potential to greatly extend the applied fields, which GaAs-based VCSELs (0.85 and 0.98 μm) are currently building up in optical interconnections and communications. In order to adjust their emission wavelengths accurately, vertical cavity structures with well-defined resonant-cavity wavelengths are required. In GaAs-based VCSELs, the monolithic growth of active layers sandwiched between two Ga(Al)As/AlAs distributed Bragg reflectors (DBRs) is generally performed[1]. On the other hand, in InP-based VCSELs, the difference of refractive indexes between InP and InGaAsP (λ_g=1.4 μm) is less than half of that between GaAs and AlAs (0.5). So, it is necessary to grow 34 pairs (about 8 μm) to obtain the reflectivity of 97%[2] and 50 pairs for 99.9%[3]. This means that the growth of monolithic structures similar to GaAs-based ones is extremely difficult. Typical methods of forming long-wavelength vertical cavity structures are as follows:

(1) Two dielectric mirrors are evaporated on both sides of an InP-based active layer [4][5].

(2) Thick InGaAsP/InP DBR and active layers are monolithically grown and then a dielectric mirror is evaporated [2][3][6].

(3) Two GaAs/AlAs DBRs are wafer-fused to an InP-based active layer [7][8].

The device performance for each method has steadily improved in recent years; however, the emission wavelength control has not yet been well discussed.

We have proposed the novel VCSEL structure shown in Fig. 1(a)[9]. InGaAsP-based multiple quantum well active layers sandwiched between p- and n-type InP/

InGaAsP(λ_g=1.4 μm) DBRs are monolithically grown and then wafer-fused to a GaAs/AlAs DBR. The resonant-cavity wavelength (λ_R) of the whole structure (Fig. 1(a)) is determined by that of the InP-based part (Fig. 1(b)) and not directly influenced by the tuned-wavelength shift of outside mirrors. The emission wavelength of VCSELs is almost completely determined by the λ_R of as-grown InP-based wafer, which depends on the thicknesses of the InP/InGaAsP DBRs and InGaAsP spacer layers. From calculations, a thickness change of 1% is equivalent to a λ_R shift of 12.6 nm for DBR layers and 1.55 nm for spacer layers. So, in order to adjust λ_R exactly to 1550 nm, thickness control of less than 1% is essential. Furthermore, precise adjustment of MQW PL peak wavelength is also required because divergence from λ_R is one of the dominant parameters affecting the VCSEL performance[10].

This paper focuses on our results for the metal organic vapor phase epitaxial (MOVPE) growth of the InGaAsP/InP-based vertical cavity structures and the VCSEL characteristics.
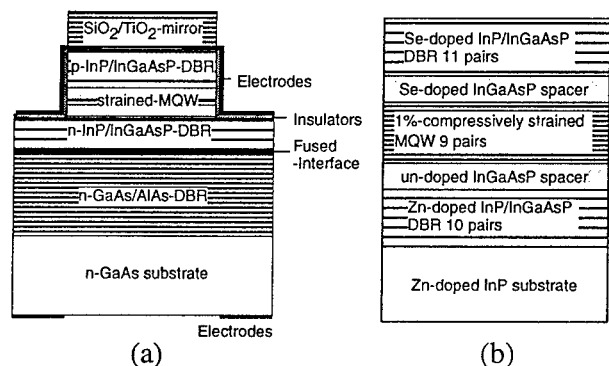
Fig. 1. (a) Wafer-fused VCSEL structure and (b) epitaxial configuration of the InP-based part.

II. Experimental

A. MOVPE Growth

Growth was performed on a 2-inch wafer that was rotated coaxially in a vertical reactor. Back ground pressure during growth was kept at 57 Torr. Trimethyl-indium (TMIn), triethyl-galium (TEGa), arsine (AsH₃), and phosphine (PH₃) were the source materials, and dimethyl-zinc (DMZn) and hydrogen-selenide (H₂Se) were the p- and n-type dopant sources, respectively. The growth temperature of all InGaAsP layers was fixed at 650°C. The growth velocity for both the InP and InGaAsP (λ_g=1.4 μm) was 1.3 μm/h. The doping level of both the p- and n-type layers is 10^{18}cm^{-3}.

In order to check the lateral uniformity and reproducibility of the InP thickness and composition, an InP layer was grown on an InGaAs layer for 20 minutes. After photolithographic patterning, only the InP layer was selectively etched and its thickness was measured by a surface profiler. The lateral uniformity and reproducibility of the InGaAsP composition were checked by two-dimensional mapping of the PL peak wavelength. The measurement was performed with a Nd-YAG laser as an exciting-light source at room temperature.

Before growing whole cavity structures, the MQW active layer and DBR were separately grown. The MQW structure consists of 9 pairs of 1% compressively strained wells (7.5 nm) and InGaAsP (λ_g=1.2 μm) barriers (7.5 nm). In order to adjust the PL wavelength to 1530 nm, well width and composition were slightly changed. The DBR consists of 10-pairs of InP and InGaAsP(λ_g=1.4 μm) layers. The thickness of the two layers in each pair was adjusted to λ/4n of 1550 nm (about 122.2 and 112.6 nm, respectively) by checking the tuned wavelength of reflection spectra.

After finishing the test growth of MQW and DBRs, the whole cavity structure was grown. In order to form a λ-cavity of 1550 nm, the thickness of the InGaAsP (λ_g=1.2 μm) spacer layers on both sides was designed to be 189 nm and tuned experimentally by checking the λ_R of reflection spectra.

B. VCSEL process

The InGaAsP/InP-based vertical cavity structure was grown on a Zn-doped InP substrate. In another MOVPE furnace, 25 pairs of Si-doped GaAs/AlAs DBRs (tuned wavelength of 1550 nm) were grown on Si-doped GaAs substrate. These two epitaxial wafers were fused face to face at 600°C for one hours in a hydrogen atmosphere. After removing the InP substrate completely, mesa structures with a diameter of 25 μm were formed by wet-etching. The p- and n-type electrodes were evaporated on the top and back sides, respectively, and 15 pairs of SiO₂ and TiO₂ dielectric mirrors were evaporated on the p-DBR. Further details are described in ref. (9).

III. Results and Discussions

A. InP and InGaAsP bulk growth

Figure 2 shows the lateral uniformity of InP thickness. For all samples, the thickness shift was less than 1% over more than a 35-mm diameter on the 2-inch wafer. Figure 3 shows the InP layer thickness versus integrated TMIn bubbling time (100 hours produces 130 μm). For each growth sequence, the carrier flow rate of the group III line was kept constant. The thickness shift was less than 1% after almost 300 hours.

For lateral uniformity of InGaAsP composition (λ_g=1.1-1.55 μm), the PL wavelength shift was consistently less than 1% over more than a 35-mm diameter on the 2-inch wafer. The PL wavelength shift of InGaAsP (λ_g=1.4 μm) was only 0.9% after 87 hours of TMIn bubbling time. The thickness uniformity of InGaAsP was similar to that of InP. The above results confirm that thickness control of less than 1% is possible at the following growth.
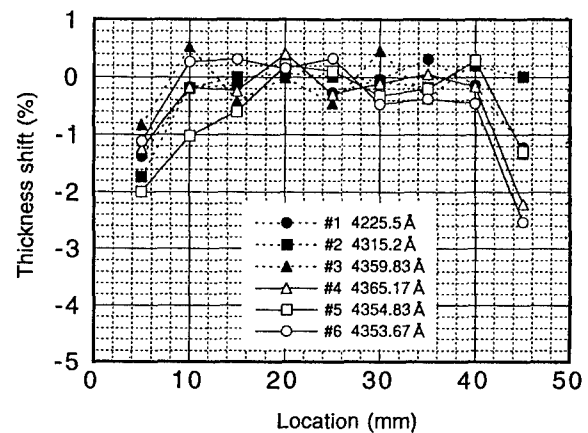
Fig. 2. Lateral uniformity of InP thickness.
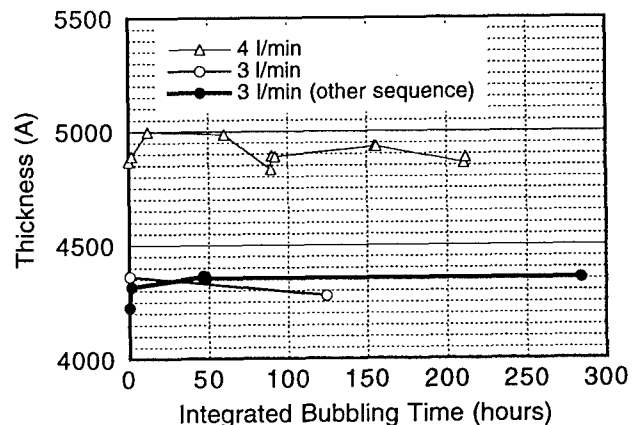
Fig. 3. Reproducibility of InP thickness.

425

B. Test growth of MQW active layer and DBR

Figure 4 shows PL peak wavelengths versus radial location. The wavelength shift is less than 1% almost over the entire 2-inch wafer diameter and the intensity fluctuation is negligibly small. The reproducibility of PL wavelength is represented as a shift of less than 0.3% over several VCSEL growths.

Figure 5 shows reflection spectra of 10 pairs of InP/InGaAsP DBRs. The valley wavelength corresponds to a tuned wavelength. By estimating the thickness deviation from this spectra and correcting the growth times of the next run, we could adjust the tuned wavelength to 1550 ± 5 nm. In Fig. 5, the reflection spectra of p- and n-type DBRs agree well with the calculated ones for a matched DBR. The test growths of the p- and n-type DBRs were performed separately because the refractive indexes for p- and n-doped layers are different.
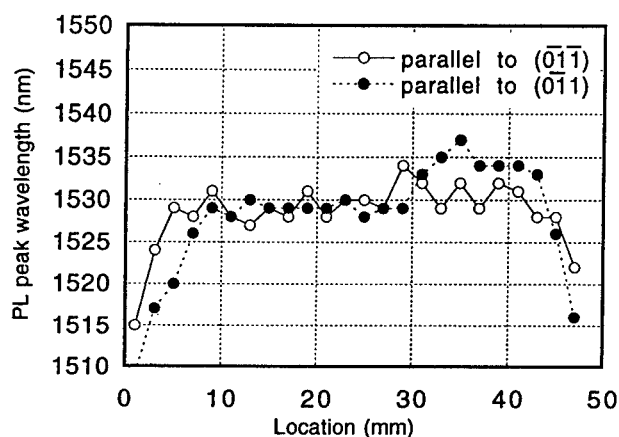
Fig. 4. Lateral distribution of MQW PL peak wavelength.
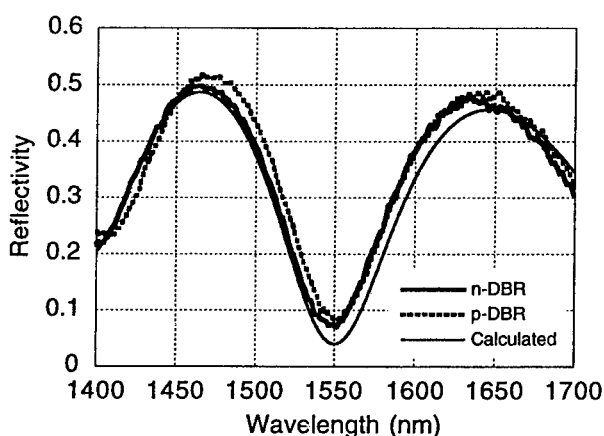
Fig. 5. Reflection spectra of 10-pair InP/InGaAsP DBR.

C. The growth of VCSEL structure

The reflection spectra of the whole cavity structure are shown in Fig. 6. The valley minimum represents the resonant cavity wavelength. Across an area 30 mm in diameter, the resonant-cavity wavelength varies only 2.5 nm from 1550 nm. The wavelength reproducibility over several VCSEL growths was within 10 nm. These results

indicate that the lateral uniformity and reproducibility of InGaAsP thickness and composition described in III-A hold throughout the growth of the thick cavity structure (5.5 μm).
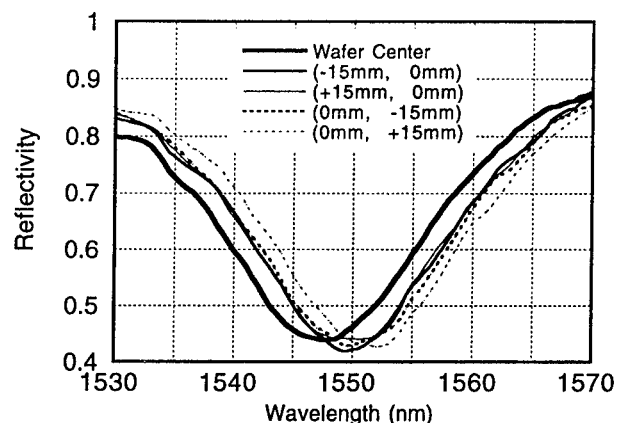
Fig. 6. Lateral distribution of resonant-cavity wavelength.

D. VCSEL characteristics

Figure 7(a) shows the reflection spectra of the as-grown InP-based wafer and the spectra after wafer fusing to a GaAs/AlAs DBR. The resonant cavity wavelength is not effected by wafer fusion. The emission spectra of the VCSEL in the CW-mode at 23°C are shown in Fig. 7(b). At the current of 10 mA, the lasing emission wavelength is 1551 nm, which is almost in accord with the resonant-cavity wavelength in Fig. 7(a). This means that the emission wavelength can be predicted by checking the as-grown resonant cavity wavelength and no additional procedures for adjusting the wavelength are necessary.

Figure 8 shows the current-output curves in the CW mode for a 25-μm diameter device. At 23°C, the threshold current was 8.8 mA, which corresponds to a current density of 1.8 kA/cm². The threshold voltage was only 2.1 V. The maximum output power was 7 μW. The VCSEL operated up to 27°C in the CW mode. We are now trying to improve VCSEL performance by optimizing the pair numbers for both InP- and GaAs-based DBRs and the MQW structures.

IV. SUMMARY

In summary, we have studied the MOVPE growth of InGaAsP/InP-based vertical cavity structures. Sufficient lateral uniformity and reproducibility of InGaAsP thickness and composition were established in order to control the epitaxial configurations precisely. The DBR tuned and MQW PL peak wavelengths were adjusted to 1550 and 1530 nm, respectively in a test growth. By further adjusting the InGaAsP spacer layer thickness in the whole cavity growth, we could obtain an InGaAsP/InP-based vertical cavity structure with the resonant-cavity wavelength of 1550 ± 2.5 nm across an area 30 mm in diameter on a 2-inch wafer. The

emission wavelength of the VCSEL wafer fused to a GaAs/AlAs DBR was in accord with the as-grown resonant-cavity wavelength.
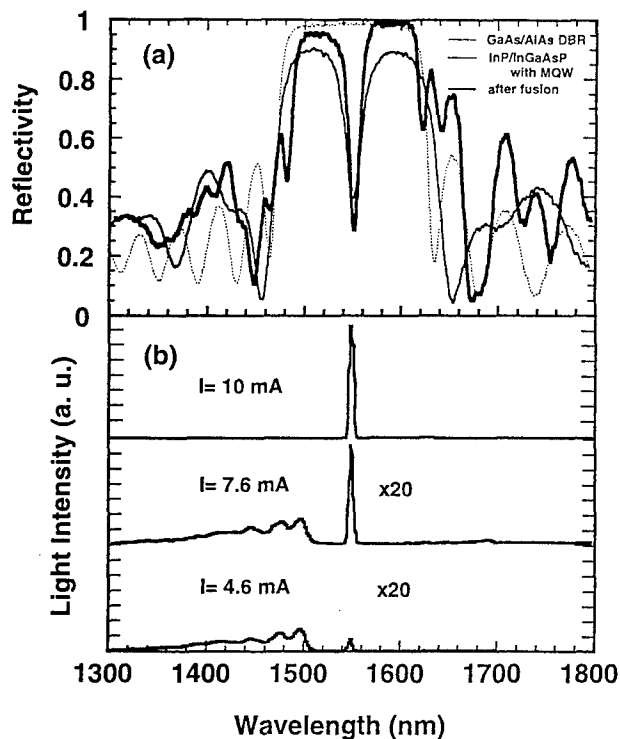
Fig. 7. Reflection and emission spectra of wafer-fused VCSEL.
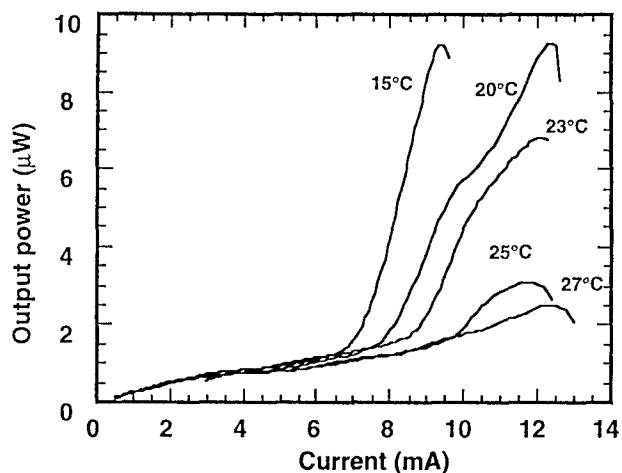
Fig. 8. Current-power characteristics in CW mode for wafer-fused VCSEL.

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427

STRUCTURAL AND OPTICAL CHARACTERIZATION OF InP/InGaAsP DISTRIBUTED BRAGG REFLECTORS GROWN BY CBE

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Introduction

High quality InP/InGaAsP Distributed Bragg Reflectors (DBRs) are a key element in Vertical Cavity Surface Emitting Laser (VCSELs) for long wavelength (1.55 μm) applications [1-3]. Because of the small index difference between InP and InGaAsP, more than 30 periods are needed to obtain reflectivities above 99 %, which makes it a challenge for the crystal growth technique. In this paper we present the structural and optical characteristics of such DBRs grown by Chemical Beam Epitaxy (CBE) at high growth rates that comply with the requirements for the integration in long wavelength VCSELs.

I Growth

All InP/InGaAsP Distributed Bragg Reflectors (DBRs) presented here were grown by Chemical Beam Epitaxy (CBE) equipped with an all-metal pressure regulated gas manifold without carrier gas using TMIn, TEGa, AsH$_3$ and PH$_3$. In order to reduce the duration of the deposition the growth conditions were optimized for higher growth rates. Using growth rates up to 2 μm/h for InP and 3 μm/h for InGaAsP (λ=1.45 μm), 30-50 pairs DBRs were obtained with structural and optical properties sufficient for the long wavelength VCSEL technology. The subtrate temperature during growth was kept at 500°C and a V/III ratio of 8 was used.

For comparing the cristalline quality and the resulting optical properties, InP/InGaAsP DBRs were grown also at the lower growth rate of 1 μm/h. In these latter experiments the substrate temperature and the V/III ratio were reduced to 460°C and 2, respectively.

II Structural characterization

For the structural characterization X-ray diffraction (XRD), Transmission Electron Microscopy (TEM) and Atomic Force Microscopy (AFM) were employed. This comprehensive set of different methods allows to get information about the cristalline perfection, the interface quality, the layer periodicity and the homogeneity of the quarternary alloy.

In spite of the high growth rates and a total layer thickness between 7 and 11 μm, the mirrors showed a smooth morphology and were featureless when imaged by phase contrast microscopy. This is of paramount importance in the context of wafer fusion of one GaAs/AlGaAs DBR to an InP

based cavity and bottom mirror. Also the high resolution X-ray diffraction rocking curve measured for a DBR grown at high growth rates exhibits no significant hint for a degradation of the cristalline quality. As shown in Fig.1 satellite peaks up to the 26th order are well resolved indicating a high structural perfection and a good vertical uniformity.
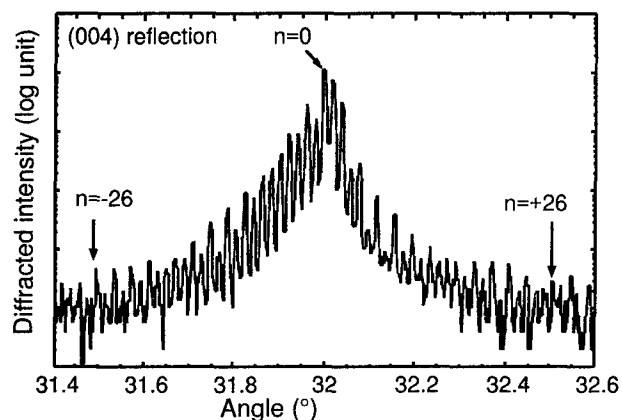
Fig.1. X-ray diffraction rocking curve of a DBR (44 periods) grown at high growth rate. The substrate peak cannot be distinguished due to the high thickness of the superlattice.

As a new characterization method for InP based device material we have used cross-sectional atomic force microscopy (AFM). Based on oxidation-related topography [4-5] the scanning probe technique provides valuable information on InP-based DBRs. Despite the extremely low difference in the oxidation rate of InP and InGaAsP (height difference below 0.5 nm) a significant contrast between both materials can be detected on the [110] cleaved edge oxidized in air. As the measurements show, the oxidation rate of the quarternary alloy

varies nonlinearly within the whole composition range for which GaInAsP is lattice matched to InP (Fig.2.).
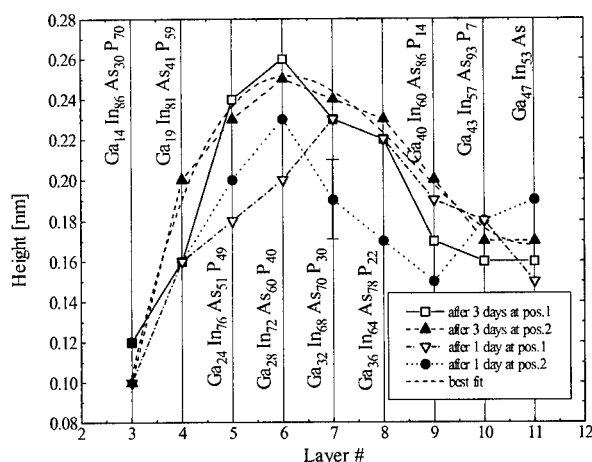
Fig.2. Plot of the oxide layer height for GaInAsP alloys covering compositions between InP and GaInAs, showing a nonlinear behaviour of the oxidation rate.

Due to this fact, the scanning probe technique visualizes not only the interface position, but also chemical variations in the layers. Non optimized DBRs grown by metal-organic chemical vapour deposition (MOCVD) showed additional interface layers which can be attributed to imperfect gas switching sequences leading to the well known enhanced exchange reactions of As and P atoms [6].

The CBE-grown DBR shown in the AFM image above (Fig.3.) exhibits sharp and distinct transitions at each InP/GaInAsP interface, while in the quarternary alloy sub-nanometer scale height variations of the oxide layer are present. These are possibly the sign of short range alloy composition fluctuations within the GaInAsP caused by the high deposition rate used during the growth of this mirror.

The combination of atomic height resolution with a very large field of view is a main advantage of the AFM technique which easily yields the complete imaging of these thick (up to 11 μm) InP based DBRs. Using the good lateral resolution the individual layer thickness can be directly measured by AFM. The values given in Table1 show a good agreement between the measurements performed using AFM and X-ray diffraction and the nominal thicknesses.

layer	AFM [nm]	X-ray [nm]	nominal[nm]
GaInAsP	120.7 ± 4	-	122.4
InP	114.0 ± 4	-	113.5
period	234.7 ± 4	237.5 ± 2.5	235.9

Table 1. Nominal and measured thicknesses of the individual layers of a DBR grown at high growth rate.
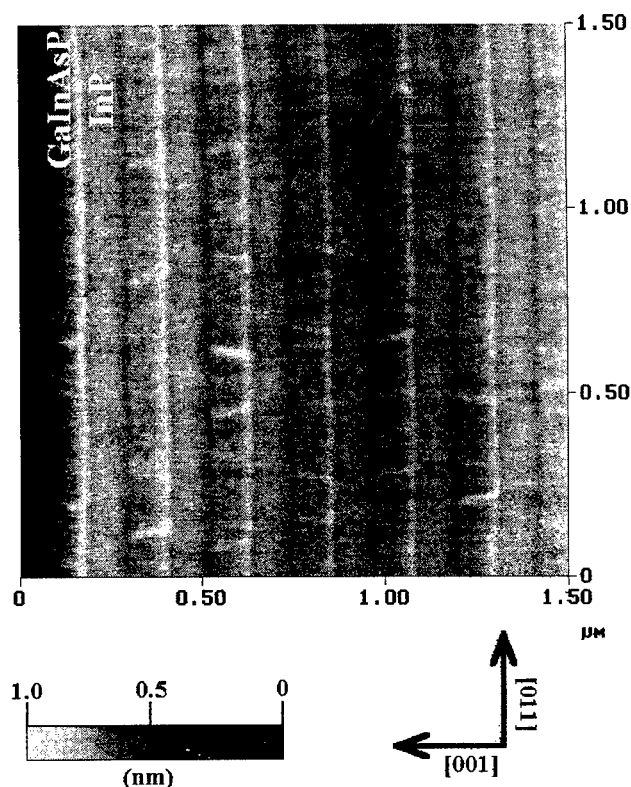
Fig.3. AFM picture of the cleave edge of a DBR grown at high growth rates. It reveals short range alloy composition fluctuations within the InGaAsP visible as bright features.

As a relatively quick and easy approach the AFM technique is sensitive to the interface structure, the alloy composition, the layer thickness and defect creation on lateral scales below 5 nm, and thus provides valuable feedback information for the optimization of the growth conditions.

In addition to cross-sectional AFM imaging, TEM was carried out to study the cristalline structure of the DBR in further detail. The samples for TEM investigation were prepared in such a way that the electron beam could be directed along the [0-11] and the [011] directions. The diffraction vectors used were 022 and 0-22, respectively. These diffraction conditions generate images perpendicular to the interface plane between the InGaAsP and the InP layers (cross sections).

Figure 4. shows two dark-field cross section TEM micrographs of an InP/InGaAsP DBR grown at high growth rates taken along the [0-11] direction (a) and along the [011] direction (b) using the diffraction conditions described above. Both images reveal modulations within the InGaAsP layers visible as irregularly shaped bright features. The modulation length appears to be about 50-100nm in the [0-11] direction and about 20nm in the [011] direction. For other diffraction conditions these contrast fluctuations are very weak or not visible. From this we conclude that strain related effects along the [022] and [0-22] directions may explain the observed

contrasts. La Pierre *et al.* [7] have reported similar observations on InP/InGaAsP material grown by gas source molecular beam epitaxy (GSMBE). They have interpreted their results as spinodal decomposition of the quaternary alloy which results in strain within the InGaAsP layers.

(a)

100 nm

InP

(b)

100 nm

InP
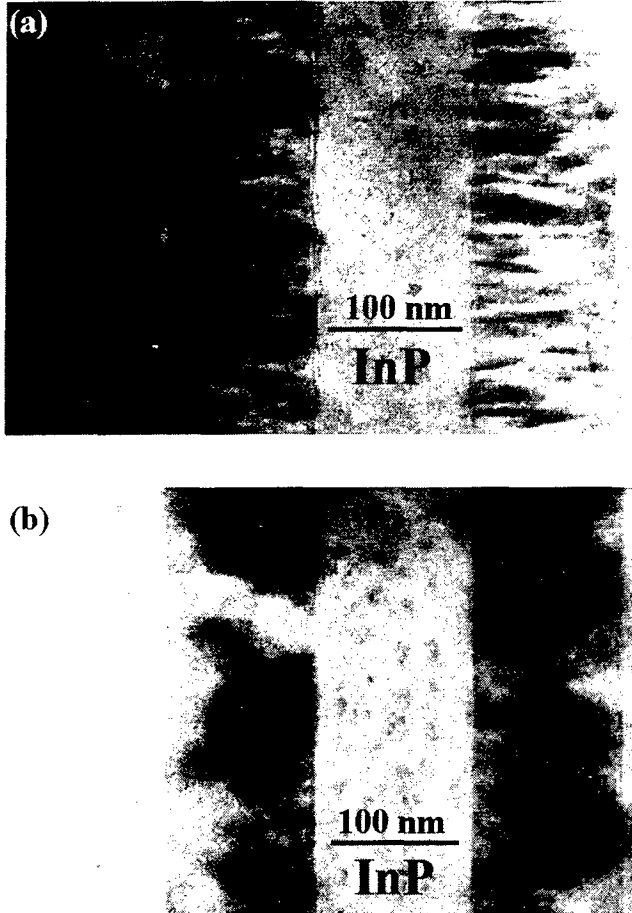
Fig.4. Dark-field cross section TEM micrographs of an InP/InGaAsP DBR grown at high growth rate revealing short range composition fluctuations within the InGaAsP alloy. The figure compares images taken along the [0-11] direction (a) and along the [011] direction (b) using the 022 and 0-22 reflections, respectively.

For the DBRs grown at high growth rate the TEM observations agree very well with the results obtained by cross-sectional AFM and confirm the hypothesis of a decomposition of the InGaAsP alloy already derived from these measurements. DBRs grown at lower groth rates (1 μm/h) do not exhibit decomposition related features in AFM images. But also in this case with TEM a very weak contrast due to decomposition induced strain is still detectable. However, due to the limited lateral resolution of the AFM technique and the low difference in oxidation between InP and InGaAsP these weak composition effects are still below the detection threshold of the scanning probe method.

From thermodynamic considerations [8] low growth temperatures are expected to favour the occurence of spinodal decompositions. Therefore, we attribute the observed decomposition in our experiments mainly to the low growth temperature used during the CBE growth. Additionally, the high growth rates may play a role for this complex process.

III Optical characterization

Reflectivity mapping performed on DBRs grown at a high growth rate on 2" wafers show a variation of the Bragg wavelength of ±0.5% over a 40mm diameter area. The absolute reflectivity of the DBR was measured using multiple reflections on two parallel DBR samples. This technique allows a very high accuracy without the need for a calibrated reference mirror. At the center of the stop band (l = 1575nm) a reflectivity of 99.1±0.1% is obtained already on a 30 pairs DBR (Fig. 5.). A 50 periods DBR with the same compositions would feature a reflectivity in excess of 99.6% when used as a bottom reflector, even in the presence of realistic absorption loss of 10 cm^{-1}. Simulations of the reflectivity curve of this sample also give an accurate evaluation of the refractive index of InGaAsP. Using n(InP) = 3.166 at 1.55μm, we obtain n(InGaAsP) = 3.436±0.006 at 1.55μm.

R_{max}= 99.1 ± 0.1% at 1575 nm
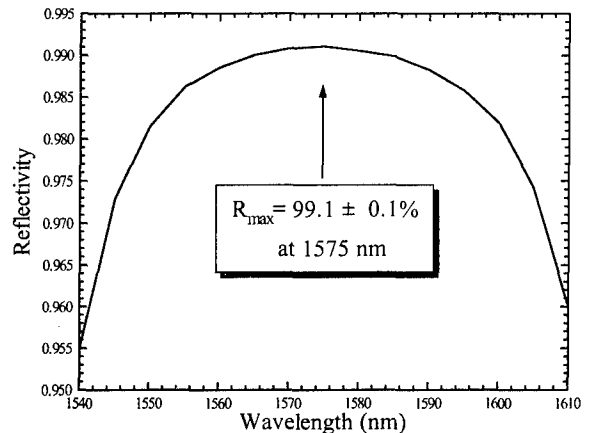
Fig. 5. Stop-band reflectivity of an InP/InGaAsP DBR grown at high growth rates measured with a multiple reflection technique.

IV Summary

Employing a set of different structural and optical characterization methods we have carried out a detailed investigation of InP/InGaAsP DBRs grown at high growth rates by CBE. While there are signs of alloy composition fluctuations on a microscopic scale, the macroscopic cristalline quality and the high reflectance make them suitable for integration in a 1.55μm VCSEL.

Acknowledgment

430

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MOMBE GROWTH OF SEMI-INSULATING GaInAsP(λ_g=1.05 μm):Fe OPTICAL WAVEGUIDES FOR INTEGRATED PHOTONIC DEVICES

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Abstract

Iron doping using elemental source material evaporated from a conventional effusion cell was applied during MOMBE growth of semi-insulating InP and GaInAsP(λ_g=1.05 μm) for waveguide applications. The influence of the growth temperature and the doping concentration on the electrical and optical properties was investigated in the range from 455°C to 505°C and $5 \cdot 10^{15}$ cm^{-3} to $5 \cdot 10^{19}$ cm^{-3}, respectively. High optical quality is demonstrated by the appearance of excitonic emission in iron doped layers at 10K. Resistivities in excess of 10^9 Ω·cm were obtained for both materials at medium doping levels grown at the lower end of the investigated growth temperature range. In addition, SIMS measurements revealed homogeneous incorporation behaviour of the iron dopant in these materials. A tendency towards some accumulation/segregation of the iron dopant was observed at higher doping levels and growth temperatures resulting in some decrease of the resistivity. GaInAsP/InP waveguide structures grown at 485°C (which is the minimum temperature necessary for selective deposition) showed resistivities of $5 \cdot 10^7$ Ω·cm in combination with low optical losses of 2.5±0.5 dB/cm.

I. Introduction

For monolithically photonic integrated circuits (PIC) optical waveguides (WG) are required to optically interconnect the different devices on the chip. Besides low optical losses, these WGs need to be semi-insulating for electrical isolation purposes, and high quality selective area growth is required to accomplish butt coupling between the WG and active devices, in particular lasers (1). Metal organic MBE (MOMBE) has been applied as the epitaxial technique of choice for material deposition offering simultaneously high quality of InP/GaInAsP layer structures (2), extreme uniformity on a 2" Ø wafer scale (3) improved selective growth (4,5) and semi-insulating behaviour using iron doping (6).

In this contribution, a systematic study of the material characteristics of Fe doped InP and GaInAsP(λ_g=1.05 μm) (in the following denoted as Q(1.05)), based on the evaporation of elemental iron source material, is presented in terms of the electrical and optical characteristics of the material and the incorporation behaviour of the dopant. In combination with low loss waveguide structures (7), Fe doping offers the possibility to fabricate semi-insulating devices whilst simultaneously maintaining low optical losses.

II. Experimental

The GaInAsP material investigated was grown in a diffusion pumped MOMBE system using solely pressure control of phosphine/arsine (PH$_3$/AsH$_3$) and trimethylindium/triethylgallium (TMIn/TEGa) which were used as group-V and group-III starting materials, respectively, without adding hydrogen as a carrier gas. PH$_3$ and AsH$_3$ were pre-cracked in a high-pressure cracking cell at 900 to 950°C. TMIn and TEGa were injected via a low-pressure gas cell and were cracked on the hot growing surface. Fe doping was achieved by thermal evaporation from a 5N elemental source material block from a conventional effusion cell. The growth temperature (T_g) was monitored with a pyrometer (λ=950 nm) and was varied between 455°C and 505°C. Growth was initiated at the oxide desorption temperature (T_g=465°C) and the growth temperature was ramped to its final value instantaneously when was growth started.

The properties of the grown GaInAsP layers were assessed by using standard characterisation tools. X-ray diffraction (XRD), 300K and 10K photoluminescence (PL) and secondary ion mass spectroscopy (SIMS) were used to determine the GaInAsP alloy composition as well as the structural and optical quality of the layers. Material resistivity was determined from the vertical I/V-characteristics of Ø:200 μm mesas fabricated from

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1 μm thick epi-layers on conducting InP:S substrates similar to reference (6) using Ti/Au contacts.

WG structures were defined in a conventional manner using the finite-difference method for device design, RIE for rib definition and the Fabry-Perot resonance technique for loss measurements. (For further details cf. (7).)

III. Results

High quality of the homogeneous InP and Q(1.05) materials has been demonstrated by x-ray diffraction FWHM values approaching theoretical limits as well as 10K PL reaching record low FWHM values of 4.4 meV for the quaternary material (7) and showing excitonic fine structure in InP. The residual carrier concentration was below $1 \cdot 10^{15}$ cm^{-3} for both materials. The lateral Q(1.05) material uniformity was found to correspond to a variation of the emission wavelength of ± 2 nm across the whole 2" Ø wafer and to a variation of the lattice mismatch $\Delta(\Delta a/a)$ of ± 120 ppm. In addition, the PL intensity remains stable within a factor of two across the 2" Ø wafer.

A. Doping Characteristics

Fe doping of InP and GaInAsP between $4 \cdot 10^{15}$ cm^{-3} and $4 \cdot 10^{19}$ cm^{-3} was achieved by variation of the source temperature between 800°C and 1100°C. Fig. 1 shows the observed Arrhenius-type dependence of the Fe concentration, as determined from SIMS measurements, on the source temperature. The linear dependence is indicative of a sticking coefficient which is at least close to one. Additionally, the absence of any deviation from the linear relationship at high doping levels suggests the absence of formation of extended Fe clusters. This is also supported by the SIMS, being capable to detect clustering, i.e. in MOVPE Q(1.05):Fe (8), which did not give any indication in
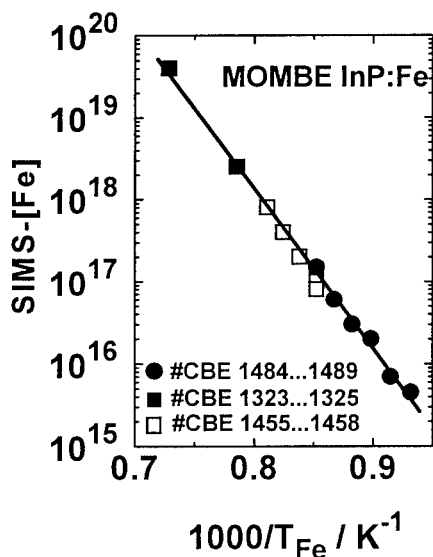
Fig. 1: *Arrhenius-type dependence of incorporated Fe concentration as measured by SIMS on the source temperature.*

MOMBE material. The data given in Fig. 1 have been collected over a long period corresponding to the growth of in excess of 150 layers. The long term stability of the Fe source is demonstrated by the fact that the deviation of all the data from the linear behaviour is obviously small. Thus, reaction of the source with the MO environment as observed for silicon (9) can be excluded.
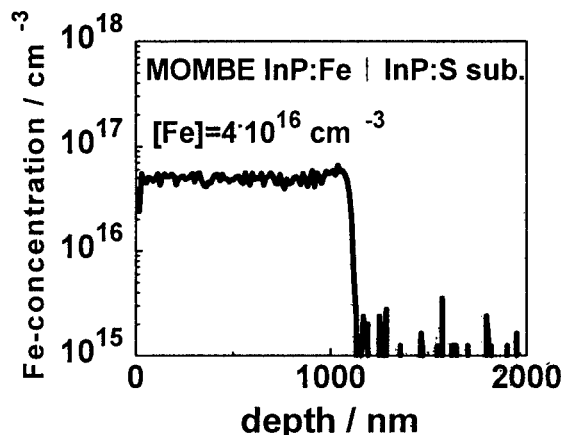
Fig. 2: *SIMS depth profile of Fe in homogeneously $4 \cdot 10^{16}$ cm^{-3} doped InP.*

Incorporation of Fe was studied by SIMS profiling. Non uniform incorporation behaviour resulted using T_g values around 500°C and Fe concentrations ([Fe]) higher than 10^{17} cm^{-3}. Surface accumulation of Fe in combination with reduced concentrations near the interface were observed and are indicative of surface segregation. In addition, some Fe accumulation at the substrate/layer interface occurs. Reduction of T_g and [Fe] drastically improves the uniformity of Fe incorporation as is demonstrated in Fig. 2. Only some minor accumulation of Fe at the substrate/layer interface is still present.

B. Optical Characteristics

High optical quality of MOMBE InP:Fe and Q(1.05):Fe is maintained, at least at moderate Fe doping levels, despite the incorporation of the deep impurity levels. Fig. 3 shows a summary of representative 10K PL spectra. The spectrum of the undoped InP reference shows dominating emission in the excitonic region centered around 1.418 eV due to the dominance of the donor bound exciton. Resolved excitonic fine structure was observed for residual carrier concentrations below $5 \cdot 10^{14}$ cm^{-3}, as also reported in (10). Impurity related transitions centered at 1.381 eV are weak suggesting low acceptor levels.

Incorporation of Fe leads to a marked increase of the impurity related emission and the appearance of the corresponding phonon replica at 1.337 eV to the expense of the excitonic emission with increasing [Fe] from $7 \cdot 10^{15}$ cm^{-3} to $5 \cdot 10^{16}$ cm^{-3}. According to (11) the emission line at 1.380 eV is assigned as a band acceptor transition (e,A°) related to carbon acceptors (C_p). This increase in carbon level with Fe
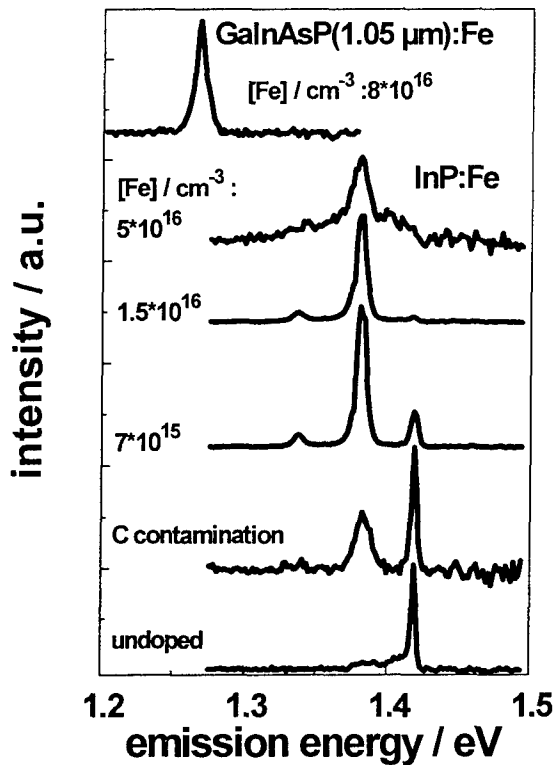
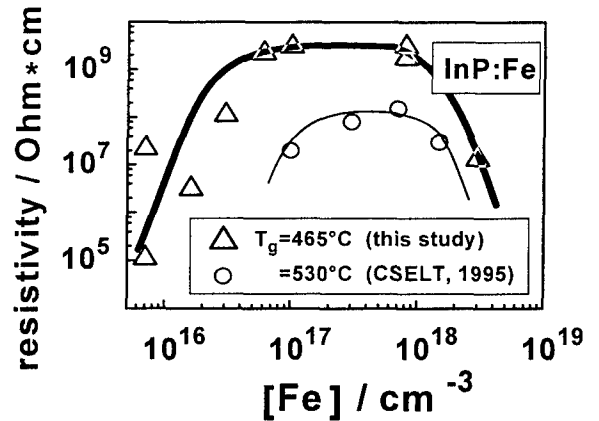**Fig. 3:** *10K PL spectra of InP:Fe and Q(1.05):Fe for various Fe doping levels.*

Fig. 4: *Dependence of InP resistivity on [Fe] for deposition at $T_g=465°C$. (Reference data for $T_g=530°C$ are given for comparison.)*

doping level is already known to occur for Si doping (12) and Be doping (13) and is attributed to be linked with the high source temperatures. This conclusion is supported by the spectrum labelled 'C contamination' which is an undoped InP layer with the Fe source at elevated temperature (shutter closed). In addition, this increasing carbon uptake leads to some slight roughening of the growth surface and a decrease of the overall PL intensity amounting to roughly an order of magnitude for mid 10^{16} cm^{-3} Fe doping levels.

The same trend was also observed for Q(1.05) layers. The upper PL trace in Fig. 3 clearly demonstrates that high optical quality of Fe doped Q(1.05) is achieved. A FWHM of 8 meV, as compared to 4.5 meV in undoped material, is obtained.

C. Electrical Properties

Material resistivities were extracted from the vertical electrical transport data of InP:Fe and Q(1.05):Fe on InP:S substrates. The I/V-characteristics show a linear behaviour over 4 orders of magnitude allowing for an accurate determination of the resistivity. Due to the layer thickness of 1 μm, the onset of breakdown occurred already near 8V. The dependence of the material resistivity on Fe concentration was investigated aiming in material with semi-insulating behaviour. Similar resistivities were measured for InP:Fe and Q(1.05):Fe. The representative results of InP:Fe given in Fig. 4 indicate that at Fe doping levels between $5 \cdot 10^{16}$ cm^{-3} and $2 \cdot 10^{18}$ cm^{-3} relatively constant

resistivities were achieved. At lower as well as at higher levels reduced resistivities occurred. While the decrease at high [Fe] is not clear and may be attributed to microcluster formation not detectable by SIMS, the decrease at low Fe levels is believed to be due to incomplete compensation of residual carriers though their concentration is below 10^{15} cm^{-3}. The maximum resistivities measured were in the range $(2\pm1) \cdot 10^9$ Ω·cm, which are the highest values reported for MOMBE grown material. For comparison, literature data for MOMBE InP:Fe grown at $T_g=530°C$ (14) are included in Fig. 4. The [Fe] dependence of the resistivity is qualitatively similar despite a general trend to markedly lower resistivity values. Based on the results of our investigation of the dependence of the resistivity on T_g, the discrepancy in Fig. 4 can be explained. The T_g dependence of the resistivity shows a monotonous decrease towards $1 \cdot 10^8$ Ω·cm increasing T_g to 500°C and remains fairly constant for higher T_g values for both materials investigated. Thus, this Tg dependence has to be taken into account if low Tg values are not applicable, i.e. in case of selective MOMBE growth.

D. Optical Waveguides

The optical waveguide layer structures investigated were composed of a 1000 nm InP buffer and a 1100 nm Q(1.05) WG layer. A 30 nm thin InP marker layer is buried 300 nm below the surface for controllable rib height definition. Optical losses of the undoped 2.5 μm wide MOMBE rib WGs amounted to record low values of 0.1...0.2 dB/cm, with typical values being around 0.5 dB/cm. The degree of lattice matching was found to most severely influence the optical losses. A lattice mismatch of ±2000 ppm results in an increase of optical losses to roughly 2 dB/cm. This leads to the conclusion that higher losses are predominantly linked with the appearance of a rough surface morphology, i.e. in the case of a high degree of mismatch.

Fe doped WG structures were deposited at 485°C to simultaneously make possible selective deposition and high

434
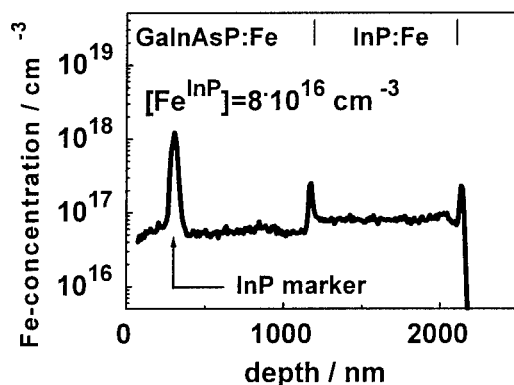
Fig. 5: SIMS depth profile of Fe in a GaInAsP/InP WG structure (cf. text) doped with a constant Fe source temperature of 900°C.

resistivities. For both materials, Fe doping levels of $8 \cdot 10^{16}$ cm^{-3} were applied to additional maintain acceptable optical quality. The mean resistivity of the whole WG stack amounted to around $5 \cdot 10^{7}$ $\Omega \cdot cm$. This slightly lower value as compared to single layers is only in part due to the higher T_g and can be further understood from the Fe profile in the WG layer as shown in Fig. 5. In the individual layers uniform incorporation of the Fe impurities is observed. In the Q(1.05) layer the concentration is somewhat lower due to the constant Fe flux (T_{Fe} is constant) and the slightly higher growth rate applied. In addition, some accumulation at the layer interfaces is observed which is most severe in the InP marker region. This, in combination with the lower Fe level in Q(1.05), not only explains the slightly lower resistivities but also the moderate increases of the optical losses to 2.5±0.5 dB/cm obtained in the semi-insulating Fe doped WG devices. This Fe interface accumulation is speculated to be associated with the simultaneous accumulation of carbon (as observed in the case of Si and Be doping) giving rise to some degraded surface morphologies as compared to undoped WG material. In addition, the intentionally incorporated deep Fe levels may also contribute to the increased internal optical losses.

Summary

Fe doping of InP and Q(1.05), which are the base materials for optical waveguides, by MOMBE using a solid Fe source has been systematically studied. Based on these results semi-insulating WG structures of high optical quality have been developed. Devices showing optical losses of 2.5±0.5 dB/cm appear adequate for application in butt coupling integration schemes using selective MOMBE deposition.

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BENEFITS AND LIMITATIONS IN BARRIER DESIGN IN InAsP/GaInP STRAIN-BALANCED MQWS FOR IMPROVING THE 1.3μm WAVEGUIDE MODULATOR PERFORMANCE

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Abstract

We have investigated the limitations in the barrier design for InAsP/GaInP strain-balanced multiple quantum wells (MQWs) by measuring double-crystal x-ray rocking curves and room-temperature photoluminescence. We show that in thin-barrier (~ 70 Å) structures with 8 MQWs, zero net strain can not be achieved due to the relaxation of the GaInP barriers caused by higher tensile strain. The net strain has to be designed at the compressive side and within the range of -0.26% to -0.54% to obtain high structural stability. Photocurrent spectra show that with 70 Å-thick barriers, the MQW region is 35% more absorptive than with 115 Å-thick barriers.

I. Introduction

There has been considerable interest in strain balance, namely, heterostructures of III-V compound semiconductors with alternative compressive and tensile strain, to increase the stability of the structures.(1)-(11) This technique has been successfully applied to a variety of III-V material systems, especially multi-quantum wells (MQWs) for optoelectronics applications, e.g., InAsP/GaInP and InAsP/InGaAsP MQWs for lasers (7) and optical modulators (1),(2),(4),(6),(8)-(11). We have demonstrated high-performance electroabsorption (EA) waveguide modulators at 1.3μm wavelength using InAsP/GaInP MQWs for RF photonic links (11), in which a large slope efficiency in the transmission-voltage curves is desirable (11). Such modulators have a p-i-n structure with the MQWs as the i-region. The higher the well/barrier thickness ratio is, the more absorptive that region is, and therefore, the higher the slope efficiency of the modulator. The InAsP well width in our structures is 90~95Å which has the best electroabsorption properties. Therefore, using thinner barriers becomes the only way to increase the well/barrier thickness ratio. To meet the 1.3 μm wavelength requirement the compressive strain in InAsP is 1.3%. In this work we set our target barrier thickness at 70 Å (compare with our conventional 120 Å).

One of the most favorable design criteria in strain-balanced structures is to achieve approximately zero net strain for high stability. However, there is a limitation on this approach. To balance quantum wells with given compressive strain and thickness, the product of tensile strain and thickness for the barriers has to cancel out that of the wells. Therefore, if one wants to increase the barrier strain to obtain a zero net strain in a thin-barrier structure, the single layer critical thickness of the GaInP barriers may be exceeded. On the other hand, if the barrier strain is not high enough when the barriers become thinner, the critical thickness of the whole MQW stack may be exceeded due to too high a net strain. These issues are investigated and the results are reported in this paper. As the results show, in this thin barrier case (70 Å) zero net strain is neither necessary nor achievable.

II. Experimental

The MQW samples were grown in a Varian GEN-II molecular beam epitaxy (MBE) system modified for gas-source MBE growth. Thermally decomposed AsH_3 and PH_3 were used as the group V sources, and elemental In and Ga as the group III sources. The samples were grown on S-doped n^+-InP (001) substrates. The growth

temperature was 460°C, and the InP growth rate was typically 1 μm/hour. The growth rate was first determined by intensity oscillations of reflection high-energy electron diffraction (RHEED) and then confirmed by computer simulation of double-crystal x-ray rocking curves (DCXRC) of MQW samples, which also provide accurate determination of the alloy compositions and layer thicknesses. In the thermal annealing experiment, a conventional tube furnace was used with a forming gas ambient. During the annealing, the samples were placed face down on a piece of InP wafer to avoid losing phosphorus at elevated temperatures.

Table 1. Structural parameters of the $InAs_xP_{1-x}/Ga_yIn_{1-y}P$ MQW samples

sample#	x	well thickness l_w (Å)	y	barrier thickness l_b (Å)	barrier strain ε_b	number of periods	PL intensity (a.u.)	net strain $\overline{\varepsilon}$
1994	0.39	93	0.25	68	1.75%	7	2.0e-6	0.10%
1998	0.39	93	0.24	68	1.71%	7	1.7e-4	0.09%
1999	0.39	91	0.18	67	1.28%	7	1.8e-4	-0.29%
2013	0.40	93	0.14	70	0.96%	8	3.5e-3	-0.26%
2062	0.36	107	0.08	78	0.57%	8	1.3e-3	-0.50%
2063	0.40	100	0.05	75	0.36%	8	1.2e-3	-0.54%
2069	0.42	94	0.02	70	0.14%	8	4.7e-4	-0.68%
2070	0.42	94	0	70	0%	8	0	-0.75%

III. Results and discussion

For comparison, a set of samples were grown with similar structural parameters except the intentionally varied Ga composition, and therefore strain, in the barriers. DCXRCs, measured for all of the samples, are plotted in Fig.1. The structural parameters were determined by computer simulations of these rocking curves and they are listed in Table 1. Room-temperature photoluminescence (PL) of these samples was also measured to characterize their optical quality. The PL spectra show that the n=1 electron-heavy hole exciton peak of all the samples has almost the same full width at half maximum (FWHM), which is around 20 meV, whereas the intensity changes significantly from sample to sample. The intensities are shown in Fig. 2 as a function of barrier strain. Sample 1994 was designed to have a zero net strain, but its DCXRC shows broadened satellite peaks, indicating rough interfaces of the MQWs. This poor crystalline quality is also confirmed by the low PL intensity. Because $InAs_{0.4}P_{0.6}$ wells with the same composition and width were used in our previous very good samples with thick barriers (120 Å), the only possible reason for this interface roughening is relaxation of the $Ga_{0.25}In_{0.75}P$ barriers (68 Å).

As can be seen in Fig. 1, the satellite peaks become very sharp for sample 2013 and remain sharp in 2062, 2063, and even in sample 2069 when the barrier strain is as low as 0.14%. In sample 2070, there is no Ga in the barriers, in other words, no strain balance, and the DCXRC does not show any satellite peaks indicating lattice relaxation. This result is consistent with the PL measurements shown in Fig. 2 where sample 2070 shows no PL signal.

The structures with Ga composition ranging from 0.02 to 0.14 (strain 0.14%-0.96%) show good crystalline quality. To verify whether the structures are metastable due to the relatively low growth temperature, 460°C, we annealed samples 2013, 2062, 2063, and 2069 at 600°C for 30 minutes. The DCXRCs after annealing are shown in Fig. 3. Comparing with Fig. 1, we can see clearly that samples 2013, 2062, and 2063 remain a good quality after the annealing, whereas sample 2069, with the largest net strain, shows broadened satellite peaks indicating some strain relaxation. Therefore, sample 2069 was metastable before annealing and the other three samples are thermally stable at up to 600°C.

In samples 1994, 1998, and 1999, the $Ga_yIn_{1-y}P$ barriers have so much strain that the critical thickness is less than

70 Å, so these barriers undergo strain relaxation. In the three stable structures, namely, samples 2013, 2062, and 2063, the barriers are within their critical thickness, and the net strain of -0.26% to -0.54% makes the whole MQW structure also within the critical thickness. Therefore, they have high crystalline quality and thermal stability. Sample 2069 and 2070 have too large a net strain that causes strain relaxation at growth temperature (460°C) or annealing temperature (600°C). Therefore, strain balance is necessary to obtain a stable MQW structure, but zero net strain is not necessary and may not be achievable.

Fig.2. PL intensities of the MQW samples.

Fig.1. The curves are DCXRCs of the MQW samples. The numbers on the right of each curve is the sample number.
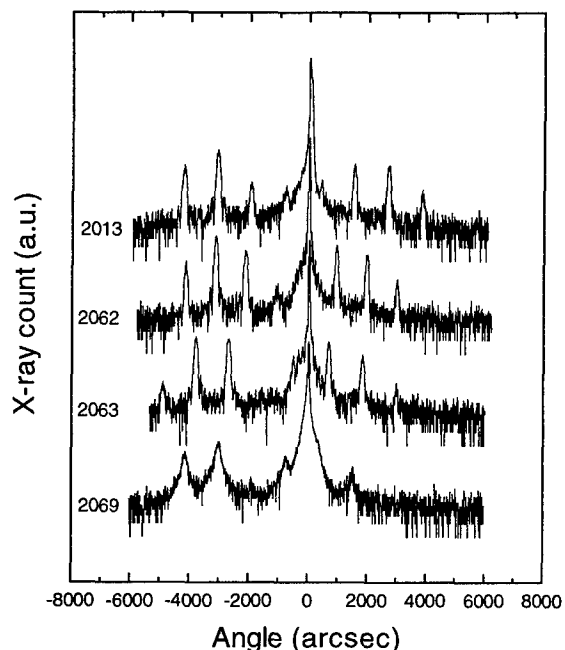
Fig. 3. DCXRCs of the MQW samples before and after the thermal annealing at 600C for 30 min.

Another thing worth noticing is the significant difference between the crystalline quality of samples 2069 and 2070, although the difference in structure is only two percent Ga in the barriers, or only 0.14% difference in barrier strain. This large difference in the crystalline quality can not be solely attributed to strain effect. The mechanism for this is not clear yet and is still under investigation.

Sample 2013 is a p-i-n structure, so we can measure photocurrent (PC) spectra. Mesa diodes with a 500 µm diameter were defined by wet chemical etching, and a ring-

shaped AuZn/Cr contact was evaporated onto the p-InP cap layer. In was used as the n-type contact on the back side of the substrate. The PC signal was collected via the ring-shaped electrode and the back contact. For comparison, the PC spectra of sample 1922, which has 6 periods of $InAs_{0.4}P_{0.6}$ (90 Å)/$Ga_{0.13}In_{0.87}P$ (115 Å) MQWs, were also measured. The i-region thickness of sample 1922 is 0.134 µm, approximately the same as that of sample 2013

(0.137 μm), which means the same built-in field in the MQWs. In sample 2013, thinner barriers enabled us to insert 8 QWs into the i-region, two more QWs than in sample 1922. The same light intensity was used for the PC measurements of the two samples. By comparing the n=1 samples, 1.38. The line widths of the two spectra are approximately the same, which is 7 meV. These results indicate that with 70 Å barriers, the MQW region is 35% more absorptive than that with 115 Å barriers, assuming the same quantum efficiency in the two samples. It is reasonable to expect a higher slope efficiency in the waveguide modulator devices with thin barriers. Those devices are still under investigation and the results will be reported else where.

IV. Conclusions

We have investigated the limitations in barrier design for InAsP/GaInP strain-balanced MQWs, namely, the critical thickness of the barriers and the net strain of the whole MQW stack. We have shown that in the thin-barrier (~ 70 Å) structures with 8 MQWs, zero net strain can not be achieved due to the relaxation of the GaInP barriers. The net strain has to be designed at the compressive side and within the range of -0.26% to -0.54% to obtain a high structural stability. We have demonstrated that with 70 Å-thick barriers, the MQW region is 35% more absorptive than with 115 Å-thick barriers.

Acknowledgment

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heavy hole exciton peak intensity, we found that the PC signal of 2013 is 1.35 times that of 1922, which is in good agreement with the ratio of the total QWs thickness in the two

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InAsP/In[Ga]P MQWs for 1.55μm modulators grown by solid-source MBE

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Abstract

Two multi-quantum wells of nominal composition $In_{0.45}As_{0.55}P/InP$ and $In_{0.4}As_{0.5}P/In_{0.95}Ga_{0.5}P$ have been grown by solid source MBE. X-ray diffraction showed that neither structure was relaxed with respect to the substrate despite compressive well strain of 1.6-1.8%. Optical characterization showed narrow exciton linewidths (~20meV FWHM) at room temperature. An absorption coefficient at the exciton peak of 21,000cm^{-1} was found from transmission measurements. There is also a rapid Stark shift for these 85nm wells leading to maximum modulation at only 4-5V for 0.3μm intrinsic region. These results imply that for a similar 50 period structure with 1μm intrinsic region a contrast ratio of 2.3dB could be achieved at less than 20V.

I. Background.

The smaller valence band offset of InAsP/InP compared to InGaAs/InP has led to much interest in InAsP/In[Ga]P lasers for the 1.3μm region since these materials promise improved performance at elevated temperatures [e.g. Ref. 1]. Modulators have also been reported in InAsP/InP showing exciton linewidths of <16meV at room temperature, despite some relaxation of the 50 period MQWs [2]. So far there has been much less work in the 1.55μm region where the compressive strain in the InAsP well reaches 2%. However, strain compensation using InGaP barriers has been shown to be effective in allowing MOVPE growth of 50 periods of InAsP/InGaP with an exciton feature at 1.55μm [3]. Here we report a study of two MQWs with wells of nominal composition $InAs_{0.55}P_{0.45}$ and barriers of InP and $In_{0.95}Ga_{0.5}P$ respectively; we examine the prospects of using such structures for 1.55μm modulators.

II. Growth and structural characterization

Two 5 period MQWs were grown by solid-source MBE at a temperature of 480°C; the active region was incorporated into a pin diode structure with a nominal ~0.5μm total intrinsic region. (004) and (115) X-ray diffraction spectra showed the active regions to contain respectively: $InAs_{0.51}P_{0.49}/InP$ 51nm barriers/8.8nm wells (M1216) and $InAs_{0.54}P_{0.46}/InP/InGa_{0.02}P_{0.98}/InP$ 50nm barriers/8.5nm wells (M1217). M1216 has ~1.6%

strain in the wells and 0.24% net strain in the MQW while M1217 is partially strain-compensated with ~1.8% strain in the wells and -0.15% strain in the barriers giving a net compressive strain of 0.13%. Simulated X-ray spectra gave excellent agreement with the measured data as shown in Figure 1, indicating uniform periodicity and abrupt interfaces. There was no evidence of strain relaxation in either sample, although the critical thickness, estimated using Matthews and Blakeslee's model [4], for a single well with 1.8% strain is only 5.5nm. Our previous findings suggest that providing the individual quantum well layers are not relaxed it does not substantially degrade the modulator properties if the whole MQW is relaxed with respect to the substrate [2]. This means that the prospects for growing MQW modulators in InAsP/InP at 1.55μm are much better than might be expected from critical thickness predictions alone.

Capacitance-voltage measurements indicated the thickness of the intrinsic regions to be 0.35μm and 0.25μm for M1216 and M1217 respectively indicating some dopant diffusion into the InP cladding layers on either side of the wells.
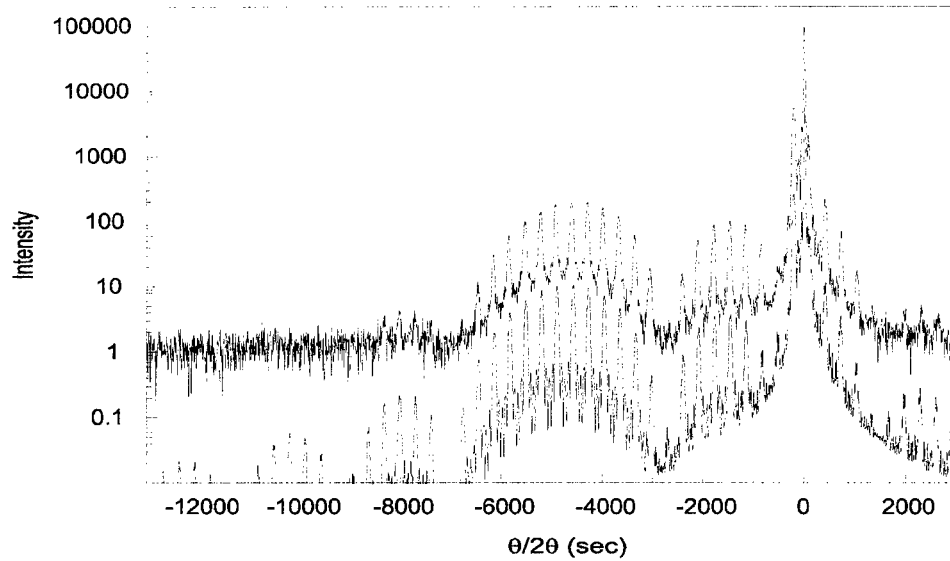
Figure 1: X-ray diffraction spectrum for M1216 (top) and simulated spectrum

III Modelling

Using a three-band k.p model in the envelope function approximation we have calculated the n=1, e1-hh1 transition energies for $InAs_xP_{(1-x)}$/InP as a function of well composition. Strain is taken into account via the deformation potentials and exciton binding energies are included[5]. The results are shown in Figure 2 for the 1.55µm region along with the measured exciton positions for M1216 and M1217.

IV Optical characterisation

Photoluminescence spectra showed room temperature transitions at 1485nm [M1216] and 1530nm [M1217] with linewidths [FWHM] of 20meV and 14-18meV respectively; the 10K linewidths were ~5meV for both devices.

Photocurrent spectra from these samples are shown in Figure 3. Both samples exhibit narrow excitonic features (HWHM ~ 10meV for M1216 and ~6meV for M1217) and a strong Stark shift with applied bias (~6nm/V from 2-6V). The sharper exciton in M1217 is probably due to the higher barriers in the conduction band for this sample. This increase in barrier height with InGaP may prove as useful as the strain-balancing effect it has in relation to InAsP.

The differential photocurrent is shown in Figure 3. It can be seen that the maximum modulation in the normally-on position (above the band edge) is achieved at 4V for M1217 and 4-6V for M1216 corresponding to an operating field of ~150kV/cm or 15V across a 1µm modulator. This is a much lower field than is required for maximum modulation in InGaAs/InP at the same wavelength [6,7]. Similar results were observed in the
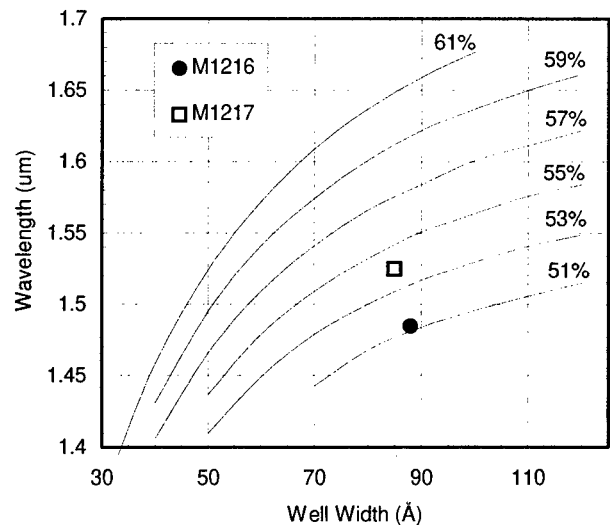
Figure 2. Transition energies as a function of composition for n=1, e1->hh1 in InAsP/InP system

441
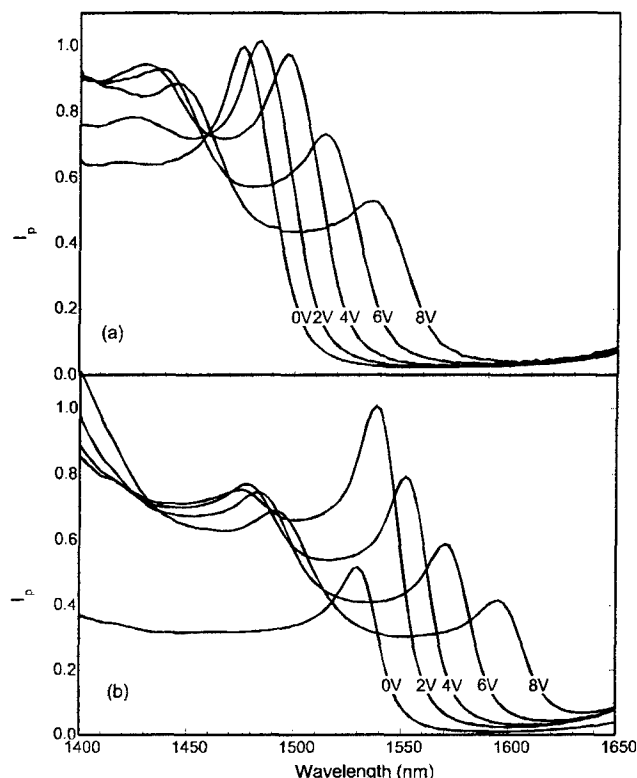
Figure 3 Photocurrent as a function of wavelength for (a) M1216 and (b) M1217.

40V applied bias [6,7]. It may be possible to improve still further on these properties since increasing the gallium composition in the barrier should enhance the exciton oscillator strength. Transmission modulators with 20-50 wells are now being grown with strain-compensated barriers and the incorporation of such devices into reflection modulators is being investigated.

V Summary

In summary, it has proved possible to grow InAsP/In[Ga]P MQWs with exciton features above 1.5µm without strain relaxation occurring. The well critical thickness exceeds the value predicted by the Matthews and Blakeslee model by about 50%. Modulation via the quantum confined Stark shift occurs at much lower fields than in the InGaAs/InP system where narrower wells must be used to reach 1.55 µm. We predict that it should be possible to achieve a contrast ratio of ~2.3 dB at < 20V for a 1.55 µm transmission modulator of 1 µm active region in InAsP/InGaP.

observed in the 1.3µm region [8]; this effect is largely due to the wider wells that can be used in the InAsP system at these wavelengths, although the smaller valence band offset may also play a role.

Absorption measurements at zero bias on sample M1216 indicated an absorption coefficient at the exciton peak due to the active region of $21000cm^{-1}$. Using this value and the measured intrinsic region thickness we can predict the performance of a thicker modulator (say 50 periods of 8.5nm /11.5nm giving a 1µm intrinsic region). Although in the case of M1216 increasing the number of wells and decreasing the barrier thickness will lead to relaxation, for the strain-balanced structure, M1217, increasing the well-barrier ratio would cause only a small increase in net strain in the sample. This could be offset by a higher gallium content so no relaxation would be expected and hence no exciton broadening. A 50 period version of M1217 with an absorption coefficient and doping level similar to M1216 would give a contrast ratio of 2.3dB (modulation depth = -1.78dB) at the exciton for a modulation voltage of about 18V. This compares favorably with InGaAs/InP devices where similar performance in a transmission modulator requires 30-

Figure 4. Differential photocurrent as a function of wavelength (subtracting 0V photocurrent) for (a) M1216 and (b) M1217.

442

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GROWTH OF Tl-CONTAINING III-V MATERIALS BY GAS-SOURCE MOLECULAR BEAM EPITAXY

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Introduction

The synthesis of the Tl-V binaries and In-Tl-V alloys have been investigated using gas-source molecular beam epitaxy. With this approach, neither the binary nor ternary Tl-containing phosphides could be attained, with virtually all of the Tl present in the form of metallic droplets. While the Tl-As system was found to produce a compound, this phase was Tl rich with a Tl/As ratio ranging between 6/1 to 9/1. This phase was always accompanied by metallic Tl which oxidized rapidly upon exposure to air. Zinc blende InTlAs was synthesized, as determined by Auger electron spectroscopy, but exhibited compositional variations believed to be due to severe Tl surface segregation. The formation of both the Tl-As and In-Tl-As phases was found to be strongly dependent upon growth temperature. The Tl-Sb system also produced a Tl rich phase, with a composition of Sb_2Tl_7, as measured by electron microprobe analysis. Unlike the arsenides and phosphides, the Tl-Sb compound could be synthesized even at growth temperatures of 375°C. This phase was found to exist in a CsCl structure and was accompanied by metallic Sb rather than elemental Tl as for the arsenides.

I. Background

InTlP, InTlAs and InTlSb have been proposed as potential IR materials[1,2]. In addition to the desirable bandgaps which have been predicted for these alloys, (1.35 eV to -0.27 eV for X_{Tl} of 0 - 1 in InTlP for example), the lattice constants are expected to differ from those of InP, InAs or InSb by less than 2%, thus allowing the use of III-V substrates. For the case of InTlP, this would also allow integration with already existing InP electronics technology. Preliminary reports of InTlSb growth have been encouraging [3-6]. Razeghi et. al.[3,5] have reported InTlSb with a cutoff wavelength of up to 9.0 m with a small lattice mismatch to InSb or -1.3%. While there have been no reports of Tl-containing arsenides, Asahi et. al. [7] have reported synthesis of stoichiometric TlP and InTlP using gas-source molecular beam epitaxy (GSMBE) as determined by x-ray diffraction analysis. Curiously they did not observe a shift in the PL spectra. By contrast, Razeghi et. al. [3] obtained a phosphorus rich phase with the stoichiometry of $(InP)_{1-x}-(TlP_3)_x$ which has a cutoff

of 8.0 μm. No other studies of stoichiometric TlP synthesis have been reported. This paper will discuss the feasibility of and the conditions necessary for production of homogeneous In-Tl-containing alloys as well as the composition and structure of the Tl-V binaries.

II. Experimental Procedure

This study was performed using elemental Group III sources in conjunction with catalytically decomposed PH_3 or AsH_3 or elemental Sb in a Varian gas-source Gen II molecular beam epitaxy system. Typical cell temperatures were 550°C, 900°C and 405°C for the Tl, In and Sb ovens respectively. Typical hydride flows were 20 sccm. Quarters of 2-inch diameter semi-insulating GaAs or Fe doped InP substrates were In mounted to Si backing wafers which were then mounted in In-free holders. Growth temperatures were measured using the substrate thermocouple (TC). Comparison of the temperature as measured by the substrate TC with the melting point of InSb showed only a 5°C discrepancy, with the substrate TC reading slightly higher than the actual temperature. Samples were

characterized using powder x-ray diffraction (XRD) to determine crystal structure, scanning electron microscopy (SEM) to evaluate surface morphology, and electron microprobe analysis (EMPA) or Auger electron spectroscopy (AES) to determine composition. While EMPA samples a large and deep (~1μm) area, the AES beam size can be focused to sample the surface of a smaller area. Combined with sputtering, this allows for a spatially precise determination of the composition.

III. Tl-V Binaries

A variety of substrate temperatures ranging from 325°-525°C as well as several Tl fluxes were investigated for synthesis of the Tl-containing binaries. For temperatures above 350°C, the Tl sticking coefficient decreased rapidly with increasing temperature. At 425°C, there was virtually no deposition of Tl. This is in good agreement with the dependence of Tl vapor pressure on temperature, which shows the Tl vapor pressure to be ~ 10^{-7} Torr at 320°C [8]. This suggests that low temperatures will be required for efficient growth of these materials. For both TlP and TlAs, metallic Tl was found to be the dominant phase for growth temperatures above ~300°C, with no evidence in EMPA or XRD of the formation of any Tl-V phase. This Tl reacts rapidly with oxygen to form crystallites of TlO_x which appear to grow out of the surface. If left in air for a long enough period of time, the oxide reaches a stoichiometry of Tl_2O, indicative of a monovalent Tl state. By reducing the temperature to 225-275°C, an As containing Tl phase was obtained, but at a Tl/V ratio ranging from 6/1 to 9/1. While this phase also oxidizes in air, the oxidation rate appears to be slowed substantially by the presence of the As. Calculations using the SRI model indicate that the difficulty in forming the P and As containing binaries is due to high equilibrium group V vapor pressures for these compounds [9].

By contrast to the arsenides and phosphides, the Tl-Sb compounds are predicted to have significantly lower Group V vapor pressures. Thus it is not surprising that Tl was found to react much more readily with antimony allowing a Tl-Sb phase to be obtained at much higher temperatures (400°C). No evidence of Tl metal can be observed

by either EMPA or XRD. The deposited material is found to be a combination of Sb_2Tl_7 and elemental Sb, with the Sb_2Tl_7 taking the form of a shell around the Sb droplet, as shown in Figure 1. The identification of these two phases has been confirmed with powder x-ray diffraction (XRD), which shows the Sb_2Tl_7 to have a complicated (i.e.
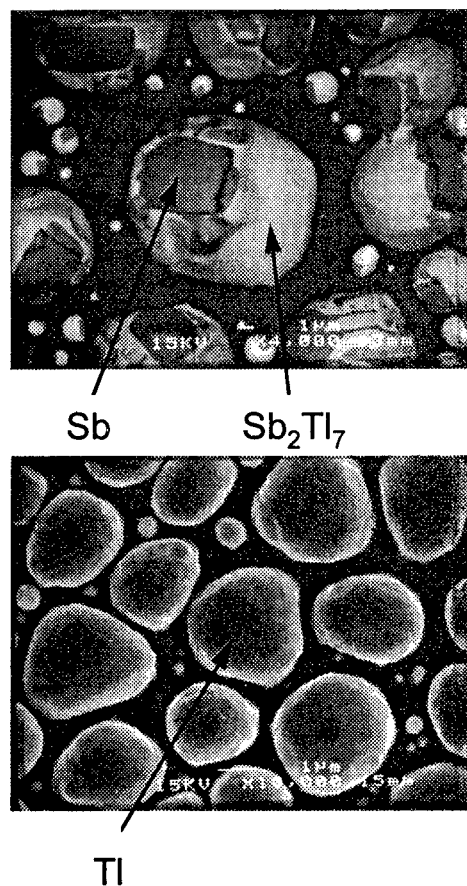
Fig. 1 Top: SEM micrograph (4000X) of GaAs surface on which TlSb has been attempted. Along with Sb droplets, a Tl rich phase (Sb₂Tl₇) was obtained. For comparison, the Tl droplet structure obtained when attempting to grow TlAs on InP at 375°C is shown at bottom (10,000X).

multi-atom/lattice point) CsCl type of structure [10].

IV. In-Tl-V Alloys

Attempts to grow InTlP or InTlAs at $T_g >$ 300°C resulted in similar morphologies as obtained for binary growth, as shown in Fig. 2. The observed phases are Tl droplets in an InAs or InP matrix. AES indicates a matrix Tl concentration of only 1 - 2%, which is the background detection limit for this

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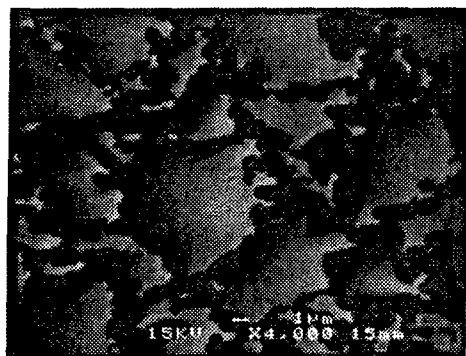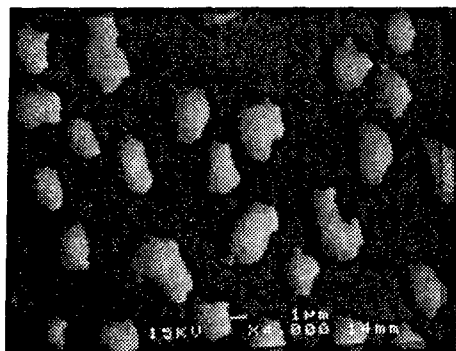
Fig. 2 SEM micrograph of surface of layer obtained when growth of InTlAs is attempted at 375°C using two different Tl fluxes: Top: T_{Tl} = 510°C, Bottom: T_{Tl} = 565°C. (4,000X).

technique. Increasing the Tl flux increased the size of the Tl pools, but did not increase the background Tl concentration. Increasing the growth temperature to 400° or above eliminates the Tl from the surface via desorption. Thus high temperatures were not useful in forming the ternary alloy.

Because of its vapor pressure, the excess Tl can be removed by in-situ annealing (Fig. 3). It was
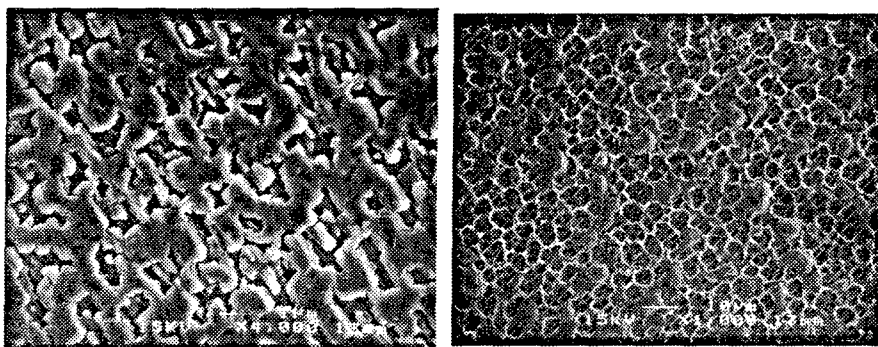
hoped that material trapped directly beneath the Tl pools might contain a higher concentration of Tl than material near the surface. However, AES of the regions previously underlying the Tl pools shows that little or no Tl incorporates in this base material. Similarly, capping of the droplets with InP was also unsuccessful, leaving Tl droplets on the surface even after 1000Å of InP was deposited. This suggests that Tl tends to surface segregate with the Tl droplets floating atop the growth interface.

By contrast to the phosphide, capping of the Tl droplets with InAs has been successful in forming a phase containing In, Tl and As (Figure 4); however, the resulting Tl profile obtained by AES is characteristic of systems which experience severe surface segregation. The near surface region is Tl-rich with some evidence of the oxidation characteristic of Tl metal. The Tl profile then tails away from the surface as the In profile increases, suggesting that an alloy with a continuously varying composition has been formed.

While this is encouraging in that it is the first apparent synthesis of InTlAs, single phase alloys with constant compositions are needed to correlate material properties with composition. Typically segregation is overcome by reducing the growth temperature. In this case, lowering the temperature to 275°C does change the observed phases. In addition to Tl droplets, which oxidize rapidly into small crystallites, islands with significantly reduced oxidation are obtained as well (Fig. 5). The AES Tl profiles in these regions are much flatter than those in films grown at 375°C, and the thickness of the Tl-rich near surface region has been reduced. This provides further evidence that segregation is responsible for much of the growth behavior observed in this study.

V. Summary

Using GSMBE it was not possible to synthesize the Tl-containing phosphides or a stoichiometric Tl-As phase. This is believed to be due the high Group V overpressures predicted for this system by the LDA

Fig. 3 Left, SEM micrograph of In-Tl-As sample grown in the same manner as that depicted at right in Fig. 2 after annealing for 10 min. at 425°C (4,000X). Right: was grown and annealed in a similar fashion using PH₃ instead of AsH₃ in an attempt to grow InTlP (1,000X).

446

calculations at SRI. While alloying with In to form In-Tl-V compounds should lower the necessary Group V flux substantially, it was also found that the Tl surface segregates, making incorporation in the III-V matrix difficult. By using low growth temperatures (<300°C), it was possible to synthesize an InTlAs compound which appears to have the proper stoichiometry. Growth in the Tl-Sb system appears to occur much more readily. The binary material obtained in this case has a formula of Sb_2Tl_7 and a CsCl type of crystal structure.

Fig. 4 SEM micrographs of samples prepared as described in Fig. 3. The sample at right was capped with InAs for 10 min. at 375°C prior to removal from the growth chamber. (4,000X).

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InAs   InTlAs   Tl/TlO$_x$

Fig. 5. Top: SEM of sample surface obtained when InTlAs growth is attempted at 275°C (4,000X). Bottom, AES profile of InTlAs showing a flat Tl profile. Analysis of the background matrix showed InAs while the droplets covered with small crystallites were a mixture of Tl and TlO_x.

Gas source MBE growth of TlInGaP and TlInGaAs as new materials for long-wavelength applications

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1. Introduction

Recently, we have proposed III-V compound semiconductors $Tl_xIn_{1-x-y}Ga_yP$ (Thallium Indium Gallium Phosphide) lattice-matched to InP as new materials for long-wavelength applications, especially for laser diodes (LDs) [1]. This material system can cover the wavelength range from 0.9 μm to over 10 μm and is suitable for the 1 μm range LDs for optical fiber communication and mid-infrared (longer than 2 μm) LDs.

The estimated band gap energy variation with alloy composition is shown in Fig.1. TlInGaP is the alloy consisting of semiconductor InGaP and semimetal TlP. For the heterostructures of this alloy system, the type-I band lineup having a wider conduction band discontinuity than that of valence band is expected. This characteristics is very suitable for the optical devices. Furthermore, the semiconductors whose band gap does not change with ambient temperature are expected because of the alloy of semiconductor and semimetal like $Hg_{0.4}Cd_{0.6}Te$. This characteristics is very promising to fabricate semiconductor lasers whose wavelength is insensitive to ambient temperature variation, which is very important for the advance in WDM (wavelength division multiplexing) optical fiber communication, because one problem in using InGaAsP/InP LDs in WDM system is that the lasing wavelength fluctuates with ambient temperature variation due to the temperature dependence of band gap energy. TlInGaP can be also lattice-matched to GaAs, covering wavelengths from 0.65 μm to about 1.24 μm (TlGaP).

Another new III-V semiconductor system is $Tl_xIn_{1-x-y}Ga_yAs$ (Thallium Indium Gallium Arsenide) [2] as shown in Fig.1. This alloy system can be lattice-matched to InP and InAs, and can be used for the optical devices in the wavelength range of 2 μm to over 10 μm. Two types of heterostructures are considered; TlInGaAs/InP and TlInGaAs/InGaAlAs. The advantage of the second type of heterostructure is that it includes only one group V element. The primary reason why the TlInGaAs alloy system might be of interest over TlInGaP is
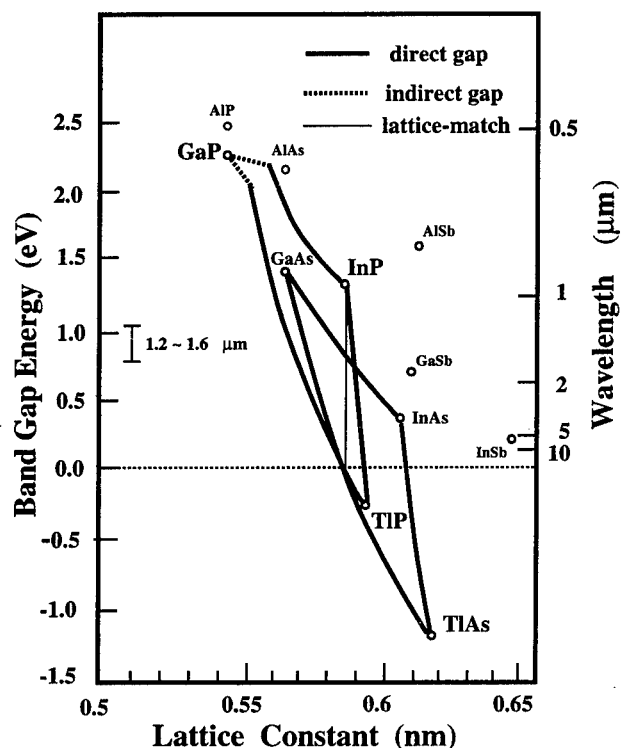
Fig.1 Band gap energy versus lattice constant for TlInGaP and TlInGaAs. Compositions for the lattice-matching to InP and GaAs are indicated by vertical solid line and vertical dashed line, respectively.

that the same band gap energy can be obtained even for the use of smaller Tl composition. Thus it might be favorable from the view point of toxicity of Tl.

In this paper, we report the growth characteristics of these Tl-based semiconductor material system by using gas source molecular beam epitaxy (MBE) on InP, GaAs and InAs substrates. Preliminary results on optical and electrical properties are also described.

2. Growth condition

The growth was conducted in a gas source MBE system. Elemental Tl (5N), In (7N) and Ga (7N) and thermally cracked PH_3 and AsH_3 were used as group III and group V sources, respectively. The substrates used were Fe-doped (100) InP, Cr-doped (100) GaAs and S-doped(100) InAs. PH_3 flow rate was 0.5-1.5 SCCM and AsH_3 flow rate was 1.2-1.5 SCCM. The toxicity of Tl is known to be higher than that of As, so that extreme care during treatment must be taken. Tl or Tl contaminated surfaces should not be touched with bare hand and Tl flakes or vapors should not be inhaled: lethal intake is documented to be at 600 mg. It is known that the hand surface suffers ulcer when Tl is touched with bare hand.

3. Results and discussion
3.1 TlInGaP grown on InP

After the growth of 0.1 μm-thick InP buffer layer, TlP binary, TlInP ternary and TlInGaP quaternary layers were grown (thickness: about 0.5 μm). RHEED patterns revealed (2x4) reconstruction at substrate temperatures of 400-450 °C showing phosphorus-stabilized surfaces. The surface exhibited mirror-like. During the growth of TlInP, RHEED intensity oscillation was observed indicating layer-by-layer growth. At lower temperatures RHEED pattern showed phosphorus-excess (2x2) reconstruction. TlInP grown under phosphorus-excess condition showed rough surface [3].
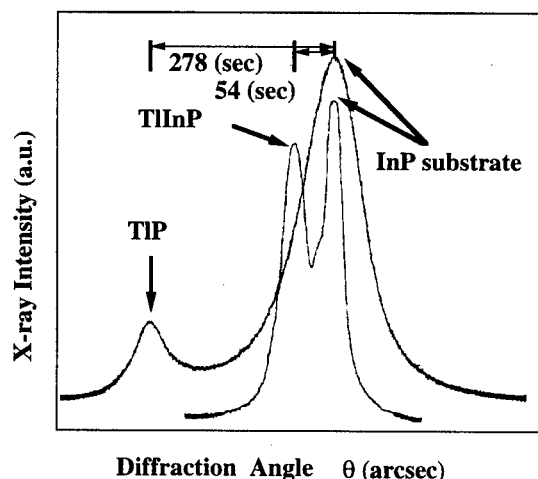
Fig.2 Double crystal X-ray diffraction rocking curves for TlP/InP and TlInP/InP.

Double crystal (monochromatic) X-ray diffraction rocking curves for TlP/InP and TlInP/InP samples confirmed the successful growth of TlP and TlInP as shown in Fig.2. The alloy composition of TlInP was found to vary with Tl flux [3]. Therefore, it was shown that the entire range of TlInP can be grown by gas-source MBE.

PL emission was detected at 77K for the TlInP layers with low Tl composition. Hall measurement on TlInP showed an n-type conduction with an electron concentration of 6.3×10^{15} (3.9×10^{15}) cm^{-3} and an electron mobility of 2,500 (22,000) cm^2/V.s at room temperature (77K) for TlInP with a Tl composition of 5%.

Temperature variation of band gap energy was characterized by measuring photocurrent versus wavelength curves as a function of temperature as shown in Fig.3. Temperature variation of band gap energy for TlInP (Tl composition = 0.09) was slower than that of GaAs, InP and InAs. Note that the band gap energy of TlInP in Fig.3 is much larger than that of InAs. This result suggests the existence of temperature-independent band gap energy for TlInP with larger Tl composition.

Quaternary TlInGaP layers were also successfully grown on InP [4]. In the double crystal X-ray diffraction measurements, the

449

No phase separation was also observed. This result indicates that the TlInGaP alloy on InP substrate is promising from the viewpoint of crystal growth. We have observed the PL only from the TlInGaP with a composition close to InP at present.
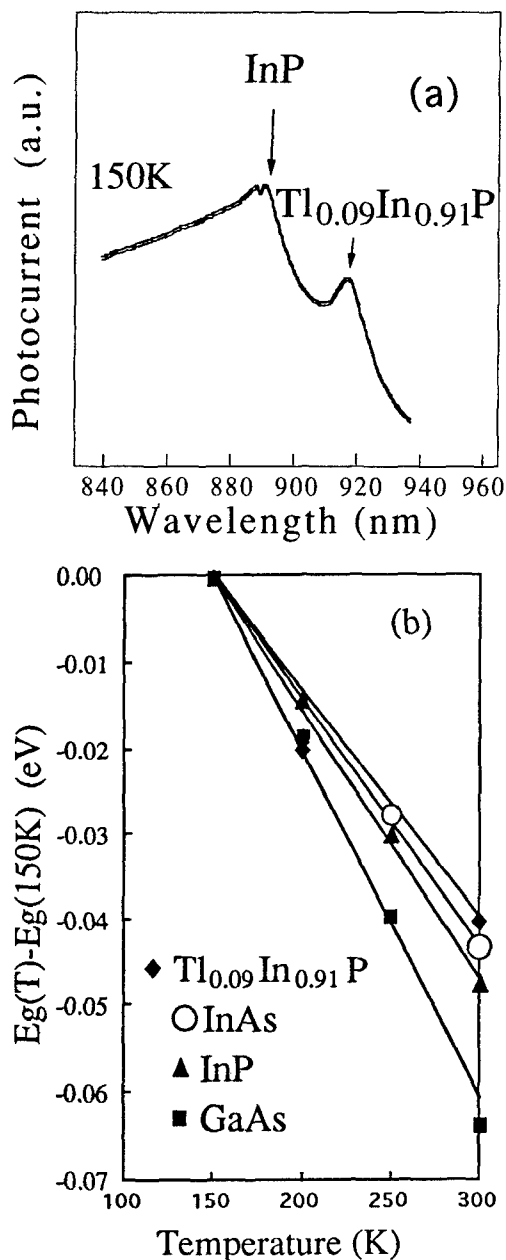
Fig.3 (a) Photocurrent versus wavelength curves for the TlInP/InP as a function of temperature. (b) Temperature variation of band gap energy for TlInP as well as GaAs, InP and InAs. Band gap energies for TlInP were obtained from the photocurrent curves.

shifts to the lower (higher) diffraction angle for the TlInGaP peak with increasing Tl (Ga) flux were observed. These shifts agree with the increase of Tl (Ga) mole fraction. Reduction of full width at half maximum (FWHM) was also observed by decreasing the degree of lattice-mismatch for TlInGaP.

450

Fig.4 (a) Double crystal (monochromatic) X-ray diffraction rocking curve for TlGaP on GaAs around the angle of GaAs. (b) Unmonochromatic X-ray diffraction rocking curves for TlGaP grown as a function of Ga flux.

3.2 TlGaP on GaAs

TlGaP layers (thickness: about 0.5 μm) were grown on GaAs substrates after the growth of GaAs buffer layer. Fig.4(a) shows double crystal X-ray diffraction rocking curve from TlGaP/GaAs, indicating that the nearly lattice-matched TlGaP was grown here. However, as shown in fig.4(b), we observed the phase separation into nearly lattice-matched TlGaP and TlP-like TlGaP or GaP-like TlGaP depending on the flux ratio of Tl and Ga. This observation for TlGaP differs from that for TlInP. This difference seems to be originated from the lattice constant difference in TlP-InP and TlP-GaP. It is noteworthy that there are three stable points (compositions) in this alloy system. This result suggests the possibility of the growth of non-phase-separated lattice-matched TlGaP by adjusting the Tl and Ga fluxes. In the TlGaP layers, we observed the increase of photocurrent in the longer wavelength region and slower temperature variation of band gap energy like TlInP on InP.

3.3 TlInAs on InAs

TlInAs layers were grown on (100) InAs. RHEED showed (2x4) reconstruction and the observation of RHEED intensity oscillations during growth of InAs and TlInAs confirmed the layer-by layer growth. Double crystal (monochromatic) X-ray diffraction and unmonochromatic X-ray diffraction rocking curves for TlInAs/InAs showed the successful growth of TlInAs and no phase separation.

4. Summary

We have, for the first time, studied the growth of new semiconductor TlInGaP and TlInGaAs by gas source MBE. Grown layers exhibited (2x4) surface reconstruction. X-ray diffraction measurements showed the successful growth of TlInP, TlGaP, TlInGaP and TlInAs. No phase separation was observed in TlInP and TlInGaP grown on InP substrate and TlInAs on InAs, while the phase separation was observed in TlGaP grown on GaAs. PL emission was observed for TlInP and TlInGaP grown on InP, though composition was close to InP. The layers showed n-type conduction with an electron concentration of 6.3×10^{15} (3.9×10^{15}) cm^{-3} and an electron mobility of 2,500 (22,000) cm^2/V.s at room temperature (77K) for TlInP with a Tl composition of 5%. Photocurrent versus wavelength measurements showed that the decrease of the band gap energy by the addition of Tl and that their temperature variation is smaller than that of InAs, indicating the possibility of temperature-independent band gap energy in these alloy semiconductors, though not confirmed experimentally yet. It is also demonstrated that the gas source MBE is a promising method for the growth of TlInGaP and TlInGaAs.

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MBE GROWN DISLOCATION-FREE ANTIMONIDES ON GaAs TuE3 COMPLIANT UNIVERSAL SUBSTRATES

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Introduction

In this work, we demonstrate the growth of a 6500Å, dislocation-free, InSb layer (~14.7% compressively lattice mismatched to GaAs) on a compliant universal (CU) GaAs substrate. Using a recently proposed [1] technology, twist wafer-bonding, the authors use a new type of III-V substrate on which almost any type of semiconductor may be grown without dislocations. The CU GaAs substrate was formed by wafer-bonding a 30Å GaAs layer to a bulk GaAs crystal with a large angular misalignment inserted about their common (100) direction. Cross-sectional bright-field TEM images of the InSb show no dislocations in all of the observed areas (~2.6μm wide in one contiguous region). Electron diffraction measurements made of the films showed the twist wafer-bonding technology to be promising for even higher lattice-mismatches.

I. Background

Compliant universal substrates are ideal substrates that can accommodate epitaxial overlayers of any lattice constant due to the extraordinarily "flexible lattice" on the substrate's surface. In order to maintain a high "lattice flexibility", a compliant substrate must be no more than a few monolayers thick, and it should be free standing [2-4]. Free-standing monolayer thick substrates are technologically challenging to implement. It was recently discovered [1,5] that a thin layer (of only a few monolayers) that is wafer-bonded to a bulk crystal with a large deliberate angular misalignment between their <011> closely approximates an ideal compliant substrate in its lattice flexibility. These CU substrates also possess the robustness and uniformity required of a practical substrate. In this work, we report on the high-quality growth of InSb on GaAs CU substrates and on conventional GaAs substrates. We chose InSb for its importance in mid-infrared detection applications. It also has the highest electron and hole mobility among all known semiconductors. More importantly, it possesses the largest lattice mismatch (14.7%) to GaAs among all semiconductors except the nitride compounds.

The process of forming a CU substrate is summarized in Fig. 1. A 1μm AlAs etch stop layer was first grown by Organo-Metallic Vapor Phase Epitaxy (OMVPE) on a conventional GaAs substrate, followed by a thin (30-100Å) GaAs epitaxial layer. The wafer was then wafer-bonded to another GaAs substrate. The wafer bonding procedure was performed at 550°C. During bonding, mechanical pressure of about 1 to 10 MPa was applied to the
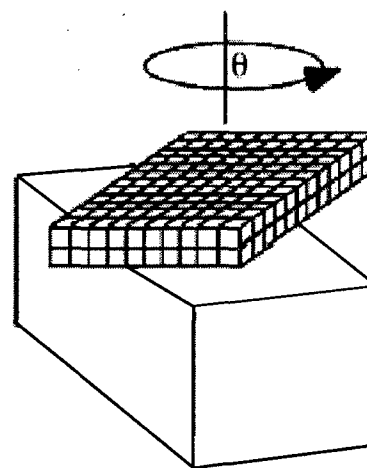
Fig. 1. A 30Å GaAs film that is 45° twist-bonded to a GaAs bulk substrate to form a Compliant Universal substrate.

wafers under the flow of hydrogen to prevent oxidation. The details of the bonding process has been elaborated upon in the literature [6,7]. In forming the CU substrate, a large (10° to 45°) angular misalignment was deliberately inserted about the common (100) direction of the two GaAs wafers, thus forming a high-angle twist boundary at the bonding interface. This high-angle twist boundary is believed to play a critical role in the compliance of the resulting substrate.

After wafer bonding, the GaAs substrate and the AlAs etch stop layer were chemically removed, leaving a thin (30-

100Å) epilayer twist-bonded to a new GaAs host substrate. Highly mismatched heteroepitaxial overlayers are then grown directly on the thin twist-bonded layer. In actual experiments, the AlAs etch stop layer is kept on top of the twist-bonded layer until just before loading the substrate into the growth chamber.
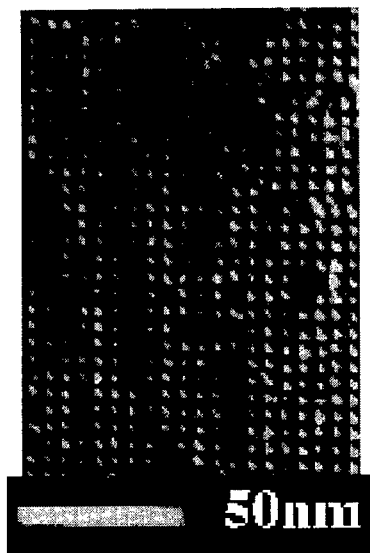
Fig. 2. A Plan-view TEM of the interface between the twist-bonded GaAs film and that bulk GaAs substrate.

Figure 2 shows a plane-view weak-beam bright-field transmission electron micrograph of the interface between the twisted 30Å GaAs film and the underlying GaAs substrate. For illustrative purposes, a small twist angle of about 4° was used. Larger angles (required for strong lattice compliance) would have produced screw-dislocations too closely coupled to be imaged meaningfully. Contained in the image is an array of vertical and horizontal white lines that are characteristic of screw-dislocations in a bright-field image [8]. The spacing measured between the screw dislocation lines uniformly obeys Frank's rule [9] which states that the Burger's vector of the dislocation is equivalent to the cross-product of the spacing between the two parallel dislocations and the twist angle vector. A spacing of about 50Å was measured between the parallel dislocation lines. At larger angles, a regime is reached where the screw-dislocations are totally coupled and the 30Å of GaAs is essentially relieved of almost any stress [9].

II. Experiment

In the experiment reported here, the thickness of the GaAs film chosen for twist-bonding was set at 30Å. After twist-bonding, solvent and acid wafer cleaning, and oxide desorption in the molecular beam epitaxy (MBE) chamber, the remaining 30Å GaAs layer was estimated to have been reduced to about 10-15Å. An angle of about 40° ± 5° was used as the twist angle between the compliant layer and the bulk wafer. A 6500Å film of InSb was then grown simultaneously on both a

GaAs CU substrate and a conventional GaAs substrate by MBE. Cross sectional bright-field transmission electron microscopy (TEM) was used to study the quality of the InSb heteroepitaxy. A dislocation density as high as $10^{11} cm^{-2}$ was observed in the InSb film grown on the conventional (100)
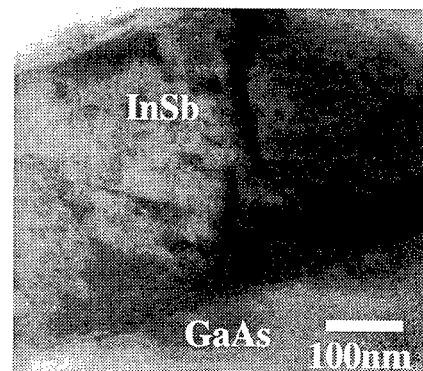
Fig 3a. A bright-field TEM of InSb grown directly on a conventional GaAs substrate. Note the high density of dislocations present in the film.
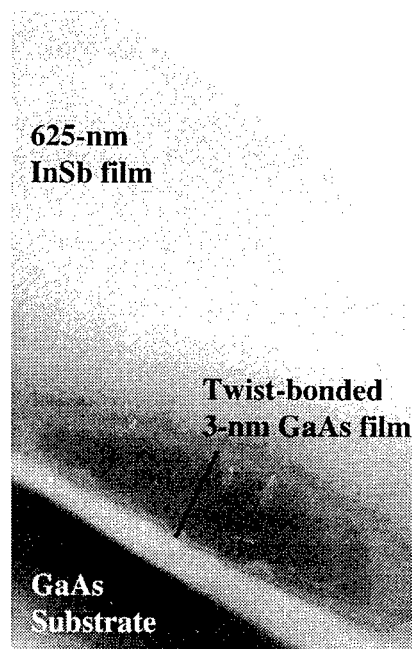
Fig 3b. A bright-field TEM of InSb grown directly on a CU GaAs substrate. Note the lack of threading dislocations and stacking faults in the film.

GaAs substrate (Fig. 3(a)). However, not a single dislocation was observed in the InSb film grown on the twist-bonded GaAs CU substrate (Fig. 3(b)). This result infers that the

453

dislocation density of an InSb crystal grown on a GaAs CU substrate is at most $10^6 cm^{-2}$ in regions within 100 nm from the heteroepitaxial interface. One may also infer that the dislocation density in the InSb layer further away from the growth interface will be even smaller. Although the twist-bonded GaAs layer was too thin (< 30Å) to be clearly resolved in the bright-field cross sectional TEM images shown, its existence was confirmed from electron diffraction patterns obtained from the InSb film and bulk GaAs crystals on both sides of the twist-bonded thin layer. Electron diffraction patterns (DP) were taken of the cross-sectional sample during the TEM examination. The DPs were taken such that the sample was aligned to the <110> direction of the GaAs bulk substrate thereby producing an off-axis InSb overlayer. The DP taken from the GaAs <110> crystal produced a pattern that matched a recognized stereographic pattern. However, the DP taken from the overlayer showed a pattern starkly different from the <110> pattern. Had the twist-bonded layer not been present, the two diffraction patterns would have exhibited identical geometric profiles with one crystal having a different spot-spot separation from the other, reflecting the difference in lattice constants. Because there is a twist-bonded layer between the InSb film and the GaAs bulk crystal, the InSb epilayer will take on the crystallographic orientation of the twist-bonded GaAs layer. This change in angular orientation is reflected in the difference in diffraction patterns between the <110> pattern observed for the bulk substrate, and the off <110> pattern observed for the InSb film. The difference in diffraction patterns shown in the image confirms the existence of a twist-bonded thin GaAs layer between the InSb growth and the GaAs bulk substrate.

III. Conclusion

In summary, we have, for the first time, demonstrated defect-free InSb (14.7% lattice-mismatched to GaAs) heteroepitaxy grown on GaAs CU substrates. The GaAs CU substrates were formed by bonding a thin GaAs layer (about 30Å) to a GaAs bulk crystal with a large angular misalignment. The results obtained here suggests that the CU substrate may serve the optoelectronics and electronics communities well as a generic, robust lattice-compliant substrate made out of any semiconductor material including GaAs and Si.

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SUBSTRATE ENGINEERING OF 1.55 μm LASERS

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Introduction

Lasers grown on InP suffer from a lot of disadvantages compared to those grown on GaAs: the price of the substrate, the high temperature sensitivity of the 1.55 μm lasers and the limitations imposed by the miscibility gap of the InGaAsP system on the design of the active regions. We propose the use of substrate engineering (in this case the growth on $In_{1-x}Ga_xP$) to solve these problems. It was recently demonstrated [1] that a thin crystal layer bonded on a bulk crystal of the same nature with a high enough angular misalignment can be used as a compliant universal substrate. When the screw dislocation array at the interface is dense enough (misalignment angle higher than about 15°) the stress introduced by an epitaxial layer on the thin film can be released at that highly dislocated interface. This concept makes it possible to create new substrates when no ideal crystal is available. In the case of the 1.55 μm lasers it is now possible to imagine a new substrate to get rid of many of the problems of the InP substrate. The structure we propose consists of growing the 1.55 μm active regions on an $In_{1-x}Ga_xP$ substrate created on a compliant universal substrate with x equal to about 0.1. For $x = 0.1$, the band gap energy of $In_{1-x}Ga_xP$ is 1.43 eV, i.e. 80 meV higher than that of InP. Most of this energy difference increases the energy of the conduction band edge. Moreover we demonstrate that it is possible to grow strained compensated quantum wells (QW) active regions emitting at 1.55 μm on that type of substrate using only InGaAs alloys.

I. Theoretical

We used the Van de Walle's model-solid theory [2] to calculate the conduction band offset in the InGaAsP system. However, the accuracy of the conduction band offsets calculated using this model are largely limited by the uncertainty on the relative position of the valence band edge of the binary materials and on the contribution of the conduction band shift to the pressure induced change of the gap. So, we fitted these eight parameters (two parameters for each binary compound) using a set of 10 selected conduction band offset values in the InGaAsP system [3,4,5].

According to these calculations the conduction band edge of un-strained $In_{0.9}Ga_{0.1}P$ is 86 meV above that of un-strained InP. So the achievable conduction band offsets on that type of substrate are potentially higher than those one can get on InP. This is one of the key elements that can help to build 1.55 μm lasers with lower temperature sensitivity and high efficiency at high temperature. Indeed, we already demonstrated that the addition of a thin $In_{0.81}Ga_{0.19}P$ layer in tensile strain on the p side of the SCH of a 1.55 μm laser

improves its above threshold temperature sensitivity T_n [6]. Without that layer, T_n is in the range of 124 K. With that layer it increases to about 164 K. In that case the addition of a thin $In_{0.81}Ga_{0.19}P$ layer in tensile strain increases the conduction band edge energy by about 85 meV at room temperature according to the model-solid theory.

Finally, the growth of a 1.55 μm emitting device on that type of substrate should also be easier than on InP. For the growth of a strain compensated QW structure on $In_{0.9}Ga_{0.1}P$ only $In_{1-y}Ga_yAs$ alloys are needed. This ternary alloy has no miscibility gap at the typical growth temperature used in MOCVD and its composition control is much easier than that of InGaAsP. The QW can be made of $In_{0.58}Ga_{0.42}As$ which is 1% compressive strained to $In_{0.9}Ga_{0.1}P$ and has an emission wave length of 1675 nm. The barriers can be made of $In_{0.28}Ga_{0.72}As$ that is -1 % tensile strained to $In_{0.9}Ga_{0.1}P$ and has a heavy hole wave length emission of 1260 nm. In such a structure the light holes are confined in the barriers like in the case of the constant y InGaAsP structures. It participates to a decrease of the laser current threshold by increasing

the life time of the holes [7]. The calculated conduction band offsets of such a structure are 125 meV between the QW and the barrier and 189 meV between the barrier and $In_{0.9}Ga_{0.1}P$. In an equivalent structure grown on InP with InGaAsP quaternaries, that is to say with the same band gap energies and strains, these values are 116 meV and 109 meV. Whereas the electron confinement energies in the wells are similar, the barrier to substrate conduction band offset increases significantly. This is a key parameter for the improvement of the temperature behavior of long wave length lasers. By changing the Ga content in the substrate around 10 % the parameters of the QW can be adjusted. Fig. 1 shows the wave length of the 1% and -1% strained $In_{1-y}Ga_yAs$ alloys on $In_{1-x}Ga_xP$ (for $0.08 \leq x \leq 0.12$) and the QW thickness necessary to achieve a 1.55 µm emission with these materials.
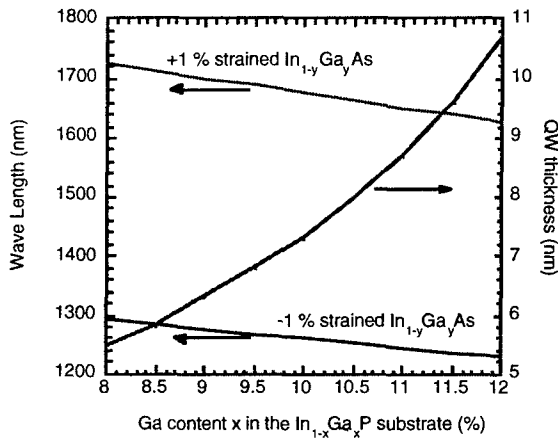
Fig. 1: Wave length of the 1% and -1% strained $In_{1-y}Ga_yAs$ alloys on $In_{1-x}Ga_xP$ as a function of x and thickness of the QW required to get a 1.55 µm emission using the -1 % strained material as the barrier and the 1% strained alloy as the QW. The conduction band offset calculated using the model-solid theory varies linearly from 73.1 to 76.6 % of the band gap energy difference for x varying from 8 and 12 %.

Double fused VCSEL active regions [8] can be grown using only three ternary compositions: the substrate, barrier and QW compositions. For in plane lasers needing a separate confinement heterostructure a lattice matched InGaAsP quaternary can be used for the cladding layers.

II. Experimental

As proposed by Ejeckam et al. [1] the compliant substrate was formed by fusing an InP substrate to an InP substrate on which a 150 nm thick InGaAs stop etch layer and a 10 nm thick InP layer were grown by MOCVD. The fusing process used here is similar to that used for double fused VCSEL [8] except that an angle was introduce between the two substrates. Angles between 13° to 45° were used. To improve the de-coupling between the thin InP layer and the InP substrate the two surfaces were intentionally oxidized before fusing. The substrate used for the growth and the InGaAs layer were then removed by wet etching. The result is an InP substrate with on top of it a 10 nm thick InP layer fused with an angle. The surface was then chemically prepared for the MOCVD growth. The results presented here used a compliant substrate fused at 20°.

The growth on the compliant substrate was performed at 610 °C and 350 Torr in a horizontal reactor made by Thomas Swan using TBP, TBA, TMGa and TMIn. The structure consisted of a 400 nm thick $In_{0.9}Ga_{0.1}P$ layer, three 7.5 nm thick QW's made of $In_{0.58}Ga_{0.42}As$ and four barriers made of $In_{0.28}Ga_{0.72}As$. The first and last barriers are 3 nm thick and the others 6 nm thick. The growth was terminated by 100 nm of $In_{0.9}Ga_{0.1}P$ on top of the QW's. The growth was also performed at the same time on a regular InP substrate for comparison.

III. Results

The (004) X Ray Diffraction (XRD) spectra of the compliant and reference substrates show that on the compliant substrate the $In_{0.9}Ga_{0.1}P$ lattice constant is closer to its equilibrium value (fig. 2). We used (115) asymmetric XRD to determine for both samples the proportion of relaxed strain. On the compliant substrate 40 % of the total misfit strain ε_0 (7100 ppm) is relaxed whereas on the reference substrate only 5 % of the total misfit strain is relaxed.

Neglecting the difference between the elastic coefficients of InP and $In_{0.9}Ga_{0.1}P$ the remaining strain ε_f in the film of thickness h_f for a perfectly independent substrate of thickness h_s should be [9]

$$\varepsilon_f = \varepsilon_0 \, h_s / (h_f + h_s) \qquad (1)$$

That is to say 129 ppm for the layer grown on the compliant substrate. This is much smaller than the actual strain observed in the $In_{0.9}Ga_{0.1}P$ layer (4260 ppm). It means that in this case the coupling between the thick InP substrate and the twist bonded 10 nm InP layer is too strong. The bonds at the interface are not weak enough to allow the in plane lattice parameter of the thin InP layer to comply with that of $In_{0.9}Ga_{0.1}P$. The apparent thickness of the substrate that would theoretically absorb 60 % of the strain, like

456

we observe, can be calculated using (1). It is 808 nm. This is much larger than the critical thickness of $In_{0.9}Ga_{0.1}P$ grown on InP t_c (16 nm) or even than two times t_c. This is the upper limit for the dislocations to be gettered in the thin substrate [10]. So, in the case presented here the substrate effectively helps the overlayer to get closer to its equilibrium lattice constant but nevertheless relaxes by formation of threading dislocations. This explains why for the structure grown on the compliant substrate the XRD peak of $In_{0.9}Ga_{0.1}P$ is broader than on the reference InP substrate and why the satellite peaks due to the periodicity of the QW's are weaker. It should be noted that the calculated apparent thickness of the reference InP substrate is only 10 μm whereas the InP substrate is 380 μm thick. This huge difference may come from the fact that the growth is not done at thermodynamic equilibrium. This delays the relaxation of the layer and thus reduces the apparent substrate thickness.
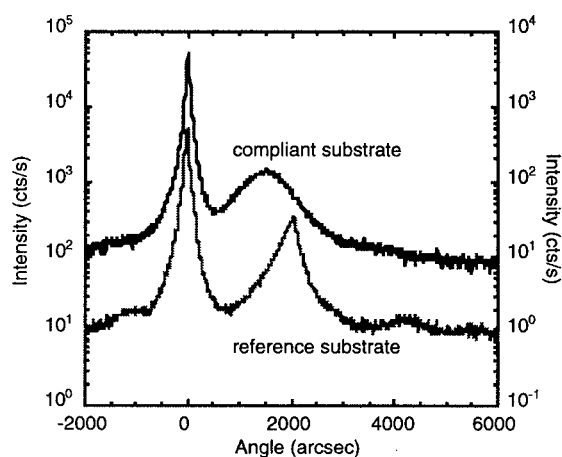
Fig. 2: (004) X ray diffraction spectra of the three QW structure grown on a compliant substrate and on a InP reference substrate.

The photoluminescence (PL) measurements performed on the two substrates are shown in fig. 3. Due to the beginning of relaxation of both samples the PL peaks are broad and their intensity is weak. This degradation of the PL is proportional to the percentage of relaxed strain. However, this should not be the case for a perfect compliant substrate whose apparent thickness is smaller than 2 x t_c.

The PL wave length of the QW's grown on the compliant substrate is 1540 nm whereas a 1550 nm emission wave length was expected for a growth on a perfect compliant substrate. The PL wave length of the QW's grown on the reference InP substrate is 1595

nm. This is close to what we calculated for such a structure grown on InP without relaxation; 1610 nm.
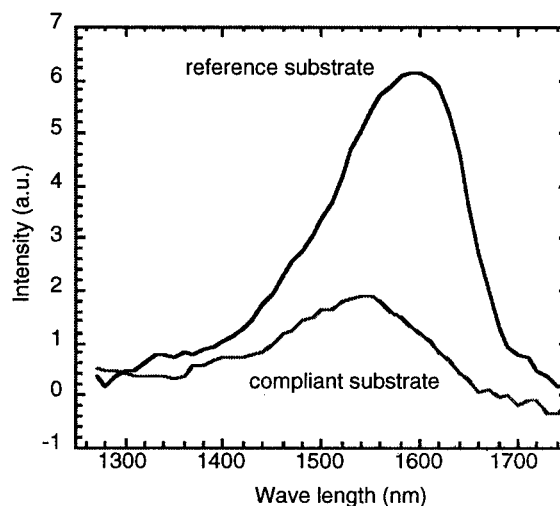
Fig. 3: Room temperature photoluminescence spectra of the three QW structure grown on the compliant substrate and on an InP reference substrate.

Although these PL results are not good enough for a laser application, they demonstrate the validity of the all ternary 1.55 μm laser.

Conclusion

We have shown that the development of compliant substrates open opportunities to improve the properties of long wave length lasers. We propose to grow 1.55 μm emitting lasers on $In_{1-x}Ga_xP$ grown on a compliant substrate with x in the range 8 % to 12 % and using only InGaAs ternary alloys for the strain compensated QW's. It will greatly simplify the growth control and most important should increase the above threshold temperature sensitivity T_η of the laser by increasing the electron confinement in the active region by about 80 meV with respect to a classical structure on InP. Our first experiments used InP compliant substrates because its lattice parameter is close to that of the InGaP alloy used. However the use of GaAs in the future will make it possible to decrease the substrate cost.

Our first experiments show that although the twist bonded substrates behave effectively as a compliant substrate the coupling of the thin layer with the thick substrate is still too high. It results in the formation of dislocations that degrade the optical properties of the structure. However, we were able to get a 1.54 μm

photoluminescence wave length from this structure, demonstrating the validity of the all ternary 1.55 μm laser idea.

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SELECTIVE MOLECULAR BEAM EPITAXY FOR FORMATION OF NETWORKS OF InP-BASED InGaAs/InAlAs QUANTUM WIRES AND DOTS

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Introduction

Recent intensive research efforts in the study of quantum effects indicate that quantum nanostructures such as quantum wires and quantum dots may become key components of next-generation ultralarge scale integrated circuits based on quantum effects. For realizing such quantum LSIs, it is necessary to establish a suitable technology for formation of networks containing high quality quantum wires and dots with high packing density. For this purpose, selective MBE growth on patterned substrates appears to be promising because damage-free, extremely small and uniform, highly integrated, and position controlled quantum wires and dots can be formed only by the growth procedures.(1, 2) However, so far, there is no reports on selective growth formation of such quantum networks .

This paper presents a novel selective MBE growth technology for formation of an InP-based $In_{0.53}Ga_{0.47}As$ high quality quantum network. As the building blocks of such a network, the arrays of isolated wires, isolated dots and coupled wire-dot structures were successfully realized by further extending the selective MBE growth process on patterned substrates reported earlier.(3, 4)

I. Experimental

For formation of the isolated InGaAs quantum wires, an array of mesa-stripes along $<\bar{1}10>$-direction (pattern A) shown in Fig. 1(a) were formed by photolithography and wet chemical etching. Period of the mesa stripes and width of top (001) terrace were 4 and 1 μm, respectively. On the other hand, a 2-dimensional array of <100>-oriented square-mesa pedestals (pattern B) shown in Fig. 1(b) was prepared by photolithography and wet chemical etching, and was used for the growth of InGaAs quantum dots. Period and diagonal length of the square-mesas were 4 and 1.4 μm, respectively. By using electron beam lithography and wet chemical etching, an array of mesa-pedestals connected with each other by $<\bar{1}10>$-oriented mesa-stripes (pattern C), as shown in Fig. 1(c), were prepared for realization of coupled wire-dot structures. In this case, terrace width of the mesa-stripe was 0.7 μm and the periods of the mesa-pedestal along the directions parallel and perpendicular to the mesa-stripes were both 10 μm. Diagonal length of the square-mesa region (d_0) were varied in the range from 1.8 to 4 μm. An example of the plan-view SEM image of the pattern

C is also shown in Fig. 1(c).

Selective growth procedures were applied to these substrates by using a standard solid source MBE system. The InGaAs ridge quantum wires were formed by growing InAlAs/InGaAs/InAlAs structures with thick InGaAs buffer layers on the patterns A.(3, 4) InGaAs/InAlAs multi-layers were grown on the pattern B to form the InGaAs quantum dots. To form the coupled InGaAs wire-dot structures, the same condition for formation of the wires was applied to the pattern C.

(a) pattern A   (b) pattern B

(c) pattern C   3μm
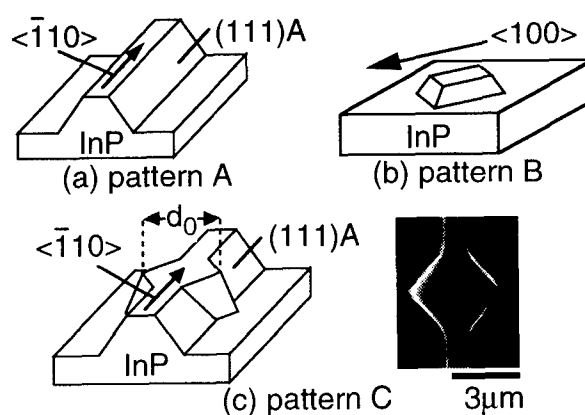
Fig. 1 Patterned substrates used in this study.

II. Results and Discussion

A. InGaAs ridge quantum wires

Figure 2(a) shows a schematic drawing of the overall wire structure grown on the pattern A. MBE growth of the thick InGaAs layer on the pattern A led to formation of a (311)A ridge structure. Subsequent growth of the bottom InAlAs layer on the InGaAs ridge at 580°C produced a narrow (411)A facet at the ridge top. Then, InGaAs wires surrounded by the (311)A and (411)A facets were grown selectively on the (411)A facet region. Since the width of the (411)A facet region was found to be proportional to the thickness of the InAlAs layers grown prior to the wire layer, the wire width could be controlled by changing the bottom InAlAs

(a)

200nm

(b)
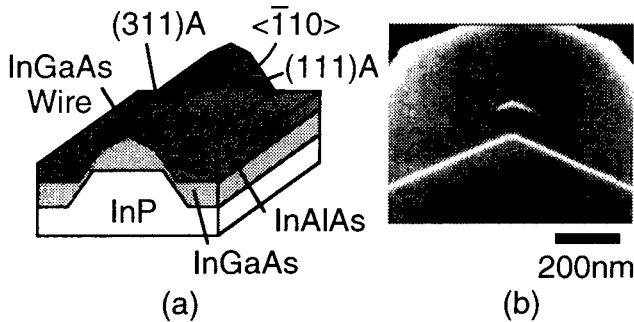
Fig. 2 (a) Overall structure of the InGaAs ridge quantum wire on the pattern A. (b) Cross-sectional SEM image of the main wire portion.
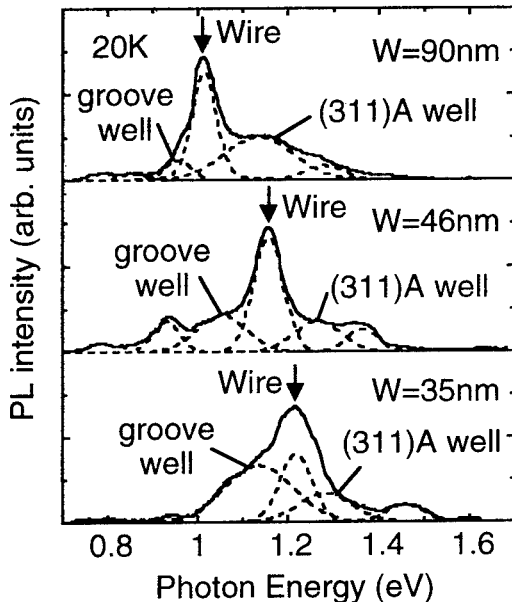
Fig. 3 PL spectra of the InGaAs ridge quantum wires having various wire width, W.

layer thickness. In this study, three kinds of InGaAs quantum wires having different wire width of 90, 46 and 35 nm, were formed. Details of such a selective growth mechanism and growth conditions have been discussed elsewhere.(3) Successful realization of arrow-head shaped InGaAs quantum wires having a lateral width of 90 nm can be seen in the SEM micrograph shown in Fig. 2(b).

Figure 3 summarizes PL spectra of the InGaAs quantum wires having different wire widths. From CL observations, dominant peaks in each spectrum was found to be due to the InGaAs ridge quantum wires themselves. The energy positions of these peaks agreed well with the numerically calculated transition energies using the observed shapes and sizes of each wire. Strong and fairly narrow emission peaks originating from the wires indicate that quantum wires having acceptable crystalline quality and uniformity are realized. Moreover, even at room temperature, strong PL emissions due to the wires was observed, also indicating the high crystal quality of the wires.

B. Isolated InGaAs quantum dots

SEM images of the InGaAs quantum dot formed on the pattern B are summarized in Fig. 4. By using an array of the mesa-pedestals, an array of the pyramidal-shaped InGaAs quantum dots defined by four smooth (521) facets were successfully formed as shown in Fig. 4(a) and 4(b).(5) As shown in Fig. 4(c), the width of the (100) terrace decreased as the growth proceeds and the growth rate of the InGaAs layer was enhanced on the (100) terrace, while the thickness of the InGaAs layers on the sidewalls remained very thin. Due to the large enhancement of growth rate of InGaAs on the terrace and the size reduction of the terrace width, an InGaAs quantum dot having a side length of 100 nm was realized on the (100) InAlAs terrace as seen in Fig. 4(c).

Figure 5 shows a PL spectrum of the InGaAs dot array taken at 20 K. Similar to the wire, the present InGaAs dot array showed a strong PL emission, indicating a formation of a high quality quantum dot array by the present selective MBE growth.

C. Coupled InGaAs wire-dot structures

Results of the SEM observations of the sample grown on the pattern C are summarized in Fig. 6. Figure 6(a) shows a plan-view SEM image of the wire-dot arrays having d_0=1.8-2.4 μm. As seen in

460

(a) Plan-view SEM image (low-magnification).

500nm

(b) Plan-view SEM image.

quantum dot   InGaAs   (521)

100nm   InP   InAlAs

(c) Cross-sectional SEM image.
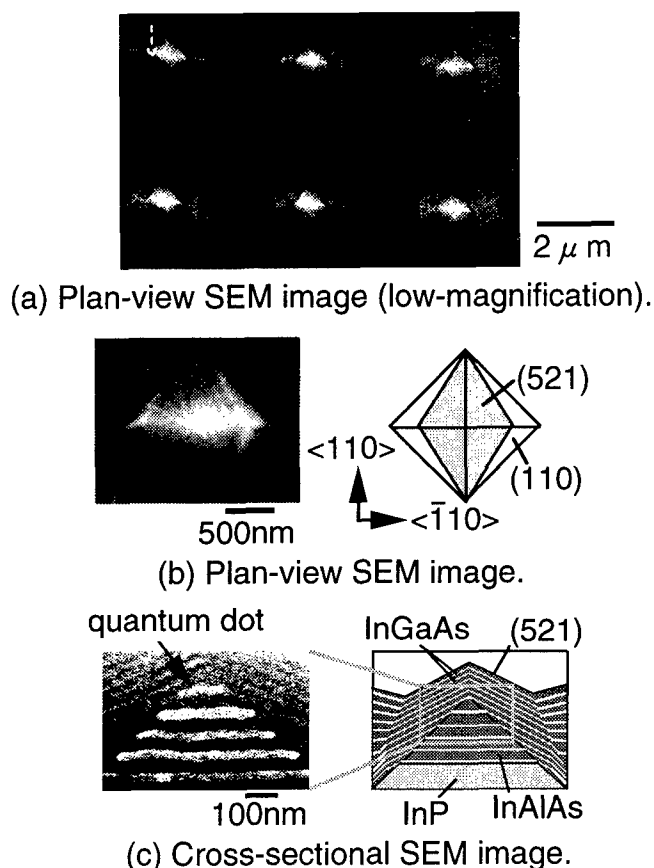
Fig. 4 SEM images of InGaAs quantum dot array on the pattern B.
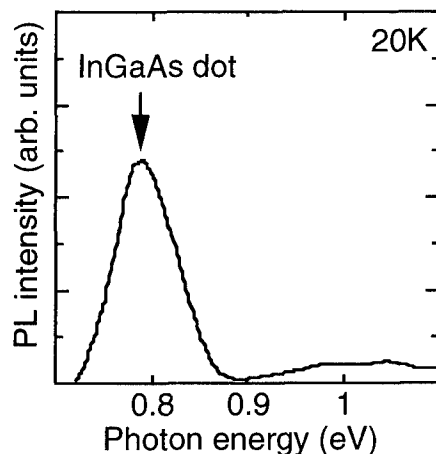
Fig. 5 PL sepctrum of the InGaAs dot array on the pattern B.

Fig. 6(a), uniformity of the wire-dot array is quite good. Magnified plan-view and bird's eye-view SEM images of the InGaAs dot on the smallest square-mesa (d_0=1.8 µm) are shown in Figs. 6(b) and 6(c), respectively. A pyramidal-shaped dot structure having four (521) facets appeared on the

square-mesa region whereas the (311)A ridge structures appeared on the narrow mesa regions.

Figure 7 shows a CL spectrum taken at 4 K by scanning the area shown in Fig. 6(b) with the electron beam. As shown here, 7 peaks indicated by arrows were observed. The peaks at 0.795 and 1.48 eV can be assigned as emissions from the InGaAs buffer layer and from the InAlAs barrier layer, respectively. To clarify spacial origins of other 5 peaks, monochromatic CL images were taken at each energy position as shown in Fig. 8. The corresponding plan-view SEM image is also given in Fig. 8(a). It was found from Fig. 8 that both of the peaks at 0.864 and 0.906 came from parasitic InGaAs quantum wells formed beside the (521) pyramids. On the other hand, peaks at 1.108 eV and 1.207 eV can be assigned as emissions due to parasitic quantum wells formed beside the ridge structure and those formed at the bottom flat regions, respectively. In the CL image taken at 1.0 eV, bright lines and spot can be clearly seen at the

d_0=2.4µm   2.2µm   2.0µm   1.8µm

10µm

(a) Plan-view SEM image (low-magnification).

(b) Plan-view   (c) Bird's eye-view
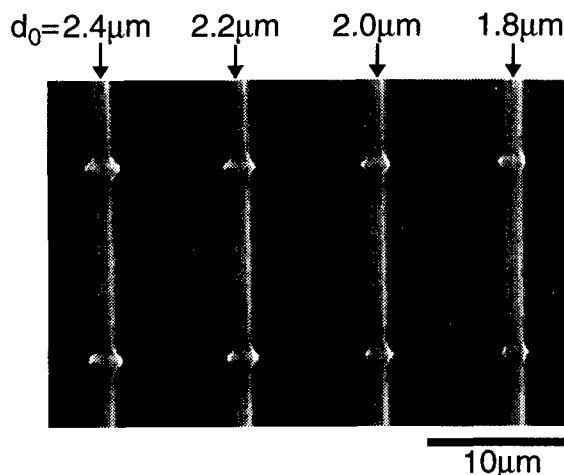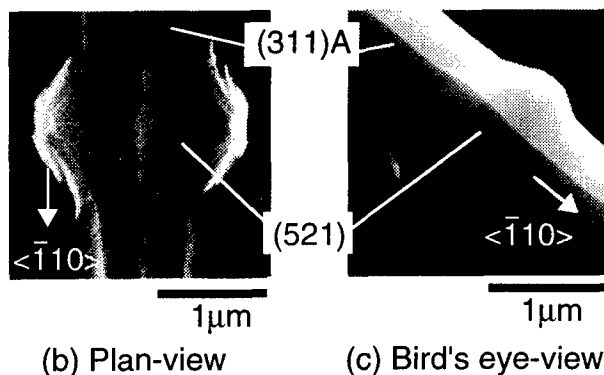
Fig. 6 SEM images of the InGaAs wire-dot structures grown on the pattern C.

461
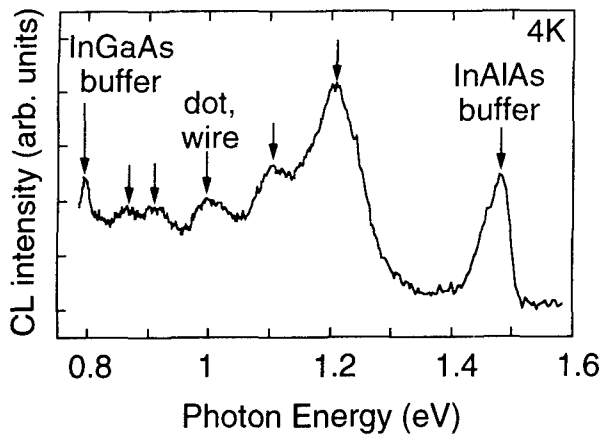
Fig. 7 CL spectrum of the InGaAs wire-dot structure taken by scanning the area shown in Fig. 6(b).

ridge top and center of the (521) pyramids, respectively. Therefore, the CL peak at 1.0 eV can be assigned as the emission from the InGaAs ridge quantum wire and InGaAs dot. Strong intensity of these spot and lines indicate the high quality InGaAs wire and dot were formed at the ridge and pyramid, respectively. Dark regions seen between the spot and lines in Fig. 8(d) indicates existence of a potential barrier between the wire and the dot. Since the degree of coupling between the wire and dot can be obviously be controlled by pattern geometry and growth condition, the present selective MBE growth technique can be applied to formation of quantum networks utilizing the various kinds of quantum mechanical phenomena, such as ballistic electron transport, quantum interference and single electron tunneling.

III. Summary

(1) High quality array of the isolated $In_{0.53}Ga_{0.47}As$ ridge quantum wires and that of the isolated $In_{0.53}Ga_{0.47}As$ dots were successfully formed by the selective MBE growth on the patterned substrates.

(2) By using the array of the mesa-pedestals connected with each other by $<\bar{1}10>$-oriented mesa-stripes, coupled $In_{0.53}Ga_{0.47}As$ wire-dot structures were successfully realized.

High quality InP-based coupled quantum structures as realized by our selective MBE appear to be promising for realization of a future high performance InP-based quantum networks.

(a) SEM image   (b) CL, E=0.86 eV

(c) CL, E=0.90 eV   (d) CL, E=1.0 eV

(e) CL, E=1.1 eV   (f) CL, E=1.2 eV
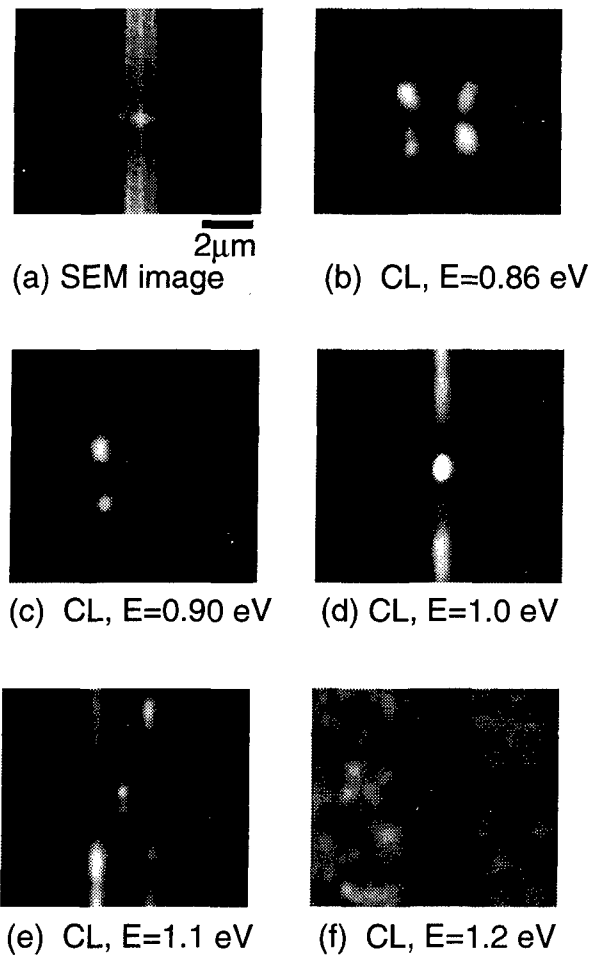
Fig. 8 Plan-view CL images taken at the energy position of the CL peaks together with the corresponding SEM image.

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GROWTH STUDY OF SELF-ASSEMBLED $Ga_xIn_{1-x}As$ ISLANDS ON InP

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Introduction

The growth of self-assembled tridimensional (3D) islands has been increasingly studied lately to produce quantum dots[1,2]. This technique is the most promissing for fundamental studies in a zero dimensional semiconductor system as well as for micro-optoelectronics devices applications, such as lasers and memory devices. The use of 3D-islands has however been limited by the lack of control of their size uniformity and of regular organization on the substrate surface.

We proposed to use InAs 3D islands as trapping zones in photorefractive structures on InP substrates[3]. For this application, we need islands which deeply confine the carriers for an efficient trapping mechanism. The islands also have to be dense enough to avoid any lateral diffusion of the carriers. In this work, we study the growth of InAs and $Ga_xIn_{1-x}As$ layers compressively strained on InP, in order to produce 3D islands which fulfil these requirements. The optical and structural properties of the islands have been characterized by photoluminescence (PL) and atomic force microscopy (AFM) respectively. We have been able to correlate the optical and structural properties of the islands by performing the PL and AFM measurements *on the same structure* for InAs and $Ga_xIn_{1-x}As$ islands. Finally, we compare the growth of $Ga_xIn_{1-x}As$ islands on (100) and (311)B InP substrates, for two $Ga_xIn_{1-x}As$ compositions.

I. Experimental.

The $Ga_xIn_{1-x}As$ strained layers are grown by gas source molecular beam epitaxy on $Ga_{0.47}In_{0.53}As$ or $Ga_{0.2}In_{0.8}As_{0.435}P_{0.565}$, (PL peak at 1.18 µm, designated below as $Q_{1.18}$) lattice-matched to InP, and capped with InP (figure 1). The amount of $Ga_xIn_{1-x}As$ deposited is above the critical thickness for the 2D to 3D growth mode transition[4]. The transition is checked on the electron diffraction (RHEED) pattern.
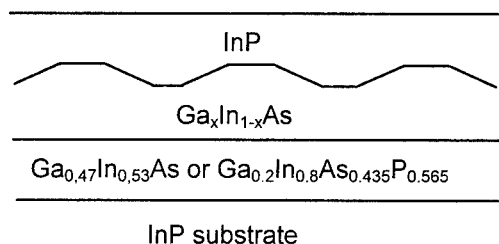
Figure 1. Structure with $Ga_xIn_{1-x}As$ islands on a $Ga_{0.47}In_{0.53}As$ or $Ga_{0.2}In_{0.8}As_{0.435}P_{0.565}$ layer lattice-matched on InP.

It is already known from transmission electron microscopy that 3D islands with and without the InP capping layer have very different dimensions[5]. This prevents the comparison between PL results on capped structures and AFM observations on uncapped samples. We developped a method which allows to make the PL and AFM measurements on the same sample.

PL studies are carried out on the as-grown samples. The PL experiments are performed at 2 K. The samples are excited at 514-nm, the power reaching the sample is about 100 W/cm². The PL is detected by a Peltier cooled PbS detector, using conventionnal lock-in technics.

The InP capping layer is then removed using a selective chemical etchant (H_3PO_4:HCl, 3:1). The $Ga_xIn_{1-x}As$ layer is revealed and characterized with an Autoprobe AFM in contact mode.

II. Results and discussion.

InAs islands and comparison between capped and uncapped islands.

A nominally 2.1 ML-high InAs layer is grown on the $Q_{1.18}$ buffer layer at 500°C. The growth is interrupted for 30-seconds at the growth temperature under an arsenic overpressure. For a first set (A), the sample is cooled down quickly and taken out of the chamber for the AFM measurements. For a second set of samples (B), the InAs layer is capped with a 500 Å-thick InP layer at 500°C.

Figure 2 shows AFM images of the as-grown sample A and figure 3 of sample B after the InP capping had been removed by the selective etching. For sample A, the islands are 1000 Å-wide, 100 to 200 Å-high and their
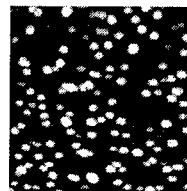
figure 2 : 2×2 µm² AFM image of the as-grown sample A.
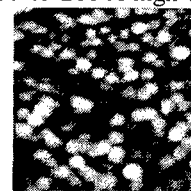
figure 3 : 2×2 µm² AFM image of sample B after removing the InP capping layer

density is 3×10^9 cm^{-2}. For the B sample, the islands are 1000 Å-wide, 25 to 40 Å-high and their density is 3×10^9 cm^{-2}.
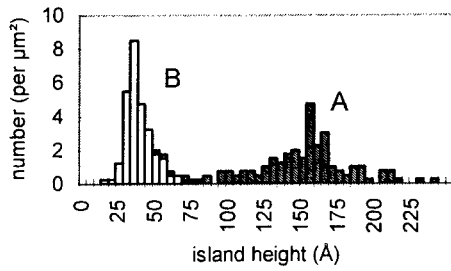
figure 4 : Island height histograms for the as-grown sample A and sample B after removing the InP capping layer.

The comparison between sample A and sample B shows the strong effect of the coverage on the island shape and distribution. The aspect ratio (height on base width) of the sample-A islands is four times higher than the one for sample B. It can be explained by energy considerations. The height of sample-A islands favors elastic relaxation of the top region of the dots. The relaxed islands induce tensile strain in the sample-B InP capping layer. It then becomes energetically favorable[6] for the islands to be flatter because they do not induce such a high strain in the capping layer. We suppose that for the sample-A the islands can also be re-arranged during the decrease in temperature, and that they are stabilized by the capping layer in sample B. We present PL experiments for sample B on figure 5. The PL signal is peaking at 696 meV, with a 75 meV FWHM. The lateral size distribution does not have a strong effect on the PL signal shape because the island base width is too large to induce quantum confinement.

We superpose the PL peak on the histogram of the height distribution to compare the optical and structural
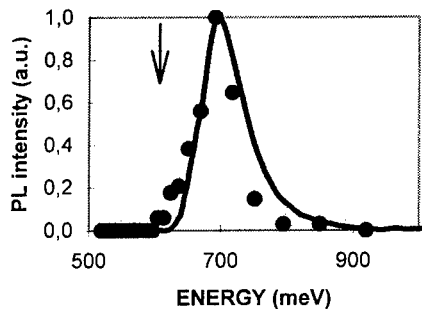
figure 5 : PL spectrum at 2K from sample B before removing the InP capping layer (——)and e-hh transitions calculations(●) from the height histogram from figure 4 (sample B).

characteristics of the islands in sample B. The horizontal axis is the e-hh (n=1) transition calculated for an InAs strained

quantum well[7] which width is the height of the island determined with AFM added to the thickness of the wetting layer. The calculation is based on the propagation matrix model for each band[7]. The vertical axis is the number of islands per μm^2 which has been normalised. There is a good agreement between sample-B PL and AFM results. The energy peak of PL coincides with the calculated one from AFM height histogram. Another important result is the good agreement between the PL FWHM and the islands height histogram FWHM. The broadening is due to the distribution of the islands heights. We also compare sample-B PL results and sample-A AFM experiments. The sample-A calculated energy peak is 100 meV lower than the sample-B PL one (arrow on the graph in figure 5). The sample-A AFM histogram FWHM is also larger than the sample-B one.

This shows that it is necessary to use the same structure for both PL and AFM measurements to be able to compare the results, rather than two different structures grown specifically for the PL and AFM measurements. It also demonstrates the validity of the method using the selective chemical etching.

$Ga_{0.2}In_{0.8}As$ islands: comparison between InP (100) and InP (311)B substrates:

In order to grow higher islands for a more efficient trapping, we studied the growth of $Ga_xIn_{1-x}As$ layers. The InAs island are 40 Å-high and increasing their height by growing a thicker InAs layer may induce plastic relaxation through misfit dislocations. Due to the introduction of gallium, the strain is lower than in InAs layers and bigger islands can be expected without any plastic relaxation.

It has been shown that the biggest islands for a given $Ga_xIn_{1-x}As$ composition are produced for a layer thickness just above the critical thickness for the 2D to 3D growth mode transition[8,9]. A 17.1 ML-thick $Ga_{0.2}In_{0.8}As$ layer (structure C) has been grown at 540°C on a $Ga_{0.47}In_{0.53}As$ buffer, followed by a 30 second-growth interruption and capped with InP. Growing on a $Ga_{0.47}In_{0.53}As$ buffer instead of the $Q_{1.18}$ buffer allows to grow the islands at higher temperature.

The PL intensity for structure C decreases by a factor of 2 to 3 only when the sample temperature increases from 2 to 300 K. For a 2D quantum well, the PL intensity would decrease by a factor of 30. The high PL intensity at room temperature can be explained by the fact that the carriers are efficiently trapped in the islands. In a 2D quantum well, when the sample temperature increases, the carriers become mobile and have a higher probability to recombine non radiatively on defects.

The AFM image of the structure after removing the InP capping layer, is shown in figure 6. The histograms give the height distribution of the islands. Their average base width is 475 Å and the island density 6.5×10^9 islands/cm^2. The islands are at most 85 Å high and the distribution peak is 35 Å.

The height distribution is larger for $Ga_{0.2}In_{0.8}As$ than for InAs. The height distribution is not symetric and

distorted towards the low values. This can be explained by the fact that the strain is much lower in the $Ga_{0.2}In_{0.8}As$ layer (2%) than in the InAs layer (3%). The elastic relaxation through the formation of 3D islands is progressive and occurs after several monolayers have been deposited. The strained layer becomes rougher before the islands appear. The smallest islands cannot be separated from the background roughness.
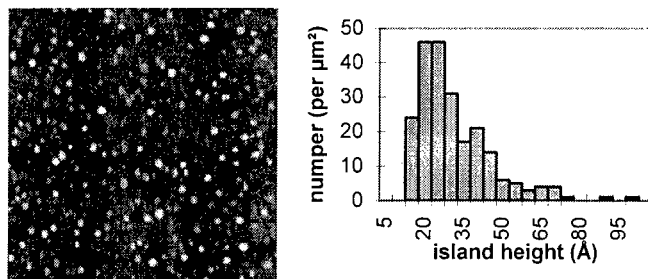
Figure 6. 2×2 μm² AFM image and height histogram of structure C, $Ga_{0.2}In_{0.8}As/InP(100)$ grown at 540°C.

The electron energy level in the $Ga_{0.2}In_{0.8}As$ quantum well being very close to the conduction band minimun of the $Ga_{0.47}In_{0.53}As$ barrier, we have not been able to calculate the e-hh transition corresponding to the height histograms for this structure.

In order to enhance the $Ga_xIn_{1-x}As$ island uniformity, we studied their growth on (311)B InP substrates. The growth of InGaAs islands on GaAs on (311)B substrate has shown a good organisation by MOVPE[10] and a narrower size distribution by MBE[11]. Self-organisation has been observed on (311)B InP substrates by MOVPE[12].

The structures have been grown simultaneously on two substrate orientations (100) and (311)B mounted side by side on the substrate holder. Structure D includes a 17.1 ML-thick $Ga_{0.2}In_{0.8}As$ layer and structure E a 11.9 ML-thick $Ga_{0.14}In_{0.86}As$ layer. The growth temperature is 510°C. After deposition on a $Q_{1.18}$ buffer layer, the $Ga_xIn_{1-}As$ is annealed 30 seconds under an arsenic overpressure and then capped with InP.

For x = 0.2, (structure D), PL measurements reveal a 2D quantum well behavior for the structure grown on (100) and a 3D islands behavior for (311)B. For the lower gallium content (x = 0.14) a 3D island behavior is observed for both orientations.

The AFM images have been made after the InP capping had been removed by the selective chemical etching. They are shown on figure 7. For the structure E (x=0.2, T=510°C), grown on the (100) substrate, no islands are observed while they are present on the (311)B substrate. These results are coherent with PL results which shows the 2D behaviour of the $Ga_{0.2}In_{0.8}As$ layer. The island height histrograms centered on 35 Å, the average island diameter is 1550 Å and their density is 1.5×10^9 per cm².

For x=0.14, on both substrate orientations, the islands can be observed. The histogram of the island height for the structure E on (100) give an average island height of 45 Å. Their density is 6.3×10^9 per cm² and their average base width

1200 Å. On (311)B, the height histogram is centered at 25 Å. The average island diameter is 860 Å and their density is 8.3×10^9 per cm².
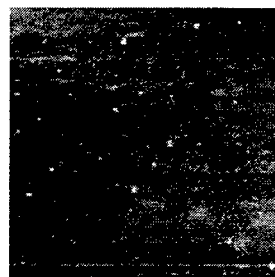
5×5 μm² AFM image of sample D grown on (100).
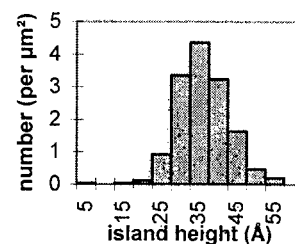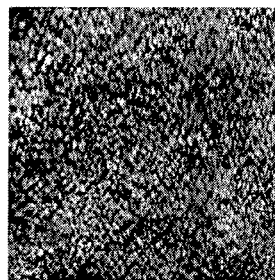
5×5 μm² AFM image of sample D grown on (311)B.
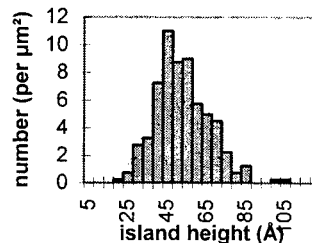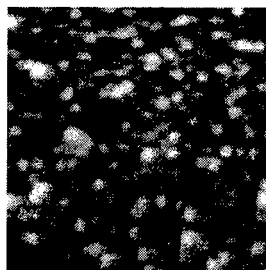
2×2 μm² AFM image of sample E grown on (100).
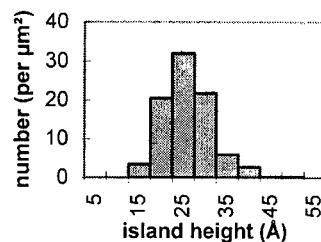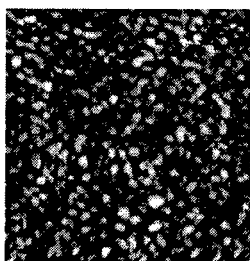
2×2 μm² AFM image of sample E grown on (311)B.

Figure 7. AFM images of the structures grown on InP (100) and InP (311)B with $Ga_{0.2}In_{0.8}As$ and $Ga_{0.14}In_{0.86}As$ and the height histograms.

The comparison between the structures C and D shows that the growth temperature has to be increased from 510°C (structure D) to 540°C (structure C) to produce islands on the (100) substrate. On the (311)B substrate, the islands are already observed at the low temperature. The height histogram is narrower for the structure grown on the (311)B substrate than for the structure grown on the (100) substrate.

Increasing the indium concentration from 80% to 86% (i.e. increasing the strain) allows the production of islands at

465

low temperature (structure E). For this composition, the structure grown on the (100) substrate presents heigher islands than the structure grown on (311)B. The height distribution is narrower for the (311)B orientation and the
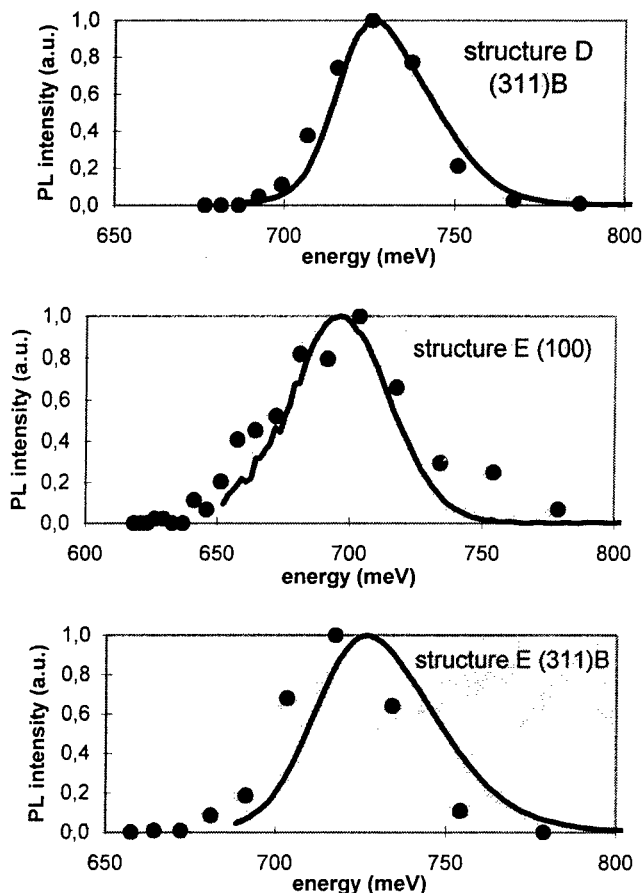

Figure 8. PL spectra at 2K from sample D and E before removing the InP capping layer ( ) and e-hh transitions calculations(●) from the height histograms of figure 7.

island density is higher.

To correlate optical and structural properties, we have used the same model and calculations as for the InAs islands. The superposition of the PL spectrum at 2 K and the results of the calculation are shown in figure 8. The wetting layer thickness has been estimated from the nominally deposited thickness minus the volume of the islands, calculated from the dimensions measured on the AFM images. There is a good agreement between the PL spectra for the structure F for both substrate orientations.

III. Conclusion.

The growth of InAs and $Ga_xIn_{1-x}As$ islands on InP has been studied and the structures have characterized by photoluminescence and atomic force microscopy.

We have demonstrated that it is necessary to perform the measurements on the same structure to be able to correlate the optical and the structural properties of the islands. We have used a selective chemical etching to remove the capping layer

used for the PL measurements to carry out the AFM observations on the same structure. The good correlation between the PL peak and the island height histogram shows that the islands can be considered as a 2D quantum wells with a modulated thickness.

The aim of the study was to grow homogeneous and high enough islands for an efficient carrier trapping. The most efficient way to obtain a high island density and a narrow islands height distribution is to use a (311)B substrate. This can be understood in term of adatom mobility at the substrate surface during the island growth: a high surface index increase this mobility[11] which in turn allows the island to grow quicker than on the (100) substrate. The fast growth of the islands limit the spreading of the sizes.

Increase the island height could be done by optimizing the growth conditions specifically for the (311)B substrate, as they may be different from the optimized one on (100). The final assesment for our islands will be to use them as trapping zones in a photorefractive structure.

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OPTICAL CHARACTERIZATION OF InGaAs/InP QUANTUM ^{TuE7} WIRE OVERGROWTH BY HYDRIDE VPE WITH InP

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We have investigated the optical properties of InGaAs/InP quantum wires prior to and after hydride VPE overgrowth. Hydride VPE is a particularly efficient overgrowth technique as it permits overgrowths with semiinsulating InP at large growth rates without leaving any voids. With this technique, a homogeneous and smooth surface was achieved. PL measurements of the overgrown wires with widths between 500 nm and 18 nm showed a significant increase of the luminescence intensities of up to one order of magnitude after overgrowth and a corresponding decrease of the side wall recombination velocity of up to two orders of magnitude. In addition, the radiative lifetimes of the wires below 100 nm are significantly increased after the overgrowth and are raised above the value of a 2D reference sample.

I. Introduction

In recent years, semiconductor nano-structures have been intensively investigated. On the one hand, they offer the fascinating possibility to study the behavior of basic physical properties when reducing the dimensionality. On the other hand, they promise novel and better features for device applications [1].

Nanostructures have been developed by different techniques [2]-[7]. Quantum structures of arbitrary size and shape can be fabricated by high resolution electron beam lithography, combined with dry or wet chemical etching. However, for device applications, an overgrowth of the open sidewalls and surfaces is mandatory in order to suppress the deterioration of the optical properties due to nonradiative recombination centers.

We have investigated the optical properties of wet etched InGaAs/InP quantum wires prior to and after hydride VPE overgrowth [8]. With this technique, we achieved an almost complete planarization of the wires after regrowth and a good surface morphology without leaving any voids. PL measurements of overgrown wires with widths down to 18 nm showed a significant increase of the luminescence intensities of one order of magnitude after overgrowth and a corresponding decrease of the side wall recombination velocity of up to two orders of magnitude.

II. Processing

The wires were fabricated using MOVPE grown lattice matched and compressively strained ($x_{In} = 75\%$) undoped InGaAs/InP quantum well samples with a quantum well thickness of 4.5 nm. Quantum wires with wire widths between 500 nm and 18 nm were fabricated by electron beam

lithography and wet chemical etching using Au etch masks. The wet etching process was carefully optimized to obtain a low concentration of residual surface recombination centers. A solution of Br_2:HBr:H_2O (1:3:12) was used at temperature of 21 °C. After the etching the gold masks were removed by a KI/I_2/H_2O solution. The etch depth was approximately 35 nm.

The etched wire structures were overgrown with a 50 nm thick semiinsulating InP:Fe layer by hydride VPE (T = 685 °C, V/III ratio ≈ 6). Etched only samples with identical wire patterns were processed as references.

Figure 1 shows a SEM micrograph of 18 nm wires after VPE overgrowth. The VPE process results in a homogeneous planarization of the etched wires. The wires are effectively buried within the InP and a smooth surface is achieved.
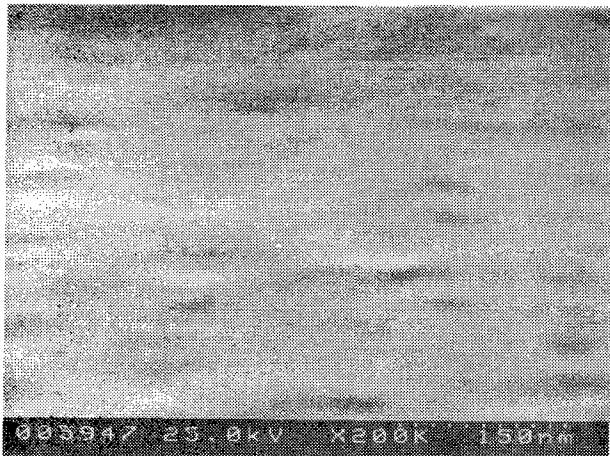
Fig. 1 : SEM micrograph of 18 nm quantum wires after hydride VPE overgrowth.

patterns with widths between 410 nm and 18 nm together with the spectra of a MESA pattern, which was used as a 2D reference (trace at the bottom of the figure). For wire widths below 50 nm a clear shift of the luminescence band to higher energy with reduced wire widths can be observed, which indicates the effective formation of a 1D potential. Hence, the blue shift is due to lateral quantization.
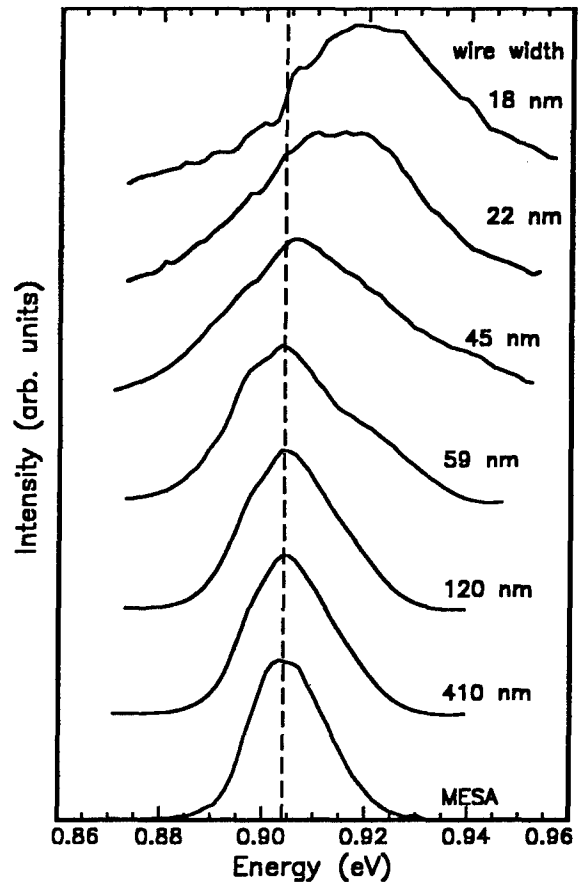
Fig. 2: PL spectra (T_{PL}=2K) of quantum wires with wire widths between 410 nm and 18 nm after hydride VPE overgrowth.

III. Optical characterization

The InGaAs/InP wires were investigated by optical spectroscopy after the etching and after the VPE overgrowth using cw-Ar^+ - ion laser (λ =514 nm, excitation density typically 1 W/cm^{-2}) for excitation and a liquid nitrogen cooled Ge detector. Figure 2 shows low temperature luminescence spectra of wire

Figure 3 shows the wire width dependence of the emission intensity of a lattice matched sample before (open dots) and after (full dots) overgrowth (T_{PL}= 2K). Before the overgrowth we observe a continous decrease of the emission intensity of the wire structures for wire widths below 100 nm. However, the relative emission intensity of the smallest wires is reduced only by about one order of

magnitude compared to that of a two dimensional reference. This indicates, that the wet etching process is essentially free of damage. After the overgrowth, this decay is removed completely and the emission intensity of 20 nm wide wires is comparable to that of the two dimensional reference.
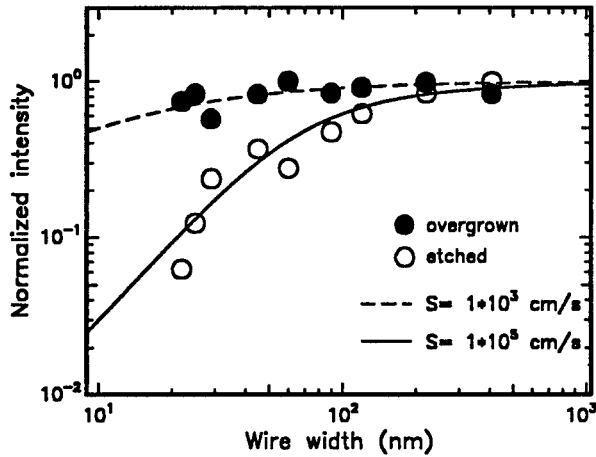
Fig. 3 : Normalized emission intensities as a function of wire width for a lattice matched InGaAs/InP sample before (open dots) and after (full dots) hydride VPE overgrowth (T_{PL}=2K). The intensity of a two dimensional reference sample corresponds to unity. The dashed and the solid line represent the calculated results of a diffusion model for the evaluation of the surface recombination velocity [9].

The improvement of the emission intensity particularly of the narrowest wires implies, that the VPE overgrowth process has efficiently passivated nonradiative recombination channels at the etched sidewalls. We have used a diffusion model for the decay of the quantum efficiency [9]. This model assumes diffusion of the generated carriers to the sidewalls of the wires and non radiative recombination at residual recombination centers. The surface recombination velocity S can be calculated as a fit parameter. With this model, we estimate a value of about 1×10^3 cm/s for the overgrown wires (dashed line in Fig. 3) This value is significantly smaller than the sidewall recombination velocity for the etched wires, which amounts to about 1×10^5 cm/s (solid line in Fig. 3).

The change of the electron hole pair lifetimes by the overgrowth has been measured using time resolved spectroscopy. The samples were excited by 0.1 ps pulses from a mode locked Ti:Sapphire laser ($\lambda = 850$ nm). The luminescence was detected with a time resolution of about 0.2 ps by optical upconversion [10]. Simultaneously with the decrease of the quantum efficiency of the etched wires, we observe a decrease of the carrier lifetime from about 1.4 ns to 0.7 ns when the wire width is reduced from 200 nm to 80 nm (see figure 4). In the overgrown structures, in contrast, the lifetime maintains the value of the 2D reference in this size range. For the smallest overgrown wires we observe even an increase to 1.8 ns, which may be due to carrier capture in interface traps. However, the long lifetimes are an additional clear indication of the passivation of the sidewall recombination centers in the etched wires after overgrowth.
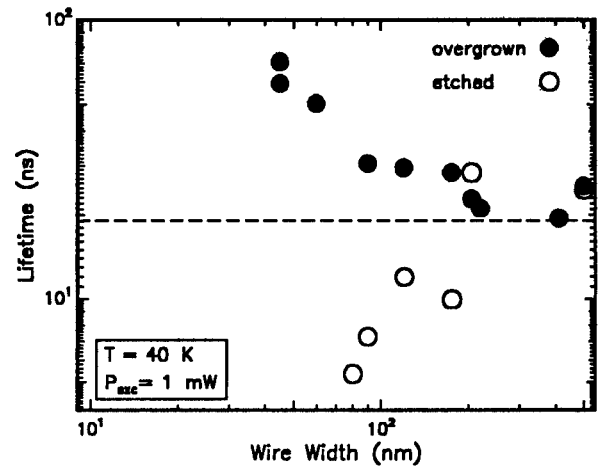
Fig. 4 : Radiative lifetimes as a function of wire width of InGaAs/InP wires before (open dots) and after (full dots) overgrowth. The lifetime of a two dimensional reference sample is about 1.3 ns (dashed line).

In order to avoid the influence of lateral carrier transfer from the InP into the overgrown structures we have investigated the change of the quantum efficiency in the InGaAs wire sections also by using below InP band gap excitation (excitation wavelength 950 nm). Before the overgrowth, the quantum efficiency decreases by about a factor of 20 in going down

469

from 500 nm to 20 nm wide wires. After the overgrowth, there is only a decay by a factor of 2 for the same range of wire widths. This clearly shows, that the increase of the emission intensities by one order of magnitude after overgrowth is due to the passivation of the nonradiative recombination centers.

IV. Conclusions

In conclusion, we have investigated the influence of hydride VPE overgrowth on the optical properties of wet etched InGaAs/InP quantum wires with wire widths between 500 nm and 18 nm. With the VPE process, a good surface morphology of the overgrown quantum wires could be obtained. In luminescence experiments we observed a significant increase of the emission intensities of the wires after overgrowth up to one order of magnitude both under resonant and nonresonant excitation. In addition, time resolved spectroscopy showed an increase of the radiative lifetimes especially for the smallest wire widths. The experiments clearly indicate, that the VPE overgrowth resulted in an effective passivation of the nonradiative recombination centers at the etched sidewalls of the wires.

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InP-based Monolithically Integrated Photoreceivers

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ABSTRACT

Photoreceivers, composed by a InGaAs photodetector monolithically integrated with either field-effect or bipolar transistor-based amplifiers, have achieved high-speed and high-sensitivities up to 20 Gb/s in single channel or aggregated throughput in multichannel configurations. A review of high performance InP-based technologies targeted to fiber optic communication applications is presented.

INTRODUCTION

In the last few years, the deployment of optical fiber systems has extensively increased, anticipating the greater demand for popular services such as voice, facsimile, electronic mail and enhanced video. With greater traffic demand, some transmission systems experiments have emphasized higher bit-rate in order to expand the bandwidth and therefore more capacity. Others have demonstrated the use of wavelength-division-multiplexing (WDM), which employs multiple channels at somewhat lower transmission rates, but attaining larger overall capacity. Both alternatives require high performance front-end receivers, which can realize effectively the conversion from the optical to the electronic domain. Within the area of high bit-rate applications (10 Gb/s and higher) for moderate distances under 100 km, high-sensitivity photoreceivers can provide the necessary link without resorting to the use of optical fiber amplifiers.

While for most commercial systems demonstrations, hybrid assemblies of the detector and hybrid amplifiers are still been used, monolithically integrated photoreceivers have recently shown comparable results to those of hybrid counterparts, demonstrating an constant trend in performance improvement for high bit-rates. Besides smaller chip area and reduced parasitics, which translates to lower noise and higher sensitivity, other advantages of the monolithic integration may include higher reliability and in a longer range possible lower assembly cost.

In this paper, the progress of InP-based optoelectronic integrated receivers achieved in the recent years will be reviewed and compared. The focus is on research results employing heterojunction field-effect transistors (HFETs) and heterojunction bipolar transistors(HBTs) successfully integrated to photodetectors for over 10 Gb/s applications with single channel or multichannel arrays.

EPITAXY AND INTEGRATION TECHNOLOGY
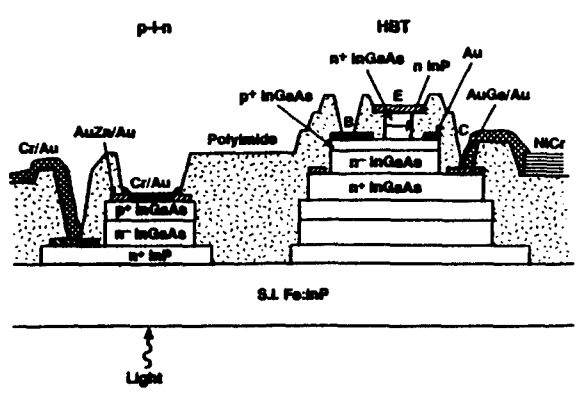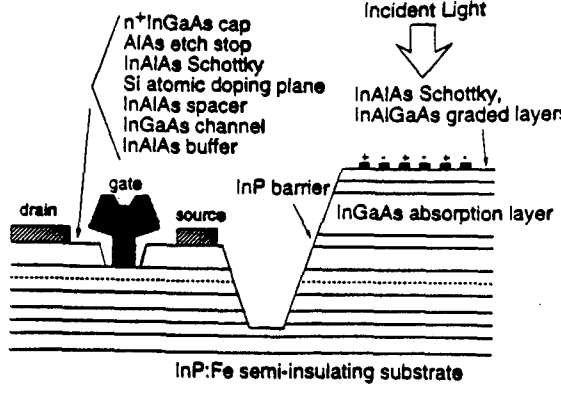
The epitaxial growth of lattice matched or strained structures on semi-insulating InP substrates has been realized either by one single or multiple runs employing metal organic vapor phase epitaxy (MOVPE), molecular beam epitaxy (MBE) or metal organic MBE (MOMBE). Usually, in one single run the photodetector layers can be grown sequentially either before or after the transistor structure is completed [1,2]. However, some

groups have been included recess etches between two growth runs to minimize the step coverage and therefore to ease lithographic constraints in the device processing [3,4]. Figure 1 summarizes some of the representative integration schemes for integrated photoreceivers which succeeded for over 10 Gb/s operation and with some of the devices characteristics.

Among photodetectors, there are few choices suitable for monolithically integration, the most popular being the conventional surface-illuminated p-i-n photodiode, with bandwidth values over 18 GHz and quantum efficiency better than 80% [1,3]. Important characteristics include good internal quantum efficiency, low capacitance, low series resistance and low dark current. In order to avoid the trade-off between internal quantum efficiency and carrier-transit time, waveguide p-i-n photodiodes (WGPDs) have recently been incorporated to photoreceivers with the advantage of planarity for packaging and integration with photonic devices. Reported values of 110 GHz bandwidth and quantum efficiency of 50% indicate the good performance of these WGPDs [5]. With more limited quantum efficiency, the metal-semiconductor-metal(MSM) detector may offer lower capacitance compared to p-i-n and in principle more compatibility for monolithic integration. Recent results including a surface layer to increase the Schottky barrier height and graded absorption layer to avoid carrier recombination have shown improved performance [2].

On transistors, parameters for high performance receivers include low capacitances, low leakage (p-n junctions and gate) currents and low parasitics. InAlAs/InGaAs-based HFET lattice matched to InP exhibit high transconductance, threshold voltage uniformity and high-frequency operation with relatively low gate leakage current. Despite the regrowth step used by some research groups, no degradation in both dc and rf performances have been observed in the transistors for modest gate lengths ($L_g > 1 \mu m$).

Kuebart et al. [3] reported a measured sensitivity of -19.2 dBm in a packaged optoelectronic integrated circuit (OEIC) by combining a front-illuminated p-i-n photodiode with a 1 μm gate length InAlAs/InGaAs HFET, in a two growth step sequence. First, the HFET layer structure was grown by LP-MOVPE, then after deep recess etch, the photodiode layers were deposited on the patterned substrate. In this case, the depth of the recess has to be adjusted to the p-i-n total thickness to minimize the step for contact. The doping of p-

pin-HBT [1]	MSM-HFET [2]
Single MOMBE run	Single MOVPE run
A_E = 3 x 8 μm^2; β = 65 f_T = 70 GHz	L_G = 0.2 μm; g_m = 800 mS/mm f_T = 105 GHz

pin-HFET [3]	WGPD-HFET [4]
Two-step MOVPE L_G = 1.0 μm; g_m = 300 mS/mm f_T = 30 GHz	Two-step MOVPE+MBE L_G = 0.2 μm; g_m = 800mS/mm f_T = 37 GHz

Figure 1: Cross sectional view of some of the most representative integration
technologies for InP-based integrated photoreceivers.

472

layer in the detector was obtained by diffusion.

Two other groups have also used the InAlAs/InGaAs HFET technology but integrating with a side-illuminated WGPD. Takahata et al.[5] in a single-step growth by LP-MOVPE has demonstrated a two-channel receiver array operating at 10 Gb/s with measured sensitivities of -16.1 dBm and -15.3 dBm for a 1 μm gate length HFET. Recently, van Waasen et al. [4] have reported a similar integration scheme obtained by a two-step growth structure. The waveguide and photodiode layers are sequentially grown by MOVPE. After removing the PD layers, the HFET structure is grown by MBE on top of the patterned waveguide. On-wafer measurements of the integrated receiver indicated a -3dB bandwidth of 27 GHz with a 1 μm gate length HFET. An alternative integration scheme was demonstrated by Fay et al. [2] using MSM-HFETs integrated receiver. In a single-step growth with MOVPE, the HFET structure was deposited prior to the MSM graded structure. For a 0.2 μm gate length, the integrated receiver had on-wafer measured bandwidth up to 18.5 GHz, with calculated sensitivity of -16.5 dBm at 10 Gb/s.

Another strong transistor technology for integrated photoreceivers is the heterojunction bipolar transistor in the InP/InGaAs emitter material system, with low noise and high frequency performance characteristics obtained with very relaxed geometries and any advanced self-aligned technology. In addition, the base-collector junction can double as a photodetector reducing the processing steps and minimizing the planarization profile. We have demonstrated operation up to 20 Gb/s with a measured sensitivity of -17 dBm for a packaged back-illuminated p-i-n/HBT photoreceiver [1]. From a single-step epitaxial growth by MOMBE, the transistor layers are stacked on top of the p-i-n. After standard self-aligned processing steps, the final transistor has 3 μm emitter width.

Table 1

InP-based Long Wavelength OEIC

	BW (GHz)	Speed (Gb/s)	Sensitivity (dBm)	Tz (Ω)
pin-HBT				
Lunardi [1]	10.4	20	-17.0	220
MSM-HFET				
Fay [2]	18.5	10	-16.5*	72
BC pin-HBT				
Yang [7]	19.5	10	-18.7*	200
Sano [8]	23.0	13	-9.9	---
HPT-HBT				
Kamitsuna [9]	12	---	---	10
pin-HFET				
Kuebart [3]	6.5	10	-19.2	260
WDPD-HFET				
Van Waasen [4]	27	20	-17.5*	100

* *ESTIMATED*

Table 1 summarizes reported research results on single channel long wavelength integrated receivers for over 10 Gb/s bit-rate operation.

CIRCUIT OPTIMIZATION

The preamplifier circuit design of choice has been the transimpedance configuration which provides wide bandwidth, large dynamic range and depending on the operation bias points, very low noise. In HFET circuit designs, the cascode or simple common-source have been used for the input stage [1,5]. The cascode input has a smaller input capacitance which translates to a lower noise and therefore higher sensitivity. While some designs include inductive peaking and high impedance configurations, the feedback resistor can also be replaced by HFET, operating in the linear region [2,6]. For bipolar transistors, the transimpedance amplifier may combine common-emitter input stage with inductive peaking or a double feedback loop for bias stabilization [1,7]. In addition to the conventional transimpedance configuration, a travelling wave amplifier (TWA), based on coplanar waveguide technology, with low input impedance appears to have the widest bandwidth reported to date on HFET-based photoreceivers [4]. By choosing a low input impedance, the measured characteristics have constant group delay with 27 GHz bandwidth. However, independent of circuit configuration, the highest sensitivity can be achieved by minimizing the noise contributions of the input transistor, which translates into high transconductance (g_m), high current gain, low parasitics (resistances and capacitances) and bias operating points. Independent of the transistor and circuit configuration, the bandwidth of the preamplifier depends strongly on the photodetector (assuming a very low dark current) and the input transistor capacitance.

MULTICHANNEL RECEIVER ARRAYS

Another very attractive application for OEICs is in wavelength division multiplexing (WDM) system architectures because the monolithic integration offers compactness, packaging simplicity and overall reduction in the number of components for achieving parallel optical signal transmission. A two-channel side-illuminated receiver array integrating WGPDs and InAlAs/InGaAs HFETs operating at 10 Gb/s has been reported [5]. The on-wafer measured sensitivities at an error-rate of 10^{-9} were -16.1 and -15.3 dBm, for each channel respectively.

In a more realistic WDM system environment, an eight-channel packaged OEIC receiver array has been reported, operating at 2.5 Gb/s per channel [10]. For simplicity and fewer processing steps, the photodetectors and transistors were fabricated from a single epitaxial structure, where the base-collector junction of the HBT doubles as the p-i-n diode. In the chip layout, the detectors were centered at a 250 μm pitch for fiber-ribbon mating. Illumination from the back of the chip through the substrate was used to optimized optical performance. The measured sensitivities of the individual channels at a bit-error-rate of 10^{-9} varied from -27.1 to -26.3 dBm, with a 0.8 dB spread mainly due to difference in optical coupling efficiency.

For multichannel receiver arrays, the interference of signals from one channel to another may degrade the overall performance. While optical crosstalk is likely to exist through optical reflections or poor optical isolation between nearest neighbors, the dominant interference seems to be from

electrical nature. Electrical crosstalk includes feedback signals originating mainly in bias supply lines and ground loops. The effect of crosstalk is a loss in sensitivity as the signal level increases and usually is strongest for nearest-neighbor channels. Recently, radiation metal shields have been integrated to receiver arrays and shown to reduce significantly the adjacent channel electrical crosstalk [11].

In Table 2, all reported long wavelength OEIC receiver arrays published in the last five years is listed, along with a figure of merit (as defined in the table) to compare the different results. As indicated a single monolithic chip can simultaneously have a large number of channels with high bandwidth and transimpedance.

Table 2

Long Wavelength OEIC Receiver Arrays

Technology	#Ch	BW (GHz)	T_z (Ω)	#Ch x BW x T_z kΩ.GHz
WGPD-HFET [5]	2	8.3	100	1.6
pin-HFET [12]	4	4.0	230	3.6
pin-HFET [13]	5	4.4	450	9.9
BC pin-HBT [14]	8	2.0	1,000	16.0
BC pin-HBT [15]	8	2.5	-	-
BC pin-HBT [11]	3	11.0	200	17.6

SUMMARY

Monolithically integrated photoreceivers using different device and integration technologies have measured performances up to 20 Gb/s. However, the results indicate that the sensitivity is more related to the individual transistor noise performance than the particular circuit configuration. New circuit architectures with measured bandwidths exceeding 27 GHz suggest operation for over 40 Gb/s bit-rate. For WDM applications, multichannel receiver arrays have already been tested in more a realistic environment of a testbed with comprehensive electrical crosstalk characterization. Further packaging improvements will certainly confirm the potential of this integration technology rather than simply be a replacement over conventional hybrid circuitry.

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DIGITAL PERFORMANCE OF HIGH-SPEED MSM-HEMT TuF2 MONOLITHICALLY INTEGRATED PHOTORECEIVERS

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Introduction

In this work, we report the first multigigabit digital performance of a monolithic MSM-HEMT photoreceiver lattice matched to an InP substrate, with measured sensitivities at 5 Gb/s, 8 Gb/s, and 10 Gb/s of -16.9 dBm, -13.1 dBm, and -10.7 dBm, respectively for 1.55 μm light. The integration of MSM-PD and HEMT is done via a vertical integration scheme in which the HEMT and MSM layers are grown sequentially on a planar substrate in a single uninterrupted growth. The integration process features 0.2 μm gate length HEMTs, 0.5 μm MSM electrodes, Cr thin-film resistors, and SiN_x metal-insulator-metal capacitors, passivation, and photodetector antireflection coatings. The receiver circuit uses a low-noise three-stage transimpedance amplifier topology, with broadband output matching to 50 Ω. Two different amplifier designs were fabricated, resulting in systems with transimpedances ranging from 865 to 580 Ω and bandwidths from 7.2 to 12.4 GHz. In all cases, the frequency response is flat over the receiver bandwidth, with no evidence of peaking or ringing. Receiver output noise power spectral density measurements have also been performed, and the input-referred noise current determined for each receiver. The low-noise amplifier design results in input noise current densities of approximately 6.5 pA/Hz$^{1/2}$ for a transimpedance of 865 Ω and bandwidth of 7.2 GHz, and 8 pA/Hz$^{1/2}$ for a transimpedance of 580 Ω and bandwidth of 12.4 GHz.

I. Background

Monolithically integrated photoreceivers are of interest for future generations of fiber telecommunication systems because of their potential for ultra-wide bandwidths with good noise and gain characteristics. The viability of monolithic photoreceivers for high bit rate communication systems has been established, with sensitivities as good as the best hybrid receivers [1]. Device technologies based on InP substrates that have been used for photoreceivers include pin-HBT [1,2], pin-HEMT [3,4], and MSM-HEMT [5-7]. Metal-semiconductor-metal photodetectors (MSM-PDs) are an alternative to pin photodiodes that may have an advantage over pin photodiodes, especially at very high speeds due to the inherently low areal capacitance of the interdigitated MSM structure. Previous digital characterization of MSM-HEMT photoreceivers have been limited to either bit rates less than 5 Gb/s for InP substrates, or have been performed on circuits fabricated on GaAs substrates [8]. For the first time, we report multigigabit performance of MSM-HEMT monolithically integrated photoreceivers lattice matched to an InP substrate.

II. Fabrication and Circuit Design

The fabrication process for the integrated photoreceivers is similar to that reported previously [7], with the exception that a Cr thin film resistor process has been added to the process sequence for additional circuit flexibility. A cross-sectional diagram of the heterostructure used for the photoreceivers is shown in Figure 1. Device isolation for both the HEMTs and MSM-PDs is accomplished using citric acid/hydrogen peroxide solutions that result in a crystallographic etch profile. This profile is sloped sufficiently to allow interconnect metallizations to be run directly over the mesa steps without the need for additional planarization. The HEMTs used in this work are 0.2 μm gate length devices with a mushroom-shaped gate profile, defined by electron beam lithography in a PMMA/P(MMA-MAA) three-layer resist structure similar to that used in [9]. In order to achieve adequate threshold voltage uniformity, the HEMT portion of the layer structure includes a 2 nm thick pseudomorphic AlAs etch stop layer. This layer allows very repeatable and uniform gate recessing with simple citric acid/hydrogen peroxide wet etchants. The HEMTs have a threshold voltage of –0.9 V, with a standard deviation of 20 mV for an 84-device sample.
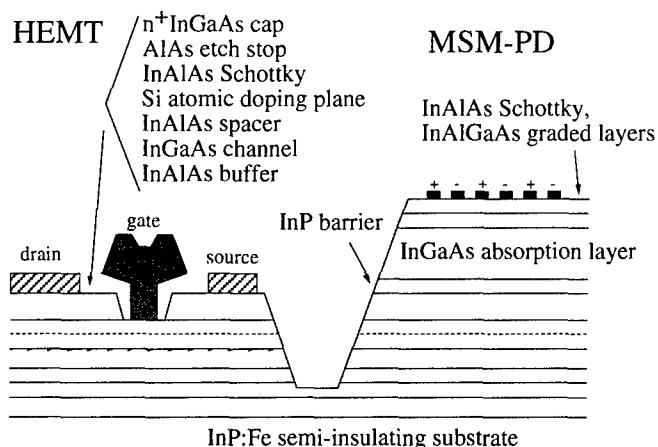
Figure 1. Schematic diagram of heterostructure cross-section.

The circuit design used for the preamplifier in the photoreceivers is a three-stage transimpedance type feedback amplifier. In this work, two different amplifiers were investigated, and a schematic diagram of each is shown in Figure 2. The circuits are differentiated primarily by the value of the feedback resistance and by the bias points selected for the amplifying transistors. In the first circuit (Figure 2a), the feedback resistor is 800 Ω, and the quiescent bias points of transistors Q_1, Q_4, and Q_5 are selected for low-noise operation at the expense of gain and speed. For the second circuit (Figure 2b), the feedback resistor value used is 500 Ω, and the amplifying transistors have been biased for maximum gain. The output stage of both amplifiers has been designed both to provide a broadband match to 50 Ω as well as to supply a small amount of additional voltage gain. The MSM-PDs used for the photoreceivers in this work had 0.5 μm electrode widths, 1 μm interelectrode spacings, and a 1 μm thick absorption region.

III. Experimental Results

The small-signal performance of the photoreceivers has been characterized, and the obtained frequency response for a representative of each circuit type is shown in Figure 3. The circuit with devices biased for low noise operation exhibits a -3 dB optoelectronic bandwidth of 7.2 GHz, and a midband responsivity of 346 V/W. The midband transimpedance of the amplifier is measured to be 865 Ω when the circuit is driving a 50 Ω load. For the second, high speed, circuit, the -3 dB bandwidth was measured to be 12.4 GHz, with a responsivity of 177 V/W and a midband transimpedance of 580 Ω. In both cases, the frequency response is flat and devoid of any resonances. To evaluate the effectiveness of the output stage for broadband impedance matching, the output VSWR was computed from on-wafer electrical s-parameter measurements of the output port. Figure 4 shows the output VSWR for a typical amplifier as a function of frequency; for all frequencies in the bandwidth of the receiver, the VSWR was found to be ≤ 1.3.

The microwave noise properties of the photoreceiver have also been characterized from output noise power spectral den-
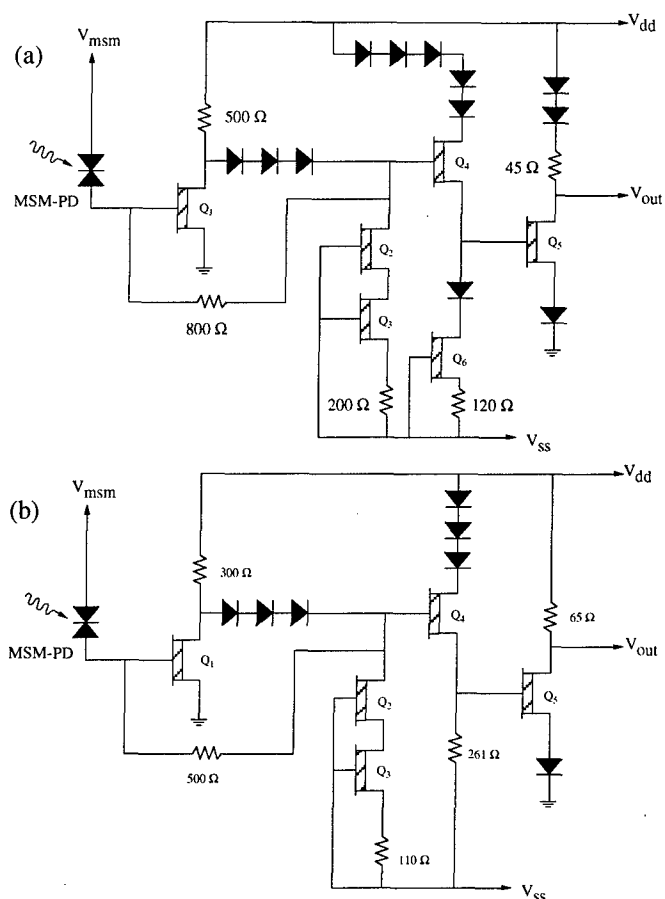
Figure 2. Circuit schematic diagrams for (a) low-noise and (b) high-speed photoreceivers.

sity measurements. Figure 5 shows the input-referred noise current spectral density obtained from these measurements for the photoreceivers in this work. For the low-noise circuit with 865 Ω transimpedance, the average input-referred noise current spectral density was 6.5 pA/Hz$^{1/2}$ for the region over which the noise was approximately constant. For the second circuit variation with a 580 Ω transimpedance and 12.4 GHz bandwidth, the average input noise current was found to be 8 pA/Hz$^{1/2}$.
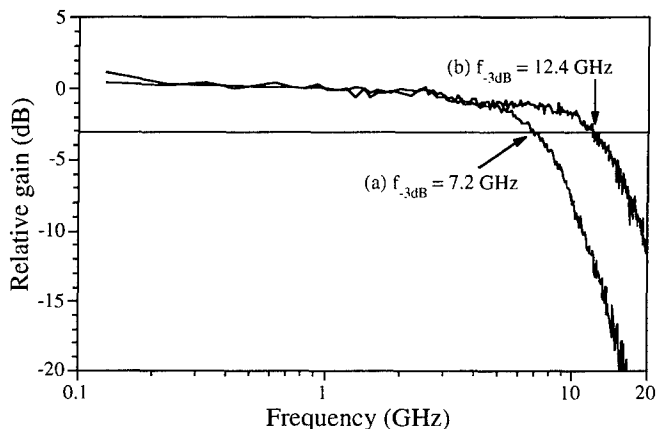
Figure 3. Small-signal optoelectronic frequency response for (a) low-noise and (b) high-speed versions of circuit.

476
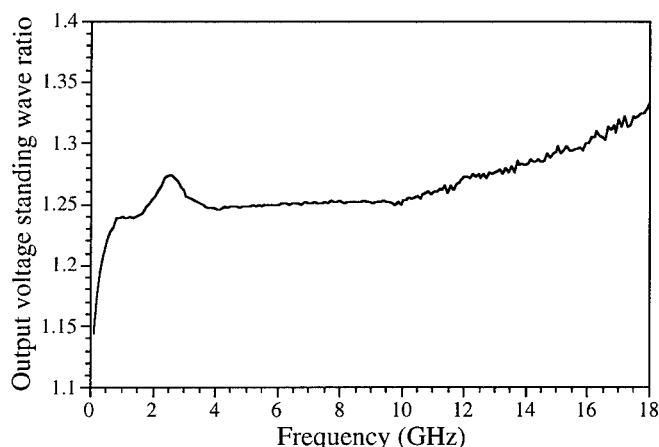
Figure 4. Output VSWR as a function of frequency for a typical photoreceiver. Within the bandwidth of receiver, maximum VSWR < 1.3.

The digital performance of packaged photoreceivers was characterized using direct bit error rate measurement. The package used consisted of microstrip lines on a duroid substrate for signal and power supply lines, with external chip bypass capacitors on each power supply line. Interconnects between the photoreceiver and the microstrip were accomplished using thermocompression wire bonds. Figure 6 shows the bit error rate performance of the receivers at 5 Gb/s, 8 Gb/s, and 10 Gb/s for a 2^7-1 pattern length pseudorandom bit stream. Eye patterns for the low-noise receiver at 5 Gb/s and 10 Gb/s are shown in Figure 6a and b, respectively. The obtained sensitivities for the receivers at a bit error rate of 10^{-9} were -16.9 dBm at 5 Gb/s, -13.1 dBm at 8 Gb/s and -10.7 dBm at 10 Gb/s. To the best of the authors' knowledge, this is the first report of directly-measured sensitivities at these bit rates for integrated MSM-HEMT photoreceivers on InP substrates. The sensitivities of the low-noise and high-speed versions of the circuit were virtually indistinguishable, despite the observed differences in input noise current spectral density and small-signal amplifier gain.
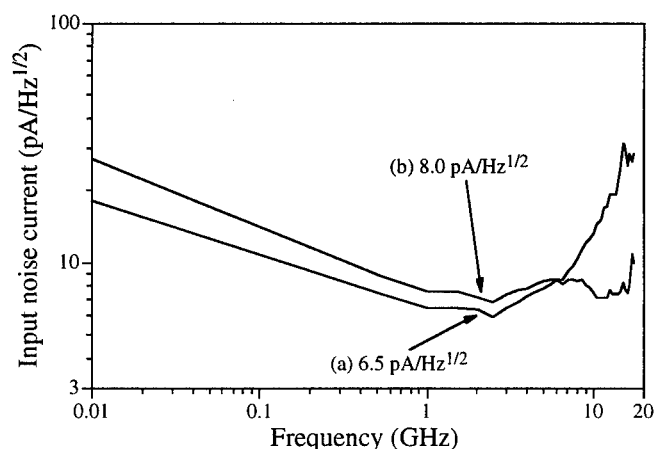
Figure 5. Input-referred noise current spectral density for (a) low-noise and (b) high-speed circuit versions.

IV. Discussion

As noted in the previous section, the sensitivity of the low-noise and the high-speed versions of the photoreceivers were practically identical, and the sensitivities measured are some-
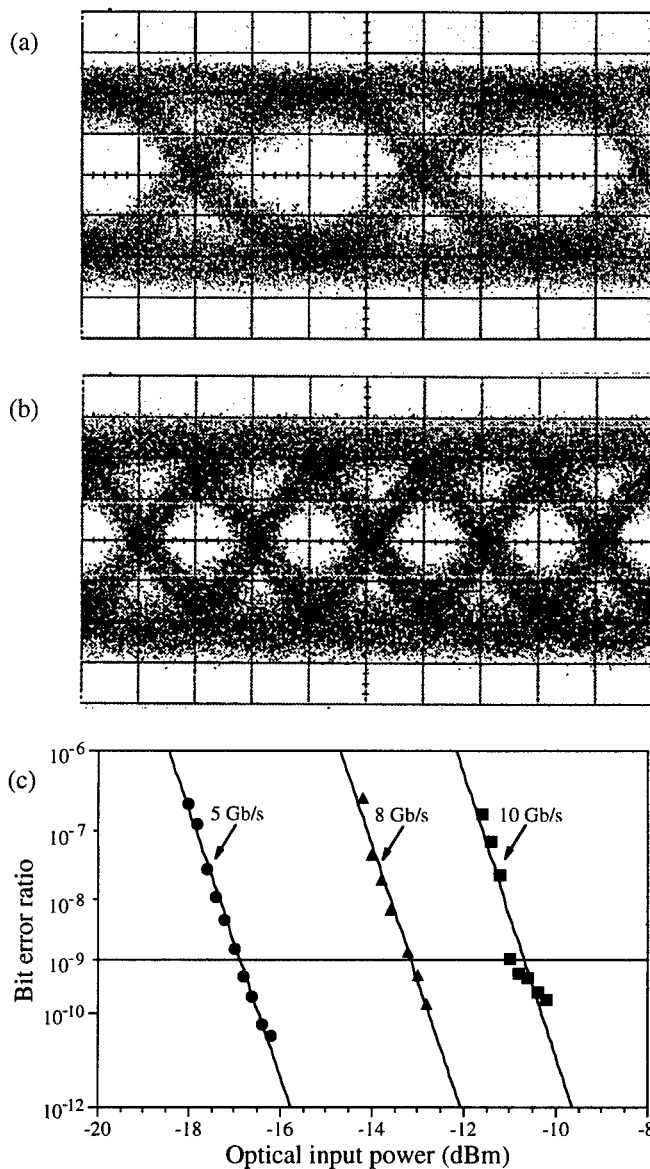
Figure 6. Eye pattern of photoreceiver at (a) 5 Gb/s and (b) 10 Gb/s for -11 dBm optical input power. Scales are 50 ps and 100 mV per division. (c) Bit error rate performance of photoreceiver at 5, 8 and 10 Gb/s.

what worse than the previous results obtained for MSM-HEMT photoreceivers integrated on GaAs substrates with 1.3 μm light [8], despite the excellent microwave noise performance that was obtained. From the input noise current spectral density, one can compute a theoretical noise-limited sensitivity that accounts for the receiver's finite bandwidth and noise contributions to bit error rate. Performing these calculations on the microwave

477

noise and small-signal frequency responses from Figures 5 and 3 results in projected sensitivities of -17.8 dBm and -14.6 dBm for the low-noise circuit at 5 Gb/s and 10 Gb/s, respectively, for a bit error rate of 10^{-9}.

To investigate the disparity between the directly measured sensitivity and the sensitivity as projected from microwave noise measurements, an analysis of the pulse response of the photoreceiver was undertaken. Figure 7a shows the response of a low-noise photoreceiver to a portion of a pseudorandom bit stream at 1 Gb/s. Although the initial rise and fall times are quite short as expected from the relatively large small-signal bandwidth of the photoreceiver, a much slower component in the output signal is readily apparent. Figure 7b shows a portion of this pulse train, as well as a curve fit to the time response, using the expression $V_o = \alpha \exp(-t/\tau_1) + \beta \exp(-t/\tau_2)$, where the parameters α, β, τ_1, and τ_2 are empirically fit to the measured data. From this procedure, $\alpha = 351$ V/W, $\beta = 207$ V/W, $\tau_1 = 0.142$ ns, and $\tau_2 = 7.762$ ns. The presence of the τ_2 response in the step response gives rise to a low-frequency "shelving" of the gain at frequencies below 100 MHz. As a result of the distortion introduced by this slow time constant, the observed eye pattern is closed somewhat compared to what would be expected from noise considerations alone. Including this effect along with the microwave noise and bandwidth results in projected sensitivities for the low-noise circuit of -16.1 dBm at 5 Gb/s and -12.9 dBm at 10 Gb/s for the photoreceivers, in better agreement with the directly determined values of -16.9 dBm and -10.7 dBm. The origin of this slow process in the photoreceiver appears to be the particular MSM-PDs used in these photoreceivers; tests of the step response of amplifiers fabricated on the same sample as the photoreceivers show no

Figure 7. 1 Gb/s PRBS pulse train, with time constant extraction from step response. Optical power is -13.6 dBm, and photoreceiver is followed by 28 dB of electrical gain.

evidence of this effect.

We postulate that the observed frequency response shelving is due to the disturbance of the usual MSM-PD electric field profile by the underlying HEMT structure. The presence of the highly conductive HEMT layers beneath the MSM-PD's absorption region results in electric field lines that are less lateral and more vertical than in a typical non-integrated MSM-PD structure, and thus the path length of the photogenerated carriers is increased. This perturbation of the electric field also tends to force more of the photocarriers to travel along the bottom heterointerface of the MSM structure, further slowing the detector. At present, further experiments are in progress to unambiguously resolve the origin of this problem, as well as to eliminate this effect.

V. Conclusions

For the first time, we have demonstrated the digital performance of monolithically integrated MSM-HEMT photoreceivers lattice matched to InP substrates at bit rates of 5 Gb/s, 8 Gb/s, and 10 Gb/s. Two different electronic amplifier configurations, corresponding to low-noise and high-speed designs, were evaluated in terms of noise, small-signal frequency response, and bit error rate. Directly measured sensitivities at a bit error ratio of 10^{-9} of -16.9 dBm, -13.1 dBm, and -10.7 dBm were achieved at 5, 8, and 10 Gb/s, respectively. Deviation from the expected sensitivity performance was observed experimentally, and possible sources for this discrepancy examined.

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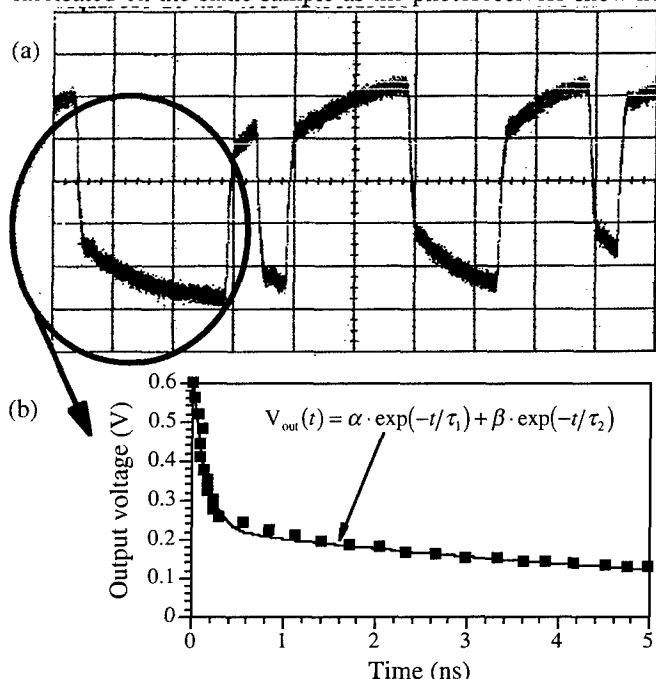
High Speed Optoelectronic InP/InGaAs Logic Pixel

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We describe InP/InGaAs optoelectronic smart pixels consisting of monolithically integrated p-i-n photodiodes, heterojunction bipolar transistor (HBT) receivers and transmitters, and surface-bonded folded-cavity surface emitting lasers (FCSELs). A minimum switching energy of 6 fJ, a maximum pixel bandwidth of 800 MHz, and a optoelectronic gain of 3 are achieved. These performance characteristics are competitive or superior to those of all-electronic interconnects.

I. Introduction

Current trends toward increasing complexity and performance of VLSI circuits have lead to a situation where the electrical interconnects are bandwidth bottlenecks in state-of-the-art computing systems. For this reason, optical information processing systems and interconnections, have generated considerable interest[1]. There are several advantages for using optics as the interconnection medium. Optical beams are relatively free from crosstalk and clock skew, and by exploiting the vertical input/output geometry in a 2D array of devices, the amount of information that can be processed by the system is vast. Smart pixels, which perform logic, amplification, switching or other functions on the incident light signals constitute the building blocks for such architectures.

In designing a smart pixel, certain performance factors must be considered, including the information flux density[2] (defined as the product of bandwidth and pixel circuit density), power dissipation, and switching energy Cascadability, or the ability for the output of a pixel to switch the next pixel in a logical chain, is another important feature. To be cascadable, the pixel output optical intensity ratio between a one and a zero state has to be greater than the incident input on/off ratio. Differential optical gain, laser threshold current, and dynamic range of the circuit are important factors in ensuring cascadability.

It has been proposed that optoelectronic gate technology, where the optical signal is converted into the electrical domain prior to processing, and then reconverting back into the optical domain for output, is suitable for smart pixels requiring high speed and low switching energy.[2] Such optoelectronic smart pixels combine the advantages of optics with the flexibility of electronics, enabling the implementation of different logic functions. Other functions such as wavelength conversion and multiplexing can also be implemented using this approach.

In this paper, we describe the design, fabrication, and performance of InP/InGaAs optoelectronic smart pixels operating at 1.3µm wavelength. A record high bandwidth of 800 MHz was achieved with a minimum switching energy of 6 fJ and an optoelectronic gain of 3.

II. Design and Fabrication of the Smart Pixel

The circuit studied is shown in Fig. 1. The optical input device and electrical circuit is composed of monolithically integrated p-i-n photodiodes and heterojunction bipolar transistors (HBTs). The output devices are 1.3µm wavelength folded-cavity surface emitting lasers (FCSELs) surface-mounted onto the pixel circuit[3]. The surface normal geometry of p-i-n photodiodes and FCSELs allows for free space, cascading array architectures.

The circuit is divided into three sections. The first consists of a p-i-n photodiode input logic circuit, and heterojunction bipolar transistors

(HBTs) Q_1 and Q_2 which form the transimpedance receiver front end. The p-i-n input logic circuit (inset, Fig. 1) consists of two p-i-n photodiodes which are connected in configurations according to the logic rewquirements of the pixel: parallel connection is used for OR/NOR logic, and series connection is used for AND/NAND logic. The feedback resistance, $R_f = 1$ kΩ, is chosen to maximize bandwidth and dynamic range, while maintaining suitable sensitivity and gain. The output of the front end is connected to an inverting voltage amplifier consisting of transistors Q_3 and Q_4. The voltage gain of this stage is determined by the ratio of the Q_3 collector resistor, $R_3 = 1$ kΩ, and the emitter contact resistance of Q_3, (~ 100 Ω). The FCSELs are connected to the collectors of Q_5 and Q_6 which form a differential pair, thus providing both positive (FCSEL$_1$ for AND and OR) and negative (FCSEL$_2$ for NAND and NOR) output logic. The total current through the differential pair can be adjusted by the emitter voltage of Q_7. The laser driver includes Q_8 and Q_9 which provide the laser pre-bias current. The supply voltage is 3 V, and the resistance of all the resistors in the circuit is 1 kΩ. This low supply voltage is necessary to ensure minimum quiescent power dissipation, thereby allowing for a maximum pixel packing density in the 2-D arrays.
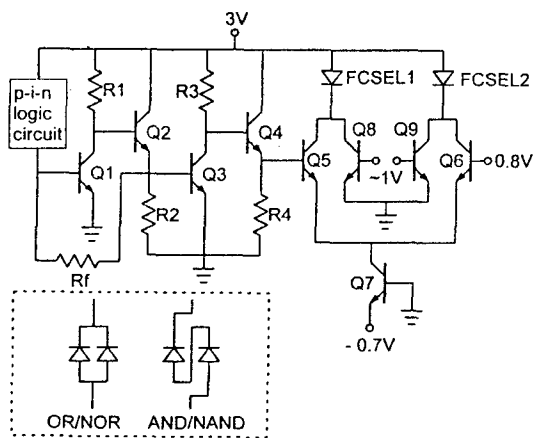
Fig. 1: Schematic diagram of the smart pixel gate

The simulated bandwidth was 800 MHz, depending primarily on R_f and the base-collector junction capacitance (C_{bc}) of the front end HBT,

and the differential gain (i.e. the product of the quantum efficiency of the p-i-n diode, laser slope efficiency, and the circuit gain) was predicted to be between 3- 8.

All wafers were grown by gas-source molecular epitaxy. The epitaxial layer structure of the circuit is shown in Table 1. The epitaxial layer structure and processing sequence of the FCSELs is identical to our previously published work[3].

Table 1. Epitaxial structure of p-i-n/HBT circuit.

Layer	Material	Doping (cm^{-3})	Thickness
emit. cont.	InGaAs	n+ 10^{19}	2000Å
emit. grad.	InP	n+ 5×10^{18}	500Å
emitter	InP	n 2×10^{17}	2000Å
set back	InGaAs	U/D	100Å
base	InGaAs	p+ 10^{19}	600Å
collector	InGaAs	U/D	4000Å
etch stop	InP	n+ 10^{19}	100Å
sub collec.	InGaAs	n+ 10^{19}	2000Å
p	InP	p+ 10^{19}	1000Å
i	InGaAs	U/D	1.5 μm
n	InP	n+ 10^{19}	2000Å
Substrate	InP	S. I.	

The processing of the p-i-n/HBT circuit was compatible with the different devices used in the circuit. First, circuit isolation mesas were formed by material selective wet etching, using 5:1:5 citric acid (50%) : H_2O_2 : H_2O solution and 3:1 HCl: H_3PO_4 for InGaAs and InP, respectively. The HBTs were passivated using a combination of etching in buffered HF followed by coating with polyimide.[4] After the 1 μm thick polyimide was cured at 300 °C for 30 minutes, contact holes were etched using O_2 plasma reactive ion etching (RIE) with a pre-patterned 1000 Å thick e-beam evaporated SiO mask. Then, Ge/Au/Ni/Au (270/ 450/215/450 Å) n-metal contacts were e-beam deposited, followed by alloying in a rapid thermal annealer (RTA) at 360 °C for 90 seconds. Ti/Pt/Au (200/300/1000 Å) p-metal contacts were then e-beam deposited. The 1 kΩ resistors were made

using 500 Å thick Ti film with sheet resistivity of 50 $\Omega/\square$. The interconnect metal is Ti/Au.

The front end and voltage amplifier HBTs (Q_1 - Q_4) had an E-B junction area of $8x8\mu m$, and a B-C junction area of $10x16\mu m$. The transistors in the transmitter (Q_5 - Q_9) handle larger currents (≤ 50 mA), and thus are larger than Q_1 - Q_4 with $16x16\mu m$ and $18x24\mu m$ for the E-B and B-C junctions, respectively. The p-i-n photodiode has a active area diameter of $30\mu m$.

The FCSELs were bonded n-side down on a 300x700 μm metal pad of the p-i-n/HBT circuit using silver epoxy, which was cured at 150 °C for 10 min. The p contact was wire-bonded to an adjacent pad on the circuit. A schematic cross-section of the smart pixel is shown in Fig. 2. Each pixel occupies $800x1600\mu m$, with the laser occupying more than 30 % of the pixel area. The pixel was mounted on a heat sink in order to achieve CW laser operation.
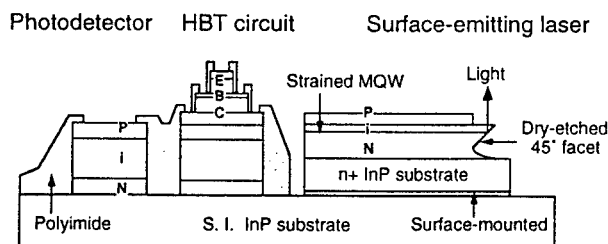
Fig. 2: Schematic cross-section of the pixel

III. Device and Circuit Performance.

The performance of the individual integrated devices was comparable to discrete devices with similar structures. The non-anti-reflection coated p-i-n dark current at -1 V is 2.4nA, and the external quantum efficiency is >55%. A current gain, $\beta >$ 400 was achieved for the HBTs, which to the best of our knowledge, is the highest reported gain for an integrated InP-based HBT[5]. The base leakage current was <10 pA is a consequence of the HF/polyimide surface passivation.[4] Thhe HBT shows high gain ($\beta > 20$) even with input currents as low as 10 pA. The FCSELs exhibit CW threshold currents (I_{th}) ranging from 24 to 50 mA,

with external slope efficiency for surface emission from 15 % to 17 % per facet. High density implementation of such circuits is almost completely determined by the power dissipation of the output laser elements. Long wavelength surface emitting lasers with very low I_{th} have yet to be achieved, although work in low threshold long wavelength FCSELs[3] and vertical-cavity surface emitting lasers (VCSELs) is making progress in this direction.

The transimpedance of the front end amplifier was 1 kΩ. The gain of the second stage amplifier was $A_v = 7$. The maximum transconductance of the laser driver differential pair was 8 mS. The circuit gain was $A_v = 56$.

The optical output power, the DC and differential optoelectronic gains as functions of the optical input power is shown in Fig. 3. The maximum differential optoelectronic gain is 3, and the DC gain is > 2.5. The differential gain is small at low input powers because of the low slope efficiency of the laser near threshold. The decrease of gain at high power is due to non-linearities in the transconductance of the transmitter differential pair. The front end of this circuit does not saturate until the optical input power exceeds 1 mW.
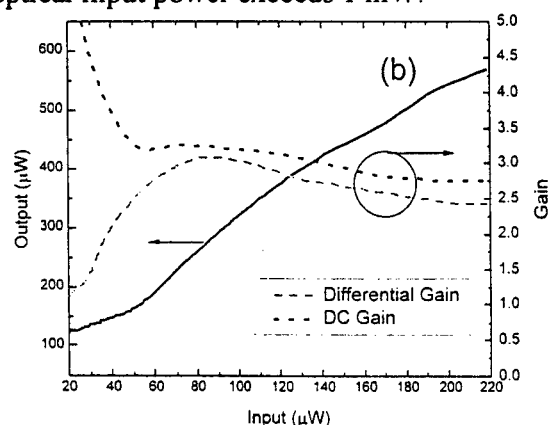
Fig. 3: Optical transfer characteristics of the pixel.

Full OR, NOR, AND and NAND operation of the circuits have been demonstrated, depending on the input diode and output laser configurations used. A circuit 3dB bandwidth of 800 Mb/s has also been measured. Figure 4 shows the BER vs. average input optical power at 670 Mbit/s, using a 2^7 - 1 pseudo random bit stream (PRBS) pattern for

the non-impedance-matched pixel receiver. Taking into account the 4 dB penalty incurred by input loading and post-amplifier noise, an average input power of -19.7 dBm is measured at BER = 10^{-9} and $\lambda = 1.3$ μm. Also, if we "correct" for the 55% quantum efficiency of the non-AR-coated p-i-n photodiode, -19.7 dBm can be decreased to -22 dBm. The eye-diagram of the pixel at -20 dBm input optical power is shown in the inset, corresponding to a switching energy of $E_{sw} = 32$ fJ. The best reported InP-based monolithic p-i-n/HBT photoreceivers have achieved $E_{sw} = 2$ fJ, using more complicated circuits, AR coated detectors, and smaller device dimensions than those used here.
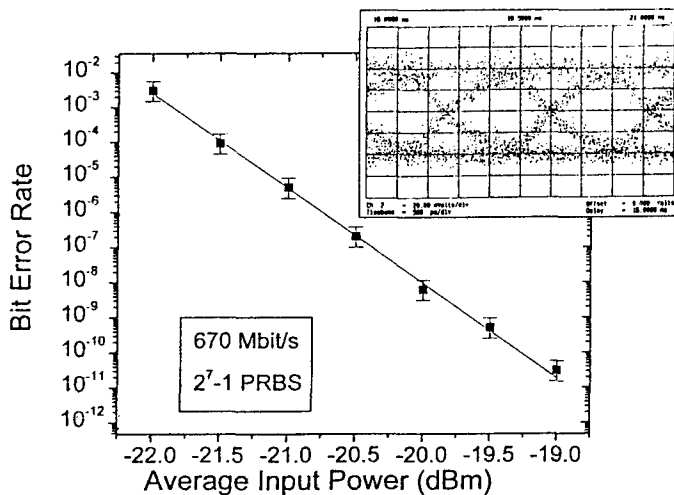
Fig. 4: Sensitivity of the unmatched pixel receiver

IV. Conclusions

The results for our pixel, summarized in Table 2, represent a significant improvement over the performance of optoelectronic smart pixels predicted[2] as recently as 1993. In that work, the performance of the pixel was calculated for NOR gates with a simpler, high-impedance amplifier circuit. Although that design has the potential of achieving high sensitivity, it has lower bandwidth and dynamic range compared to the transimpedance amplifier design used here. Further improvements in switching energy are possible using a more sophisticated receiver circuit or smaller transistor geometry, as demonstrated recently for state-of-the-art monolithic p-i-n/HBT photoreceivers. However, larger circuits may lead to increased pixel size and

power dissipation, thus decreasing the array circuit packing density.

Table 2. Summary of the smart pixel performance

Bandwidth	800 MHz
Sensitivity	-23 dBm
Switching Energy (cascadable)	6.3 fJ
Power Dissipation (w/o laser)	250 mW (30 mW)
Dynamic Range (cascadable)	20 dB (10 dB)
Max. Differential Gain	3
Cascadable DC Gain	≥ 2.5
Front End Transimpedance	1 kΩ
Second Stage Gain	7
Diff. Pair Transconductance	8 mS
Max. HBT gain	≥ 400
p-i-n Quantum Efficiency	55 %

In conclusion, we have described the design, fabrication, and performance of optoelectronic InP/InGaAs smart pixels suitable for use in high density optical interconnects and computing. The circuits consist of monolithically integrated p-i-n/HBT circuit electronics with surface-bonded FCSELs as the output devices. The vertical geometry of the optical input and output devices allows for free space operation, and the $\lambda = 1.3$ μm operating wavelength makes this technology compatible with long-haul fiber optic communication systems.

V. Acknowledgment

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20 GHz HIGH PERFORMANCE PLANAR
Si/InGaAs P-I-N PHOTODETECTOR

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INTRODUCTION

Wafer fused planar Si/InGaAs *p-i-n* photodetectors were fabricated. They show high internal quantum efficiency ($\eta \sim 1$), high speed (21 GHz), record low dark current (100 pA at 4V bias), and no evidence of charge trapping, recombination centers or a bandgap discontinuity at the heterointerface.

Directly bonding[1-4] III-V and Si wafers allow the fabrication of devices which optimize the characteristics of each material. We demonstrate here high performance $\lambda = 1.55$ μm telecommunication *p-i-n* photodetectors on a Si substrate. These devices are then used to investigate the characteristics of the wafer fused Si/InGaAs interface, which are important for both *p-i-n*s and avalanche photodiodes[5,6] (APDs). The planar detectors, consisted of a 24 μm Zn diffused active region in a Si/InGaAs/ InP bonded wafer (shown in Fig.1).

The Si wafer consisted of a 0.5 μm undoped Si epi-layer grown on an n^+ substrate using rapid thermal epitaxy[7]. The III-V wafer was grown on an n^+ InP substrate using low pressure MOCVD (metal organic chemical vapor deposition), and consisted of a 0.3 μm $In_{0.53}Ga_{0.47}As$ (abbreviated InGaAs) stop etch layer, followed by a 0.6 μm InP window layer, and a 1.0 μm InGaAs absorption layer (all undoped). These wafers were fused in an oven at 650° C in flowing H_2 as described previously[5]. After bonding, the InP substrate and the InGaAs etch stop layer were removed.

The DC photocurrent and the reverse dark current were measured as a function of bias voltage from $V_b = 0$ to 10 V (shown in Fig. 2). Note that the photocurrent is constant with V_b even down to zero bias, suggesting that there is no significant charge accumulation or trapping at the interface. Further, the dark current is a record low for Si:III-V bonded wafers, ($I_D = 100$ pA at $V_b = 4$ V), and is in
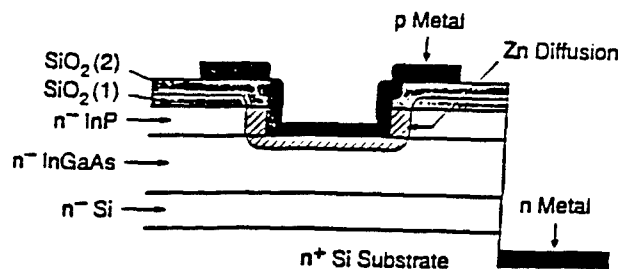
Figure 1.Structure of back illuminated planar Si/InGaAs PIN detector.
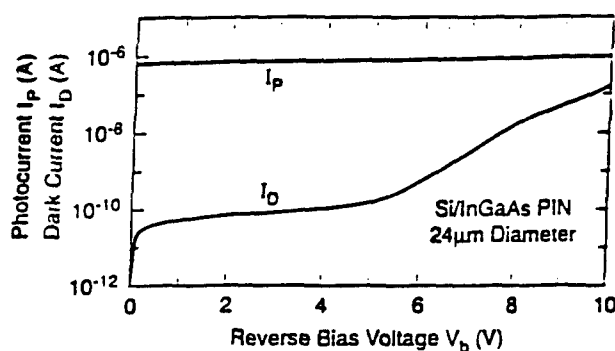
Figure 2.Photocurrent and dark current for a reverse biased Si/InGaAs PIN.

This result clearly demonstrates that there is no measurable loss of photogenerated carriers across the Si/InGaAs, further confirming the nearly ideal interface.

The capacitance was measured as a function of voltage (Fig. 3), and shows a
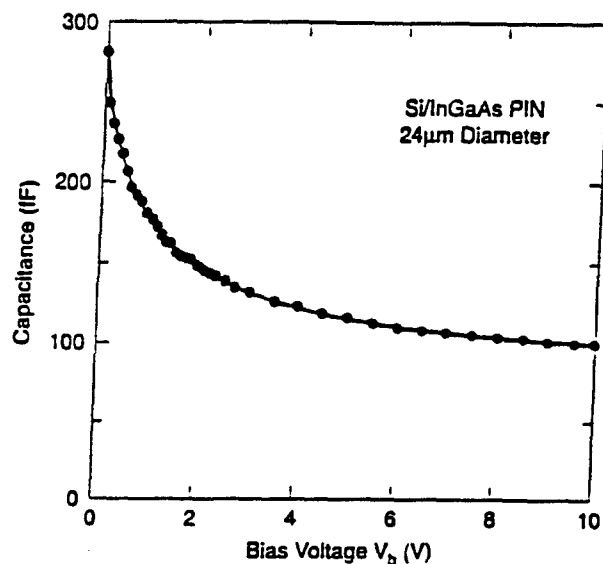
Figure 3.Measured capacitance vs. bias voltage

fact comparable to state of the art InP/InGaAs p-i-ns, again indicating the excellent quality of the interface. Additional support for this conclusion is supplied by forward I-V measurements, which over the range $V_b = 0.1$ to 0.4 V are given by $I = I_0 \, exp(qV/nkT)$, with a near unity ideality factor $n = 1.1$ to 1.2. The absolute value of the quantum efficiency $\eta = \eta_i \eta_a$ (where $\eta_a = 1\text{-}e^{\alpha L}$, is the absorption quantum efficiency, and η_i is the internal quantum efficiency, i.e. the fraction of the photogenerated carriers which are collected) was accurately measured at $\lambda = 1.55$ µm. After correcting for the reflectivity of the incident Si surface, and the thickness of the InGaAs absorption layer, the internal quantum efficiency was determined to be $\eta_i = 100$ % to within the accuracy of our experiment (5 %).

smooth decrease with increasing V_b, with no indication of a change of slope, demonstrating that there is no excess charge at the interface. Combining C = 100 fF (at $V_b = 10$ V) with the measured contact resistance $R_c = 40$ Ω [i.e. a total circuit resistance of R = $(50 + R_c)$ Ω = 90 Ω], results in a calculated RC frequency response of $f_{RC} = 1/(2\pi RC) = 18$ GHz, which is expected to dominate the response speed, since the transit time limited frequency is calculated to be $f_T = 38$ GHz. The measured 3 dB bandwidth which was found to be 21 GHz, is shown in Fig. 4. This good agreement with f_{RC}, again demonstrates that there is no trapping at the interface due to either defects or a hetero-bandgap ΔE_c discontinuity. Thus, the Si/InGaAs interface seems nearly ideal not

484

Si/InGaAs PIN
24μm Diameter
λ = 1.55μm
V_b = 10V

indication of trapped charge at the interface, the internal quantum efficiency is ≈ 100%, the high speed response is RC limited at 21 GHz, and the photocurrent noise is close to the minimum shot noise limit. All these measurements demonstrate that there is no significant charge trapping, recombination centers, or bandgap discontinuity ΔE_c at the heterointerface and thus, that the Si/InGaAs interface is nearly ideal. This indicates that record performance, high gain-bandwidth, low dark current APDs can be expected.

only in the lack of any defects or charge trapping, but also in having a small discontinuity ΔE_c ≈ 0.

As a final characterization of the interface, we measured the absolute photocurrent noise power[8] using a noise figure meter at a frequency of 30 MHZ and a bandwidth of 4 MHZ. The current noise power is linear in I_p, as expected, with a slope of 3.4×10^{-3} kT/μA in good agreement with the minimum shot noise limit of $2qRI_p/kT = 3.9 \times 10^{-3}$ kT/μA, (for R = 50 Ω); thus, showing no excess noise and no evidence of traps.

In addition, we have also done a detailed study of the wafer bonding process. Wafers were bonded at various temperatures from 650^0 C to 475^0 C and differing amounts of H_2 and N_2. The reverse biased dark current was found to increase with decreasing temperature, while the forward biased current indicated that tunneling through a thin interface high bandgap layer was important. The quantum efficiency, however, remained near unity for all the bonded samples.

In conclusion, we have fabricated and measured novel planar Si/InGaAs *p-i-ns*. We find that the photocurrent is flat with voltage down to V_b = 0, the reverse bias dark current is extremely low (100 pA at V_b = 4 V), the forward bias current has an ideality factor n near unity, the capacitance $C(V_b)$ shows no

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485

WAVEGUIDE AlInAs/AlGaInAs AVALANCHE PHOTODIODE FOR 20 Gbit/s PHOTORECEIVERS

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Introduction

High speed photodetectors are needed in optical communication systems and avalanche photodiodes are essential in highly sensitive photoreceivers at the 1.55 μm wavelength. Avalanche photodiodes (APDs), when compared to PIN photodiodes, provide higher responsivities due to their internal gain M. An improvement in the signal to noise ratio of about 10 dB is expected at 20 Gbit/s. Very good performances have already been demonstrated at 10 Gbit/s [1]. For higher bit-rates, a side-illuminated structure has been proposed [2], to reach simultaneously high responsivity and high speed. The simulations allowing to design waveguide APD structures, their fabrication and their characteristics are reported in this paper.

I. APD design

A. Electrical simulations:

The frequency response of an APD with separate avalanche and multiplication region is plotted on figure 1 as a function of the multiplication factor M for different absorption thicknesses. The calculation, as described for example in [3], is based on the following assumptions: (i) electron-hole pairs are generated homogeneously in the absorption layer which is a good approximation for side-illuminated photodiode with thin absorption layer, (ii) electrons and holes drift towards the contact layers at saturation velocities v_n and v_p . The multiplication layer thickness is 0.25 μm, as determined from previous work [4]. The degradation of the frequency response originates from both the carrier transit time through the active layers and the multiplication process. To achieve 20 GHz bandwidth at a multiplication factor of 5, the GaInAs absorption layer must be reduced to less than 0.3 μm.
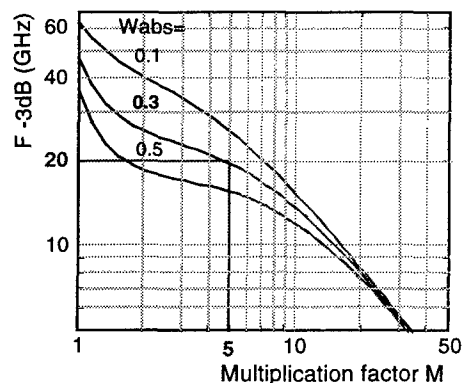
fig. 1: Frequency response of an APD versus M for InGaAs thicknesses of 0.1, 0.3 and 0.5 μm.

The multiplication process becomes possible when the electric field in the different regions is well distributed. To get a high electric field in the avalanche layer together with a low electric field in the absorption layer, it is necessary to insert a field buffer layer. Figure 2 shows the electric field distribution versus thickness for a structure with or without a field buffer layer. Calculations are based on Poisson and current continuity equations. The structure with no field buffer layer provides high dark current and low multiplication. Indeed, a high field in the low band-gap energy InGaAs region

generates a high tunnel current while the field in the avalanche region is not adequate to provide the carrier multiplication.
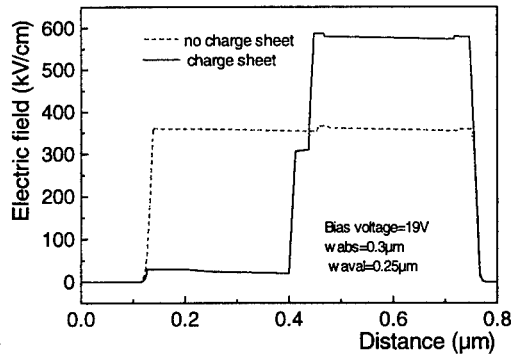
fig. 2: Electric field distribution versus position across the structure of an APD with and without a field buffer layer.

These simulations allow to design an APD with both a high bandwidth and a suitable gain M.

B. Optical simulations:

Because of the side-illumination, the APD is considered as a waveguide structure where the InGaAs layer is the waveguide core. AlInGaAs Optical cladding layers are added around the active layers. To match the propagating field of the WG-APD to the input optical beam for optimal coupling efficiency, it is necessary to optimize the cladding layer thicknesses. Simulations use mode calculations, overlap integral calculations and confinement factor for responsivity [5]. The responsivity formula used is expressed by:

$$S(A/W) = \frac{\lambda}{1.24}(1-R)\sum_i \eta_{ci}\left(1-exp\left(-\Gamma_i\alpha_{abs}\frac{n_{abs}}{n_{ieff}}L\right)\right) \quad (1)$$

where η_{ci}, Γ_i, α_{abs}, n_{abs}, n_{ieff}, R, L and λ are the overlap integral between the ith-order mode and the input beam, the confinement factor of the ith-order mode in the InGaAs layer, the InGaAs absorption coefficient, the real part of the InGaAs refractive index, the effective index of the ith-order mode, the power reflection loss at the facet, the diode length and the wavelength.

Figure 3 shows the calculated coupling efficiency between a 3µm spot size diameter gaussian beam

and the APD as a function of bottom cladding layer thickness. When increasing the thickness, higher-order modes appear in the structure leading to a coupling efficiency higher than 80%.
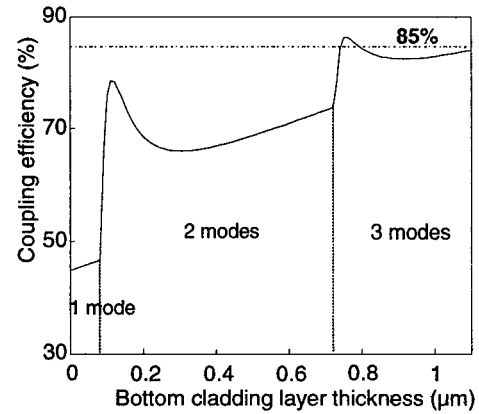
fig. 3: Coupling efficiency as a function of the bottom cladding layer thickness.

Figure 4 represents the TE guided modes and the responsivity in the y direction (see fig. 5) of a multimode structure. The structure is assymetric: the fundamental mode is mostly confined in the absorption layer, it is absorbed in a few microns and is also the main contribution to the coupling efficiency. The total optical field in the structure is all the more well matched with higher-order modes. The expected responsivity (at M=1) is 0.9 A/W for a 20 µm long device at 1.55 µm wavelength and with a 3 µm spot size lensed fiber.
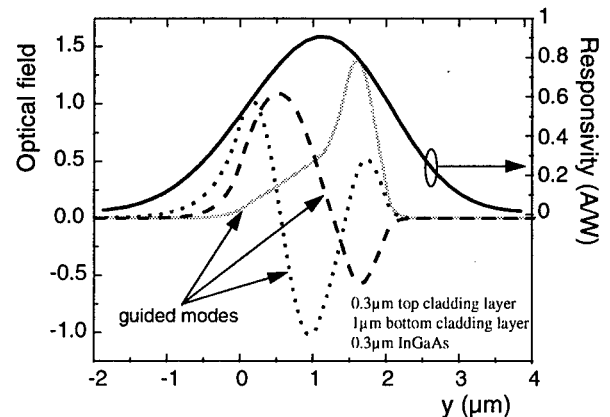
fig. 4: TE modes and responsivity (M=1) versus y for a 20 µm long WG-APD (0 µm=InP substrate interface)

II. Fabrication

The epitaxial layers were grown by molecular beam epitaxy (MBE) on InP-n+ substrate. After an AlInAs buffer layer, they comprise a n+- AlGaInAs bottom cladding layer, an undoped AlInAs/AlGaInAs superlattice multiplication layer, a p-type field buffer layer, an undoped GaInAs absorption layer, a p+- AlGaInAs top cladding layer and a p++- GaInAs contact layer. After delineation of the waveguide, achieved by a combined dry and wet etching, p and n-type ohmic contacts are formed by alloying MnAu and AuGeNi respectively. Silicon nitride is used for the passivation of the devices. The WG-APD schematic cross section is shown in figure 5.
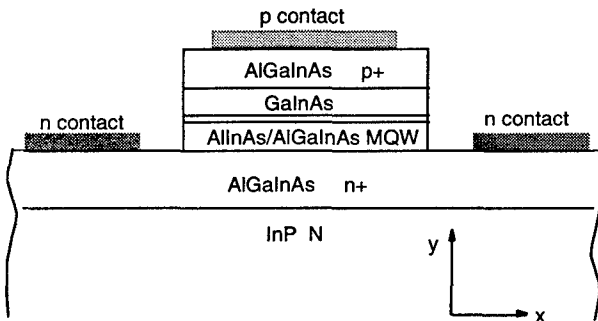
fig. 5: Description of the waveguide APD structure.

III. Results

10×30 μm² devices exhibit very low capacitances of 50 fF, when the absorption layer is fully depleted, and dark current under 1μA.

Some Dark current measurements as a function of reverse bias as a parameter of temperature allow to investigate the different current origins in the APD. Figure 6 represents the measured dark current versus bias voltage for different temperatures. The breakdown voltage (right bottom inset) is higher when increasing the temperature which confirms the multiplication factor decrease with temperature for a fixed high bias [6]. The activation energy Ea can be deduced from the slopes of the dark current characteristic in logarithm scale versus inverse temperature for several bias voltages. Ea decreases with increasing voltage. It is due to the generation current first in the avalanche region (at low voltage

(Ea=0.47eV at 5V) and secondly in the InGaAs region at higher voltage (Ea=0.33eV at 15V).
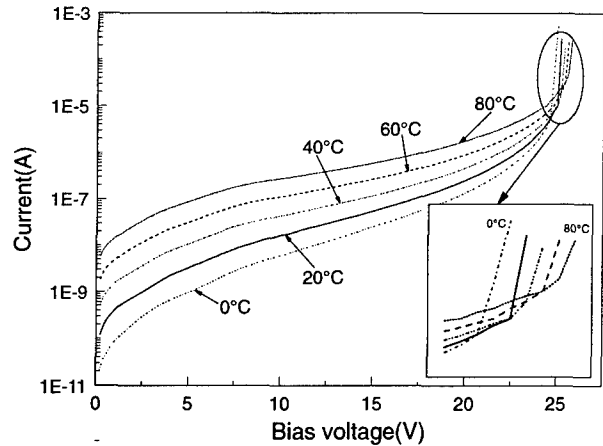
fig. 6: Dark current as a function of bias voltage for temperatures of 0, 20, 40, 60 and 80°C.

The determination of the multiplication factor M is of prime importance to evaluate the performances of the avalanche photodiodes. The M versus bias voltage characteristic has been obtained from shot noise measurement under illumination since it is not precisely obtained from the current versus bias measurement. The noise power density formula is [7]:

$$S_i = 2qI_pM^{(2+x)} \qquad (2)$$

From the noise power spectral density measurement at 10 MHz versus photocurrent, plotted on figure 7, the primary photocurrent is obtained and gives accurately the unity value of the gain.
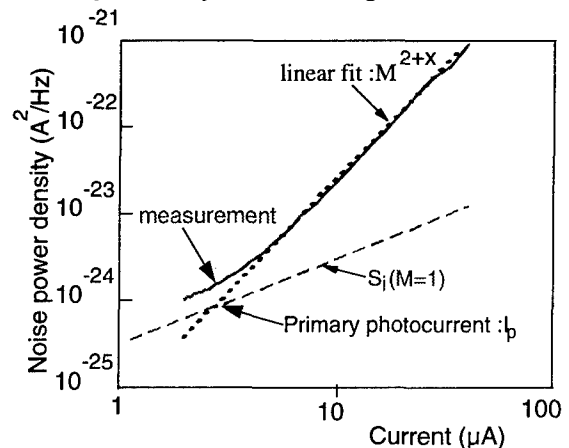
fig. 7: Primary photocurrent determination from noise power density measurement.

488

M values over 10 are measured. From this measurement, a low excess noise factor of 4.5 is deduced at M=10.

From on-probe frequency measurements at different biases (on 50 Ω), the 3 dB bandwidth is plotted versus M in figure 8. A 3 dB bandwidth over 20 GHz is measured at M=3.2 and a gain-bandwidth product over 160 GHz is extrapolated at higher gain.
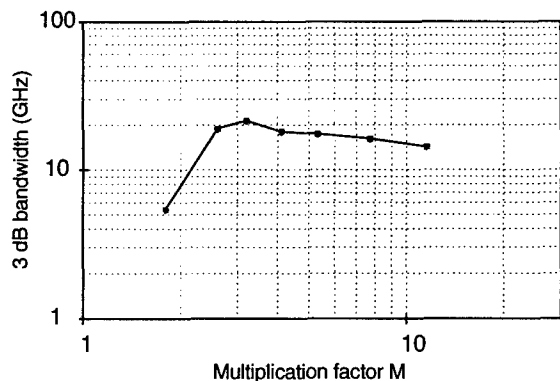
fig. 8: Measured 3-dB bandwith (on 50Ω) versus multiplication factor M.

Optical measurements of the APD responsivity have also been made with a lensed fiber (3 μm spot size). Figure 9 shows the measured responsivity as a function of the applied bias. A very high responsivity of 10 A/W is obtained: this result confirms the high potential of the waveguide avalanche photodiode approach as well as the multiplication factor determination.
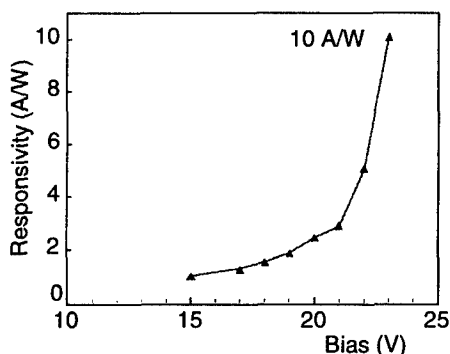
fig. 8: Measured responsivity versus bias.

IV. Conclusions

Side-illuminated waveguide AlInAs/AlGaInAs superlattice avalanche photodiodes have been designed and fabricated. These devices exhibit state of the art bandwidth (> 20 GHz) and gain-bandwidth product of 160 GHz, and are suitable for 20 Gbit/s operation. Concerning optical measurements, a high responsivity of 10 A/W was obtained for the first time for a WG-APD.

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High-speed InGaAs-based Vertical Schottky Barrier Photodetectors

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Introduction

High-speed photodetectors that possess good sensitivity are required for high-speed fiber optic communication receivers, optical data links, and sampling systems [1]-[2]. The vertical Schottky barrier (VSB) photodetector is capable of achieving extremely high bandwidths [3] and high responsivities [4]-[5]. To minimize the difficulty of coupling optical radiation into the device and to avoid complex and expensive packaging techniques, front-illumination is typically employed [3]-[7]. A transparent and low-resistivity Schottky contact material is required in the VSB in order to simultaneously obtain high responsivity and high bandwidth. Previously, a 10 nm thick layer of semi-transparent Au on n^--InAlAs has been used to realize 0.42 A/W InGaAs-based VSB photodetectors [7], and a 100 nm thick film of transparent indium-tin-oxide (ITO) on n^--GaAs has been used to realize 0.40 A/W GaAs-based VSB photodetectors [3], [6]. Although the 10 nm thick layer of Au is semi-transparent, the opacity of Au limits the responsivity. Therefore, it is important to investigate the potential of transparent conductors as an electrode material for VSB photodetectors.

In this work, we report on the design, fabrication, and characterization of an InGaAs-based VSB photodetector that uses a lattice-matched n^--InAlAs Schottky barrier height enhancement layer in conjunction with a 320 nm-thick film of ITO to form a high quality transparent Schottky contact. The Schottky barrier height of ITO on n^--InAlAs was determined to be 0.68 eV through the use of Norde plots and I-V measurements. The thin film of ITO and the device passivation layer of silicon nitride, together, form an odd-multiple quarter-wave transformer to 1.31 μm perpendicularly incident light. The devices exhibited very low dark current densities, high responsivities, and high 3-dB bandwidths. A dark current per unit area of $8.87 \cdot 10^{-5}$ A/cm^{-2} at an applied bias of 5 V was obtained. The responsivity for all the devices tested ranged from 0.55 to 0.59 A/W at a wavelength of 1.31 μm. The 15 μm diameter devices exhibited 3-dB bandwidths of 19 and 25 GHz in response to 1.55 μm illumination with an applied bias of 5 and 10 V, respectively.

I. Design and Fabrication

The InAlAs/InGaAs lattice-matched epitaxial layers were grown by organo-metallic vapor phase epitaxy (OMVPE) on top of a (100) InP:Fe substrate. The layer structure consists of a 25 nm InP:Fe buffer layer, followed by a 300 nm n^+-InP:Si ($6 \cdot 10^{18}$ cm^{-3}) ohmic contact layer, a 1.0 μm InGaAs absorption layer, a 50 nm In(Ga, Al)As graded layer, and finally, a 50 nm InAlAs Schottky barrier height enhancement layer. All of the epitaxial layers, with the exception of the n^+-InP:Si layer, were unintentionally doped with a background concentration between 10^{15} to 10^{16} cm^{-3}. Since the barrier height of most metals on In$_{0.53}$Ga$_{0.47}$As is very low, between 0.2 and 0.3 eV, a Schottky barrier height enhancement layer was used to reduce leakage current due to carrier injection across the barriers. A graded layer is incorporated to reduce the conduction and valence band discontinuities at the interface between the Schottky height enhancement layer and the

490

absorption layer. The band edge discontinuities can impede carrier motion and trap carriers resulting in a degradation of the frequency response and the introduction of uncontrollable dc and rf gain (8).

A schematic of the device prior to the application of an antireflective and passivating coating of SiN_x is shown in Fig. 1. An anisotropic active area mesa profile was formed by using a highly selective etchant composed of citric acid and H_2O_2. The removal of the n^+-InP layer for device isolation purposes, was performed using a selective etchant consisting of H_3PO_4, HCl, and CH_3COOH.

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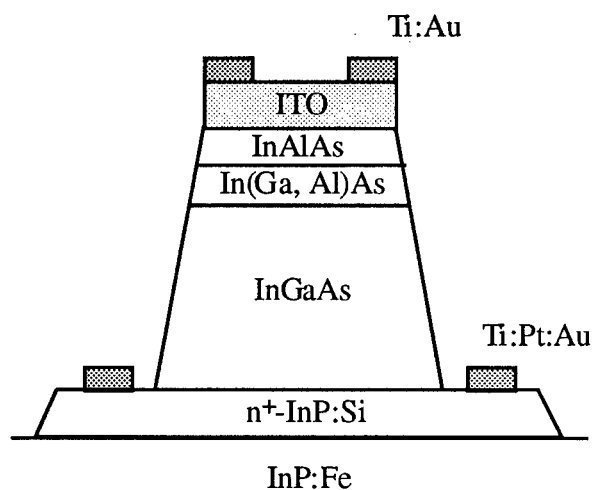
Fig. 1: A schematic of the VSB photodetector.

An rf magnetron-sputtered film of indium-tin-oxide (ITO) which possesses low resistivity and high transparency (9) was used to form the Schottky barrier contact. The refractive index of this film was determined to be approximately 2.05 which is very similar to the refractive index of the plasma-enhanced chemical vapor deposited (PECVD) film of Si_3N_4. The refractive index of this PECVD film is 1.95. In order to obtain good step coverage and to form an antireflective coating to perpendicularly incident 1.31 μm optical radiation, the thickness of the ITO and Si_3N_4 were chosen to be λ/2 and 3λ/4 corresponding to nominal thicknesses of 320 nm and 500 nm, respectively. The spectral transmission characteristics of an ITO film deposited on a Corning 7059 substrate are displayed in Fig. 2. The transparency of the

film is in excess of 85% over most of the spectral range.
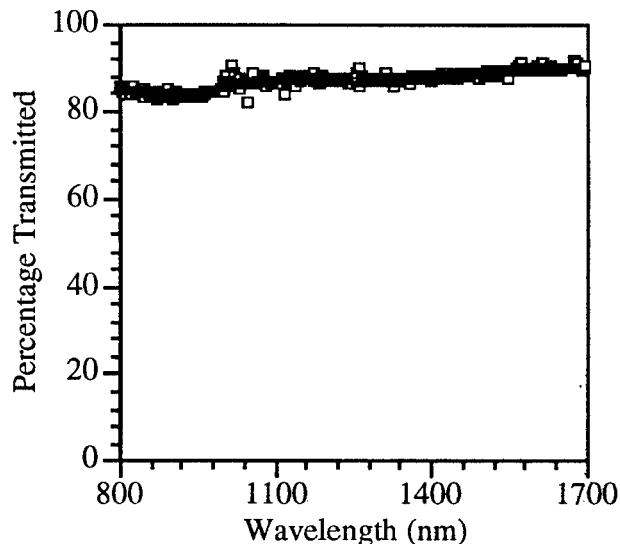
Fig. 2: Percentage of optical power transmitted through an ITO film.

Dry etching in a CH_4:H_2 plasma was used to define the ITO contact (10). The resistivity of the ITO contact was decreased and the quality of the Schottky contact was improved by performing a postetch anneal of the sample (11). The Schottky barrier height of ITO on $In_{0.52}Al_{0.48}As$ was determined, from current-voltage measurements and current-voltage-temperature measurements using modified Norde plots, to be 0.677 and 0.674 eV, respectively. The ideality was determined to be 1.12 from current-voltage measurements. An annular contact ring of Ti:Au (20:180 nm) was formed on top of the ITO to reduce the series resistance of the Schottky contact. This metallization was also used to extend a contact from the ITO, at the top of the mesa, down the passivated mesa sidewall to a microwave contact pad. The nonalloyed ohmic contacts to the n^+-InP:Si where formed using Ti:Pt:Au (20:10:170 nm). The nonalloyed ohmic contact resistance and sheet resistance was 0.030 Ω•mm and 19.7 Ω/□, respectively. The ohmic metallization was also used to form the microwave contact pads. A scanning electron micrograph (SEM) image of a completed VSB photodetector with a diameter of 25 μm is displayed in Fig. 3. The horseshoe-shaped ohmic contacts and the Schottky contact stripe are connected to microwave contact pads in a

491

ohmic contacts and the Schottky contact stripe are connected to microwave contact pads in a ground-signal-ground configuration with a center-to-center spacing of 150 μm.
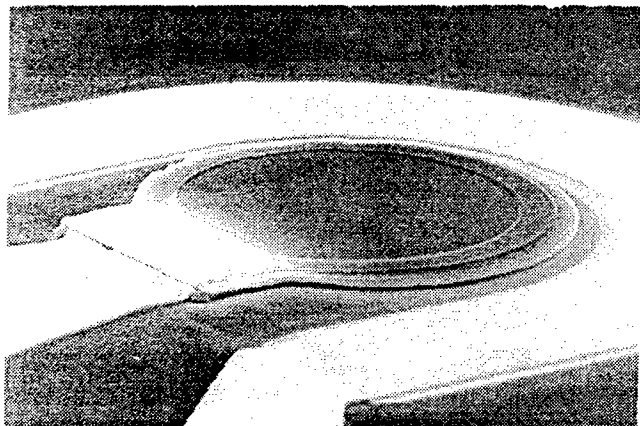
Fig. 3: A scanning electron micrograph of a completed 25 μm diameter VSB photodetector.

II. Results

The dark current characteristics for various devices is displayed in Fig. 4. The dark current at an applied bias of 5 V was 1.41, 3.09, and 7.27 nA for the 15, 50, and 100 μm devices, respectively. The dark current per unit length of the perimeter of the active region mesa ($I_D/2\pi r$) was found to be virtually identical for all the devices, approximately $1.7 \cdot 10^{-3}$ A/cm^{-1}, while
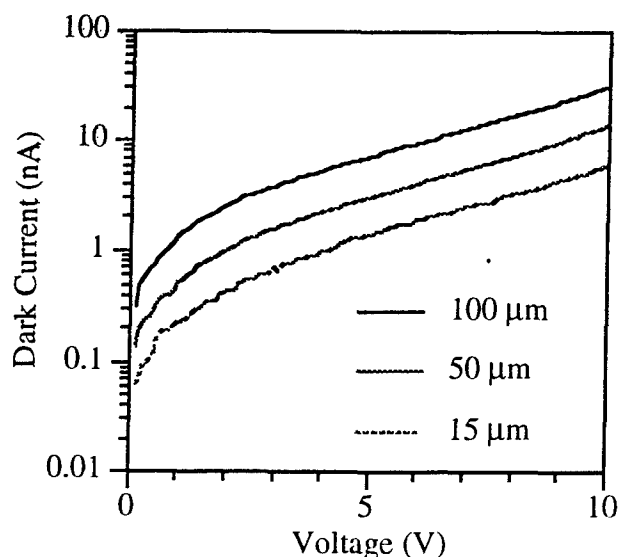
Fig. 4: The dark current of VSB photodetectors with various active region diameters.

the dark current per unit area ($I_D/\pi r^2$) of the Schottky contact was found to increase as the diameter of the devices was decreased, where I_D is the dark current and r is the radius of the active region mesa. This suggests that the dark current in these devices is predominantly due to surface-state conduction along the periphery of the mesa instead of conduction across the Schottky barrier contact. The 100 μm diameter devices exhibited the lowest dark current densities of $8.87 \cdot 10^{-5}$ A/cm^{-2} for an applied bias of 5 V.

The responsivity of all the devices was found to be between 0.55 and 0.59 A/W at a wavelength of 1.31 μm and with an applied bias of 5 V. The responsivity versus voltage is displayed in Fig. 5. The responsivity is virtually independent of voltage in the saturation regime indicating that uncontrollable dc gain is low in these devices (8).
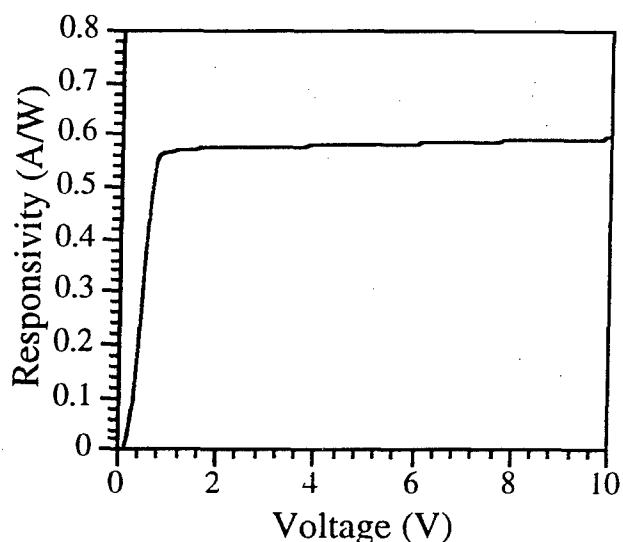
Fig. 5: The responsivity of a 100 μm diameter VSB photodetector to 1.3 μm light.

The frequency response of the photodetectors was determined from modulated-frequency measurements using an HP83420A lightwave test set at a wavelength of 1.55 μm. The response was measured into a 50 Ω characteristic impedance. The frequency response of 100, 50, and 15 μm diameter VSB photodetectors, with an applied bias of 5 V, is displayed in Fig. 6. The bandwidth of these devices, for an applied bias of 5 V, was found to

492

be 2.2, 7.8, and 19.0 GHz for the 100, 50, and 15 μm diameter devices, respectively.
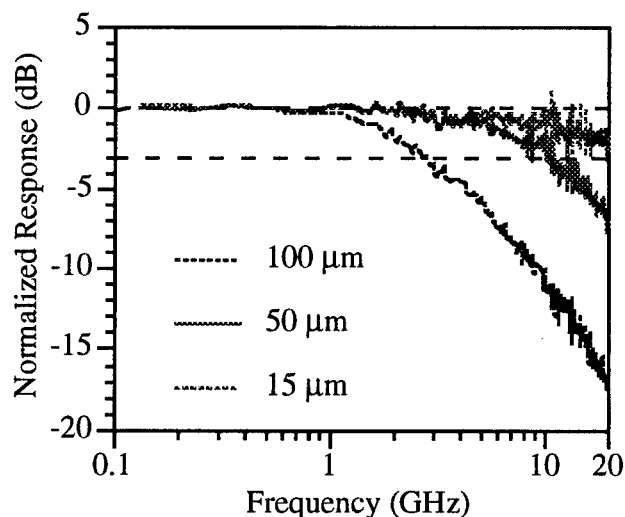
Fig. 6: The frequency response of VSB photodetectors with various active region diameters.

The bandwidth of these devices was improved by increasing the applied bias from 5 to 10 V. This is a direct result of increased carrier velocities which causes a reduction in the average carrier transit times. Higher biases were not applied to these devices during the bandwidth measurements because the dc breakdown voltage of these devices is between 10 and 15 V. The bandwidth of the VSB photodetectors biased at either 5 or 10 V is displayed in Fig. 7. Since the measurement system is calibrated only up to 20 GHz, the frequency response of the devices were fit to a single pole linear system and the 3-dB bandwidth was approximated from these curve fits.

III. Summary

We have designed, fabricated, and characterized a high speed and high responsivity vertical InGaAs-based Schottky photodetector that utilizes a lattice-matched InAlAs Schottky barrier height enhancement layer and a film of ITO to form both a Schottky contact and an antireflective coating to 1.31 μm optical radiation. High responsivities of up to 0.59 A/W were obtained in conjunction with dark current densities below $1 \cdot 10^{-4}$ A/cm^2 and 3-dB bandwidths of 25 GHz.
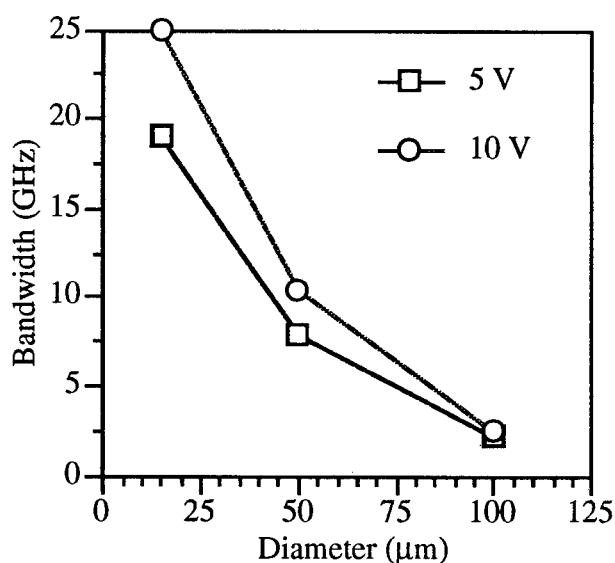
Fig. 7: The bandwidth of VSB photodetectors with various active region diameters.

IV. Acknowledgments

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HIGH BANDWIDTH InP/InGaAs BASED MSM-2DEG DIODES FOR
OPTOELECTRONIC APPLICATION

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Introduction

In this work the electrical and optoelectronic behavior of InP/InGaAs based MSM diodes above a two dimensional electron gas is investigated. The electric field distribution of this MSM-2DEG device is modified by the two dimensional electron gas, leading to improved performance compared to a conventional MSM diode. An InGaAs layer between the Schottky metallization and the two-dimensional electron gas (2DEG) acts as absorption region for 1.3 to 1.55 µm wavelength light. This wavelengths are used for long distance glass fiber communication systems. The substitution of the conventionally used InAlAs by InP avoids the problems related to aluminum (ageing, DX centers, lack of etch control). Photodetectors have been fabricated with responsivities up to 0.61 A/W, at 1.3 µm wavelength. RF-optimized devices show bandwidths up to 16 GHz, which is, to the authors' knowledge, the highest bandwidth reported for MSM photodetectors at this wavelength.

I. The MSM-2DEG Diode

Metal-semiconductor-metal diodes with inter-digitated electrodes are widely used as fast photodetectors [1-6]. In this work the influence of a 2DEG on the performance of an InGaAs/InP based MSM detector is reported. This device, that we call MSM-2DEG diode, consists of two Schottky contacts on an inverted HEMT layer structure, with an InGaAs absorption layer between the contacts and the 2DEG [7].

The introduction of a 2DEG layer into the MSM structure has two reasons. The first is the modification of the electric field to improve the device performance compared to the conventional MSM photodetector. [8]. The second aim is to make the photodetector compatible to HEMT fabrication without need of a second epitaxial growth step.

The 2DEG with its high sheet carrier concentration (typically in the order of 1 to $2*10^{12}$ cm^{-2}) acts as an equipotential plane which forces the electric field mainly perpendicular to the surface and below the Schottky contacts in contrast to the conventional

MSM diode where the field extends between the metallizations. Fig. 1 shows the different potential distributions of the two devices. This difference changes the electrical as well as the optoelectronic DC and RF behavior.
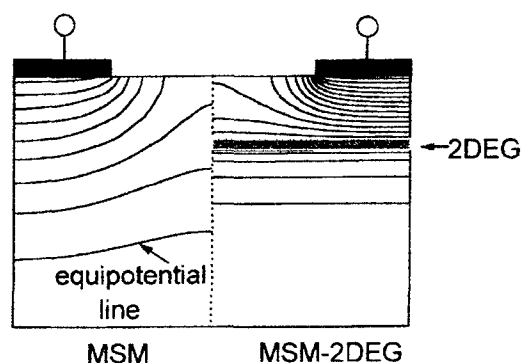
Fig. 1: Calculated potential distribution of the MSM-2DEG diode compared to the conventional MSM device [7]

II. Device fabrication

The layer system is grown by low pressure MOVPE with nitrogen as carrier gas on (100) oriented semi-insulating InP wafers (InPACT) with low etch pit densities (EPD<$3*10^4$ cm^{-2}). Low EPD's are of great importance for the device performance. Hall measurements yield 2DEG concentrations of typically $1.7*10^{12}$ cm^{-2} and electron mobilities of about 12000 cm^2/Vs. The nitrogen based epitaxial process reduces fabrication costs, increases the layer homogeneity and enhances the process safety, compared to the commonly used H$_2$ carrier gas [9]. The conventionally used InAlAs high bandgap material is replaced by InP to avoid the Al-related problems (ageing, DX centers, lack of etch control). The low Schottky barrier on InGaAs is enhanced by a p-doped InP surface layer [10]. A typical layer sequence is shown in Fig. 2.

15nm p-InP 1.5E18cm-3	barrier
15nm InP	enhancement layers
125..500nm InGaAs	absorption layer
10nm In(x) Ga(1-x)As	channel, x=77%
5nm InP	spacer
7nm n-InP 2E18cm-3	carrier supply
300nm InP	buffer
semi-insulating InP substate	

Fig. 2: Typical layer sequence of an MSM-2DEG diode

The fabrication process consists of standard optical lithography, metal evaporation and lift-off. The mesa to insulate the devices is performed by reactive ion etching and subsequent wet etching with a citric acid based solution. The sub-µm fingers are defined by electron beam lithography. A 10 nm thick Platinum layer forms semi-transparent Schottky contacts with a transparency of 90%. A 150 nm thick Pt layer is used for opaque contacts. The sides of the mesa are insulated by polyimide. The pads (Cr/Au) are performed as final step.

III. Electrical behavior

The current-voltage behavior of a conventional MSM device can be described by an anti-series circuit of two Schottky diodes. The current is mainly determined by the reverse-biased diode. A barrier-enhanced Schottky contact with voltage-dependent barrier height shows a pronounced voltage dependence of the reverse current. At the MSM-2DEG device, however, the applied voltage forces the depletion region of the reverse biased contact into the channel below this contact. As a consequence the channel resistance increases and the reverse current becomes almost voltage independent [7]. Fig. 3 depicts this behavior for devices with a pronounced voltage dependence of the Schottky barrier.
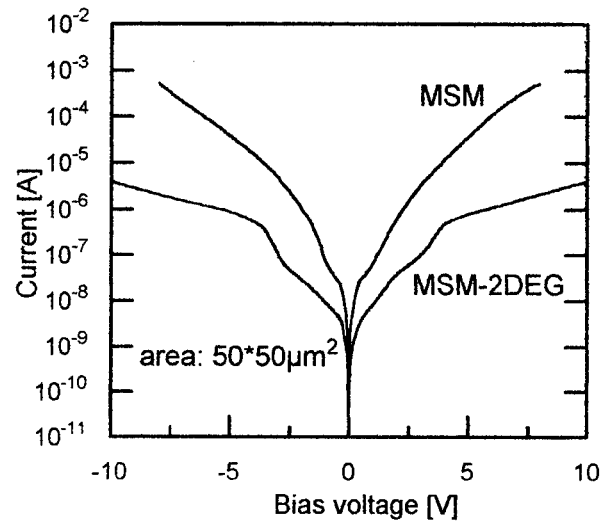
Fig. 3: Influence of the two dimensional electron gas on the current-voltage characteristics

The breakdown voltage of the devices depends on the finger spacing. It is 20V at 0.8 µm spacing and increases to 33 V for 3 µm. There is no significant difference between devices with and without 2DEG.

The capacitance of the diode is modified by the 2DEG. The depleted 2DEG layer acts as a capacitance that lies in series to the Schottky contact capacitance [7]. This 2DEG capacitance

increases with increasing distance of the channel layer to the surface [11]. Fig. 4 shows the measured capacitance of the MSM-2DEG diode as function of the finger geometry and the absorption layer thickness d_a. The values are slightly smaller than for conventional MSM devices.
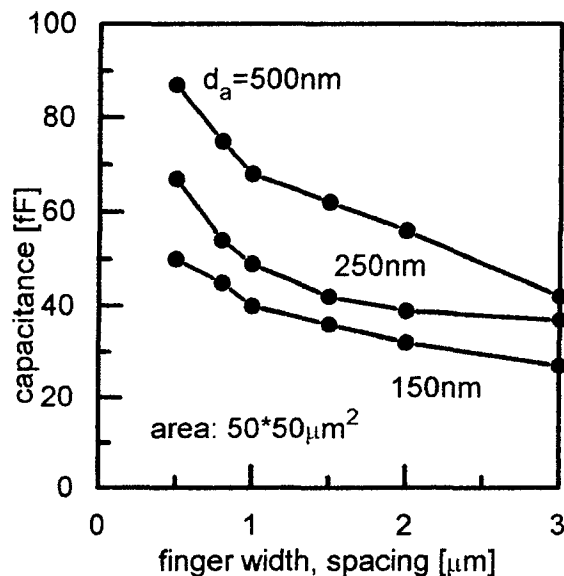
IV. Optoelectronic results

Fig. 4 Capacitance of the MSM-2DEG diode

Optoelectronic measurements are performed at 1.3 μm wavelength. A laser beam is directed to the photodetector by a glass fiber. For RF measurements the beam is RF modulated at frequencies between 130 MHz and 20 GHz by using a Mach-Zehnder interferometer of a HP83420A lightwave test set. The optoelectronic RF response is measured with an HP8510B network analyzer.

A disadvantage of a conventional MSM photodetector compared to a pin device is the shadowing of part of the active area by the Schottky contacts, which reduces the responsivity. One attempt to solve this problem is the use of transparent contacts or backside illumination to enhance the DC responsivity [2,3]. Unfortunately the bandwidth decreases due to photo-generation of carriers in the region of low electric field below the electrodes. A 30-50 % bandwidth reduction has been reported.

Introduction of a 2DEG channel increases the electric field strength below the contacts. Fig. 1 shows the potential distribution of this MSM-2DEG device. MSM-2DEG photodetectors were fabricated with opaque and with semitransparent Schottky contacts. A device with a 500 nm thick absorption layer and opaque contact fingers with width and spacing of 2 μm, respectively, shows a DC responsivity of 0.39 A/W at 1.3μm wavelength, and a 3 dB bandwidth of 8.5 GHz. A semitransparent Schottky metallization increases the responsivity to 0.61 A/W, without reducing the bandwidth.

The finger spacing of the MSM-2DEG should be reduced to sub-μm dimensions to increase the electric field in the region between the Schottky contacts. A high electric field and a thin absorption layer are necessary to increase the bandwidth of the photodetector.

The frequency response of MSM-2DEG devices with finger width and spacing of 0.5 μm and with different absorption layer thicknesses is depicted in Fig. 5. As expected, a thinner absorption layer gives a lower response, but a higher bandwidth.
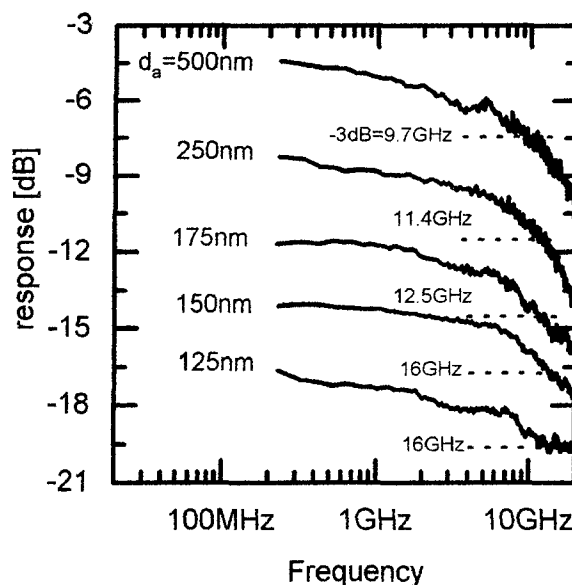
Fig. 5: Frequency response of MSM-2DEG photodetectors for different absorption layer thicknesses d_a. Finger width and spacing: 0.5 μm Optical power: 5 μW, wavelength: 1.3 μm 0 dB: 1 A/W

496

Fig. 6 shows the dependence of the bandwidth on the finger geometry, for different absorption layer thicknesses. For great finger spacing the bandwidth is transit time limited. The bandwidth increases with decreasing finger width and spacing until a saturation occurs. This saturation can be attributed to RC limitation of the bandwidth. Reduction of the absorption layer thickness reduces the 2DEG capacitance and therefore increases the RC-determined bandwidth.
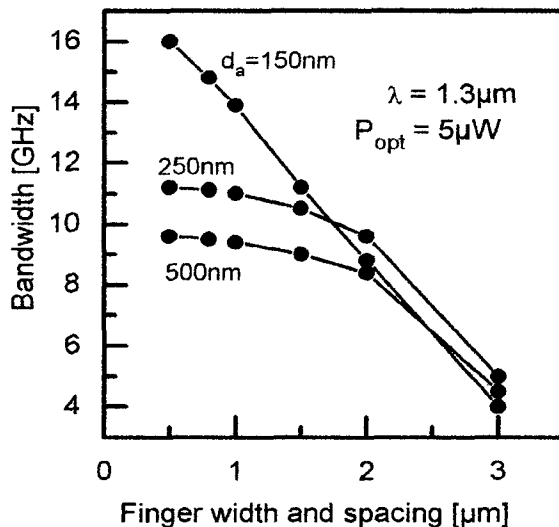
Fig. 6: Bandwidth as a function of finger geometry and absorption layer thickness d_a

Table 1 gives characteristic values of the MSM-2DEG device and of published MSM detectors at 1.3 µm wavelength.

Table 1: DC responsivity and bandwidth of MSM photodetectors, measured at 1.3µm wavelength

	Responsivity [A/W]	Bandwidth [GHz]	Reference
MSM	0.35	11	[1]
MSM	0.96	4.7	[2]
MSM	0.76	6	[3]
MSM	0.39	4.5	[4]
MSM	0.3	8.4	[5]
MSM	0.39	13	[3]
MSM	0.27	9.6	[6]
MSM-2DEG	0.61	9.6	this work
MSM-2DEG	0.21	16	this work

V. Conclusions

The electrical and optoelectronic properties of InP/InGaAs based MSM photodetectors are improved by introduction of a 2DEG, using an inverted HEMT layer structure. The 2DEG reduces the dark current of the barrier enhanced diode and allows a transparent or semitransparent Schottky metallisation without degradation of the optoelectronic RF properties. A responsivity-optimized device with 500 nm absorption layer has a DC responsivity of 0.61 A/W and a bandwidth of 9.7 GHz. The responsivity exceeds published values of MSM-detectors with similar bandwidth [5,6]. An RF-optimized photodetector shows a bandwidth of 16 GHz and a DC responsivity of 0.21 A/W. The high bandwidth and the thin absorption layer thickness of 150 nm make this device useful for integration in HEMT circuits [8].

Further improvement of the device performance is expected by reducing the device area of $50*50\mu m^2$.

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14 May 1997

A Flexible 3-Inch Fabrication Line for InP-Based HEMT and HBT MMIC Production

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Introduction

We discuss the issues related to fabrication of InP based MMICs for government and commercial production applications. InP based MMICs offer unique advantages for many government systems which include lower noise figure, lower DC power consumption and higher linearity. Under the MAFET program, TRW is bringing both InP HEMT and InP HBT-based MMICs from a R&D state into production capability. Manufacturing issues will be addressed from a critical node point of view, where critical nodes are defined as those process steps with the greatest impact on the MMIC performance and yield.

I. Background

InP-based MMICs have been researched and developed at TRW for over 10 years. The performance advantages relative to GaAs based MMICs will only be fully realized when they can be repeatably and reliably designed, fabricated and assembled into systems. This paper focuses on the wafer manufacturing aspects of both InP HEMT and InP HBT-based MMICs. Our approach has been to transition the 2-inch R&D processes to 3-inch production processes while transforming the fabrication laboratory from an R&D focus to a production mode. The transition from R&D to production takes advantage of the >15 years experience at TRW in GaAs MMIC production and process transfers [1].

There are two key aspects to this transition. First, common processes are utilized wherever possible to reduce the overall number of distinct steps. This modular approach adds enormous flexibility to a multi-technology production line. It increases the throughput volume of a specific process, providing more process stability, simpler maintenance and expandibility. Second, Statistical Process Control (SPC) techniques are applied to not only determine the current health of the process, but also to drive process improvements.

II. InP MMIC Production

The overall InP wafer production flow for both HEMT and HBT MMICs is shown in Fig. 1. Note that 50% of the steps are shared by both technologies. The manufacturing critical nodes, indicated in bold boxes, can be divided into two main categories. First, those that affect transistor performance and second, those which affect the passive component performance. The two baseline cross-sections are shown in Figs. 2 and 3 for InP HEMT and HBT, respectively [2][3]. The transistor performance critical nodes include epitaxial growth, HEMT gate formation, HBT emitter and base etching, and ohmic contact formation. The passive components critical nodes are thin film resistor metalization, MIM capacitor dielectric and backside wafer thinning. All of these processes must be well controlled to successfully fabricate high yield InP-based MMICs.
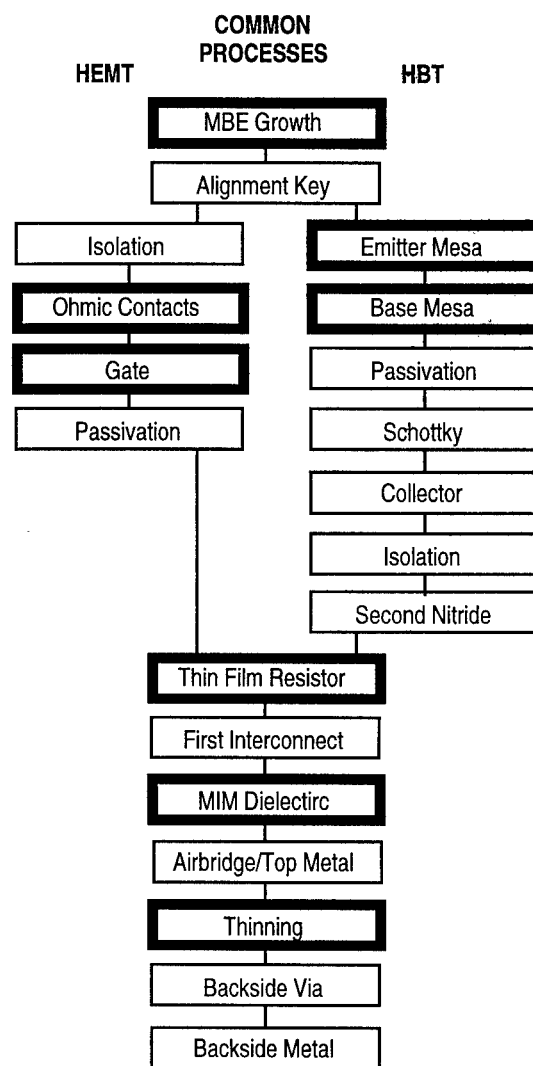
Fig. 1. Flexible InP MMIC manufacturing process flow where the critical nodes are indicated by bold boxes.
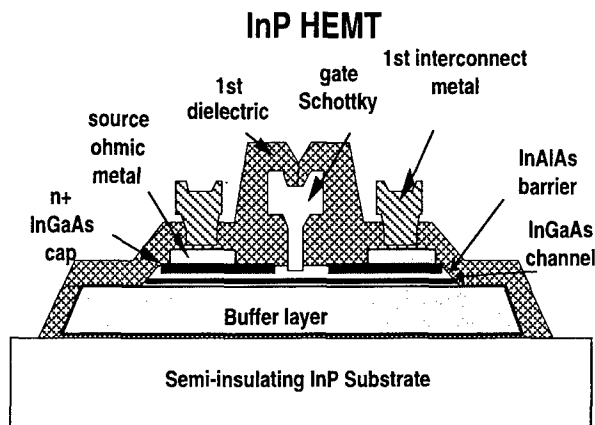
InP HEMT

Fig. 2. Production baseline InP HEMT cross-section.
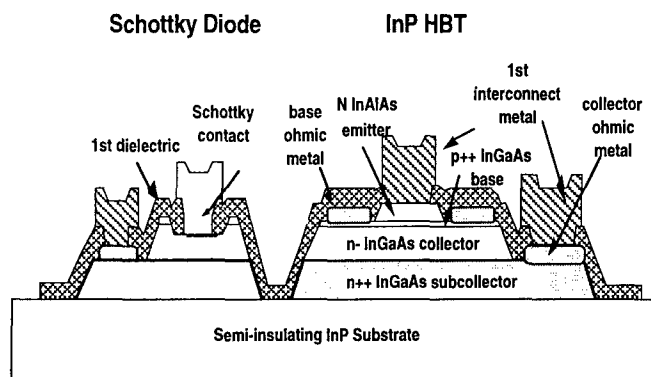
Fig. 3. Production baseline InP HBT cross-section.
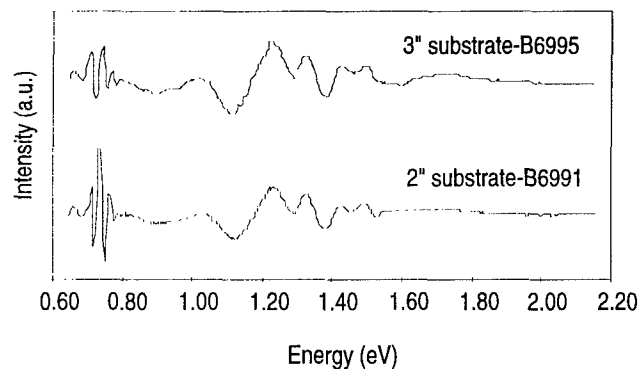
Fig. 4. Comparison of photoreflectance spectra for a 2-inch R&D InP HBT wafer and a 3-inch production InP HBT wafer.

Traditional statistical process control (SPC) methods have been applied to the InP fabrication line to help monitor process stability, increase process capability and drive future improvement efforts. The most important critical node in InP MMIC production is the molecular beam epitaxial (MBE) growth. Single crystal semi-insulating InP substrates are purchased from several suppliers and screened for defect density and resistivity. The first step in both the HEMT and HBT flow is to grow the device active layers. The R&D MBE profiles for both technologies were transitioned from 2-inch substrates to production 3-inch substrates. There were two goals for this transition: first, repeat the profile quality and uniformity on the 3-inch wafers; second, guarantee a repeatable manufacturing growth process.

Photoreflectance spectroscopic analysis enables non-invasive characterization of buried heterojunction devices such as HBTs following MBE growth. The photoreflectance spectra for a 2-inch R&D InP HBT wafer and an 3-inch production InP HBT wafer is plotted in Fig. 4. The excellent agreement between these two spectra indicates that the 2-inch R&D profile has been faithfully reproduced on the 3-inch wafer.

Examples of the production repeatibility for HEMT MBE growth is shown in Fig. 5 where the 2-DEG mobility and sheet carrier density are plotted for baseline profile monitor wafers representing over 150 production wafers. The mobility specification is 9000 - 12000 $cm^2/Vsec$. The ± 3 sigma process limits are both within the specification limits, demonstrating a process capability C_{pk} over 1. The InP HEMT and InP HBT epitaxial growth processes are both well understood and provide the reproducibility required for MMIC production.

The second most important critical nodes in InP MMIC production are gate formation for HEMTs and the emitter etch for HBTs. Both physical and electrical parameters are tracked after InP gate formation by electron beam lithography. The key physical parameter is the gate length as measured by scanning electron microscope after gate metal lift-off. The SPC tracking chart for gate length is shown in Fig. 6.
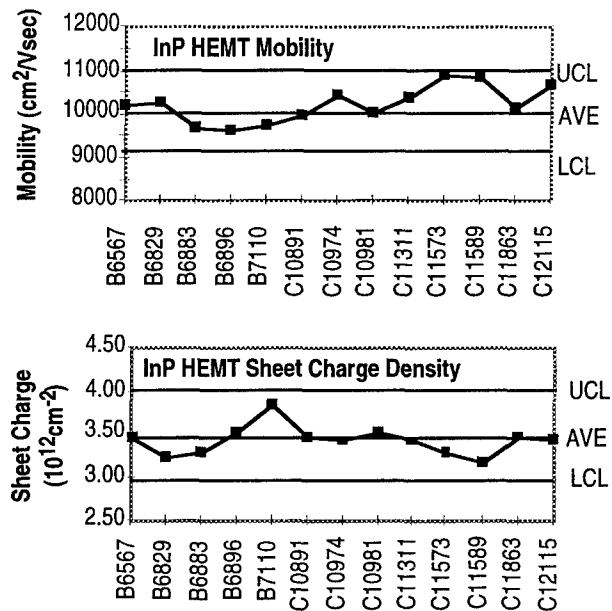
Fig. 5. Post MBE growth mobility and sheet charge density for InP HEMT monitor wafers.
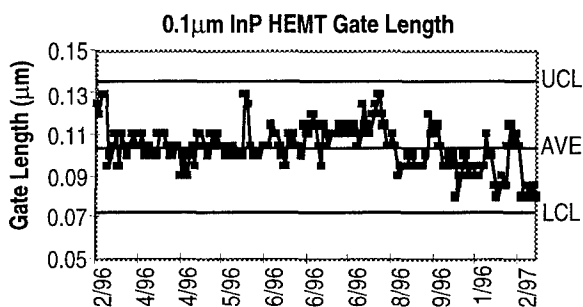
Fig. 6. 0.1µm HEMT Gate Length SPC tracking chart.

502
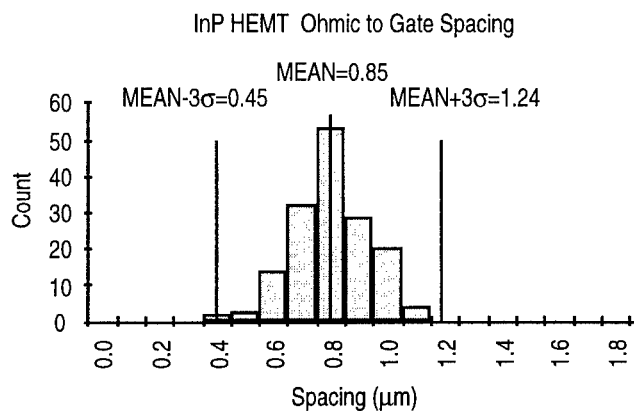
Fig. 7. Histogram of the gate to ohmic spacing for the InP HEMT production gate process.

Another important physical parameter tracked after InP HEMT gate formation is the spacing between the gate and the ohmics. This is a critical parameter for FET performance and is key to mating the electron beam lithography with the optical lithography used to define the ohmic metal. A histogram of this spacing is plotted in Fig. 7.

The InP HBT critical parameters associated with the emitter and base mesa critical nodes are transistor performance parameters. Transistor parameters are key measures of the process stability for both the HBT and HEMT technologies. In Fig. 8, the measured $V_{be(on)}$ and current gain ß are plotted for the production InP HBT process. The $V_{be(on)}$ is obtained at 10µA while the current gain is monitored at 4mA for a $1X10µm^2$ emitter device. In addition to DC parameters, RF parameters are also tracked as critical parameters. The cutoff frequency, f_t, is plotted in Fig. 9 for a $1X10µm^2$ quad emitter HBT as a function of lots processed over the last year. The data exhibits lot to lot repeatability of ±6% and an average cutoff frequency of 65 GHz.

Several critical nodes and parameters have also been defined for InP MMIC production for the passive components. The critical parameters are thin film resistor (TFR) sheet resistance, capacitor dielectric thickness and final substrate thickness after thinning. These parameters, as well as the transistor critical parameters, can also critically impact MMIC performance and yield. An example of one of these is shown in Fig. 10 where the sheet resistance of the TFR film is plotted for runs over the last year. The process capability Cpk is 0.96.

Over 50 different MMICs including LNAs, mixers, frequency converters, VCOs and high linearity amplifiers from X-Band through W-Band have been manufactured using the InP based MMIC processes. Fig. 11 shows the output power spectrum of a monolithic fundamental mode W-Band VCO in the 1 µm InP HBT process. The measured oscillation frequency is 94.7 Ghz and the peak output power is -3.5 dBm. This is the highest frequency fundamental mode oscillator ever reported using bipolar device technology. The gain and noise figure of an InP HEMT LNA is plotted for several sites on one of the 3 inch manufacturing wafers in Fig. 12. The best noise figure for this circuit is 3 dB. This wafer shows a typical performance of 3.5 dB.
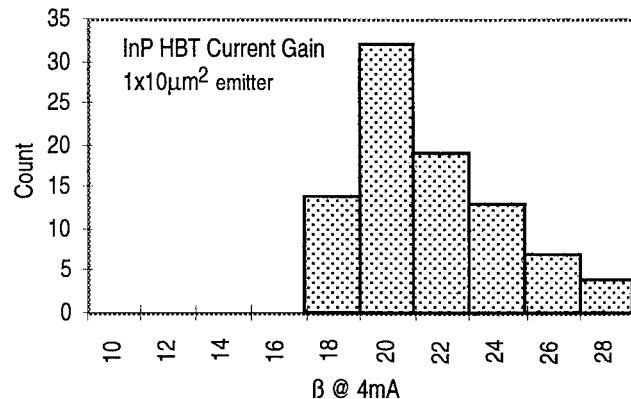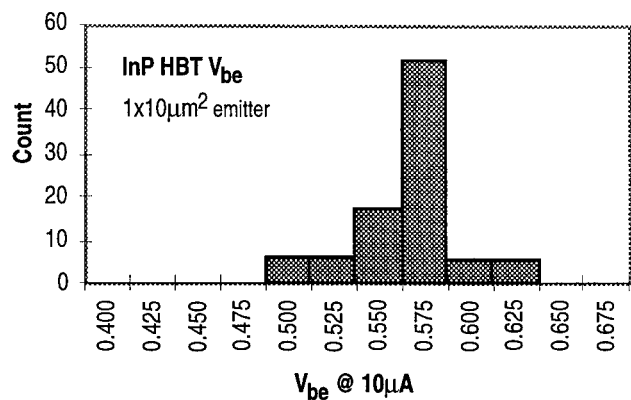
Fig. 8. Histogram of the characteristic $V_{be(on)}$ and ß for the InP HBT profile.
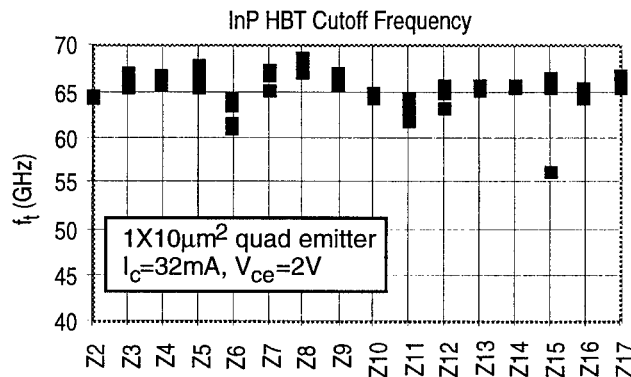
Fig. 9. Variation of f_t for InP HBTs representing >100 wafers.
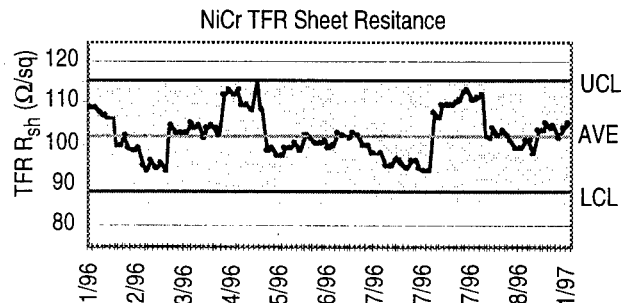
Fig. 10. SPC tracking chart for the TFR sheet resistance.

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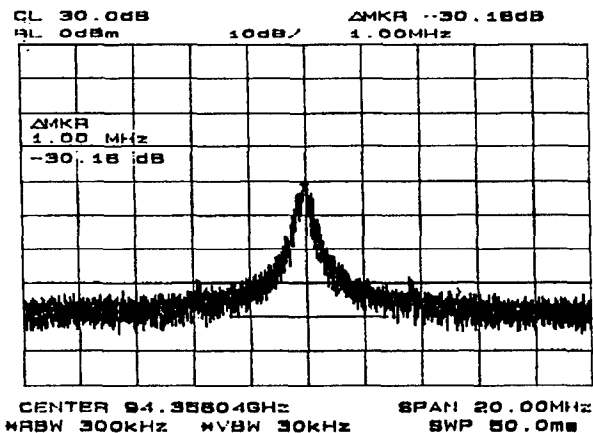
Fig. 11. Output power spectrum of fundamental mode W-Band InP HBT VCO.
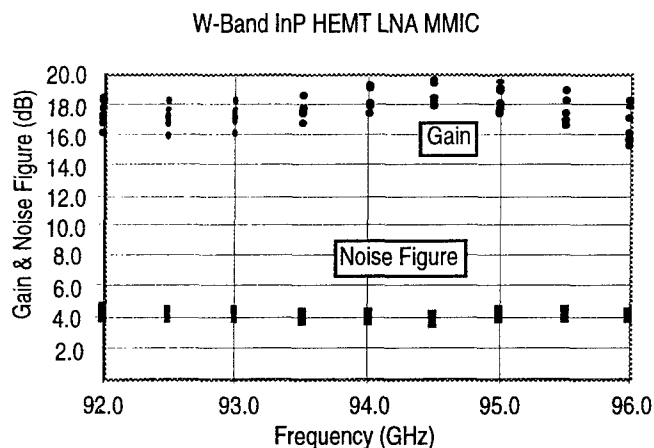
Fig. 12. Gain and Noise Figure response of all sites of a W-Band InP HEMT LNA from one wafer.

III. Conclusion

InP based MMICs will provide key performance advantages in terms of lower noise figure, lower DC power consumption and higher linearity for government and commercial production applications. TRW has transitioned InP MMIC fabrication from R&D to production. The key elements of this transition were a change from a product oriented focus to a process one, the use of statistical process control techniques and a drive toward process commonality between the HEMT and HBT technologies. We have demonstrated the repeatable processes and process capability necessary for InP MMIC production. MMIC performance for the production process compares well with the R&D performance.

IV. Acknowledgments

V. Referencess

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Effects of Annealing on the Performance of InP/InGaAs HBTs Grown by LP-MOCVD

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Introduction

The effects of rapid thermal annealing on InP/InGaAs heterojunction bipolar transistors with a carbon-doped base have been studied. The hydrogen concentration in the base has been studied as a function of the anneal temperature and time. A 10 minute anneal at 590° C under N_2 completely eliminates hydrogen from the base. By using shorter anneals and/or lower temperatures, the dc and rf device performance were studied as a function of the base hydrogen concentration. The results show that the base sheet resistance decreases with annealing time as does the dc current gain. As expected, the maximum frequency of oscillation increases as the base resistance decreases. The unity current-gain cutoff frequency, however, is significantly enhanced by removing hydrogen despite the resulting increase in the base hole concentration. A likely explanation for this behavior is that a large percentage of the hydrogen in the InGaAs base region incorporates as a compensating donor rather than forming a neutral CH complex.

Background

The low diffusivity of carbon makes it an excellent p-type dopant for the base of InP/InGaAs heterojunction bipolar transistors (HBTs). However, at the low temperatures required to grow heavily carbon-doped InGaAs by LP-MOCVD, a significant amount of hydrogen incorporates into the base layer. The nature and role of hydrogen in the base is not yet clearly understood, although several important characteristics have been observed. First, hydrogen has been observed to reduce the hole concentration to less than 70% of that of the carbon acceptors, limiting the as-grown hole concentration to or below 1×10^{19} cm^{-3}.[1] This makes it difficult to achieve carbon-doped HBTs with a low base sheet resistance using the MOCVD technique. (A hole concentration of $\sim 4 \times 10^{19}$ cm^{-3} is often desirable for state-of-the-art devices). Second, hydrogen in the base of GaAs-based HBTs has been shown to degrade device reliability because it can debond from carbon during device operation, thereby altering the base sheet resistance and current-gain with time.[2,3] Carbon-doped InP/InGaAs HBTs are likely to have similar problems. Finally, studies on single layers of heavily carbon-doped InGaAs indicate that the presence of hydrogen degrades the minority carrier mobility and may therefore degrade HBT performance.[4] Thus, it is important to understand the effect of hydrogen on device performance and to be able to control and/or eliminate hydrogen in the base. Lindner et al[5] have demonstrated that the hydrogen concentration in the base can be reduced by using TMAs during a post growth in-situ anneal. Recently, we have demonstrated that hydrogen can be removed from the base of carbon-doped InGaP/GaAs HBTs through *ex-situ* rapid thermal annealing (RTA) in an N_2 ambient without damaging the epitaxial layers.[6] In this work, the RTA technique was applied to InP/InGaAs HBTs. First the effects of the annealing conditions on the base hydrogen concentration were studied, then the effect of hydrogen on device performance was investigated. The results indicate that samples in which the hydrogen has been completely removed demonstrate superior performance.

Experimental Procedure

All material in this study was grown by LP-MOCVD using an Emcore GS3100 rotating disk reactor at a chamber pressure of 76 Torr. The column III precursors were TMIn, TMGa, and TEGa and the column V precursors were 100% AsH$_3$ and PH$_3$. Disilane diluted in H$_2$ (200 ppm) and CCl$_4$ diluted in H$_2$ (2000 ppm) were the n- and p-type dopants, respectively.

Pieces of an InP/InGaAs HBT (the as-grown layer structure is shown in Table 1) were annealed at

Table 1. Epitaxial structure of InP/InGaAs HBT.

InGaAs	$[Si] = 1 \times 10^{19}$ cm^{-3}	1500 Å
InP	$[Si] = 5 \times 10^{18}$	25 Å
InP	$[Si] = 5 \times 10^{17}$	1000 Å
InGaAs	$[C] = 2 \times 10^{19}$ $[H] = 1 \times 10^{19}$	1000 Å
InGaAs	$[Si] = 5 \times 10^{16}$	5000 Å
InP	$[Si] = 1 \times 10^{18}$	100 Å
InGaAs	$[Si] = 6 \times 10^{18}$	3000 Å

Figure 1 [H] in the base of an InP/InGaAs HBT as a function of anneal temperature as measured by SIMS. The anneal time was 5 min.

various temperatures and times to study the effect of annealing on the hydrogen concentration. Annealing was performed in an N_2 ambient and the samples were removed after cooling to 100°C. A piece of GaAs was placed on the surface of the sample to maintain an As overpressure at the surface during the anneal. No differences in the surface morphology were observed in any of the samples after annealing. Secondary ion mass spectroscopy (SIMS) measurements were performed to determine the hydrogen content in the base of each sample.

Based on these results, we found that the hydrogen concentration in the base can be controlled through the annealing conditions. The effect of hydrogen on device performance was studied by carefully controlling the annealing conditions so that different amounts of hydrogen were left in the base. Large area dc devices had an emitter area A_E of 60 x 110 μm^2 and the rf devices had an A_E of 4 x 5 μm^2.

The dc characteristics including the common-emitter current-gain, ß, the base sheet resistance, R_{sb}, and the base and collector ideality factors, n_b and n_c, respectively, were measured. The s-parameters were measured from 1 to 40 GHz using an HP8510C Network Analyzer. The unity current-gain cutoff frequency, f_t, was measured by extrapolating H_{21} at 10 GHz by 20 dB/decade. The maximum frequency of oscillation, f_{max}, was measured by extrapolating Mason's Invariant, U, at 20 GHz by 20 dB/decade.

Results and Analysis

Figure 1 shows the variation in hydrogen concentration with annealing temperature for an anneal time of 5 min as measured by SIMS. It is clear that the annealing procedure is successful at removing hydrogen from the base. At temperatures below 550°C, the hydrogen concentration is essentially the same as that of the "as-grown"
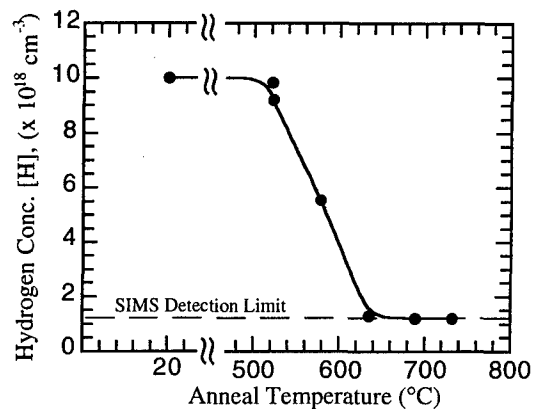
sample ($\sim 1 \times 10^{19}$ cm^{-3}). However, at 625°C, the hydrogen concentration has dropped by an order of magnitude. At higher temperatures, [H] becomes limited by the sensitivity of the SIMS measurement.

Figure 2 shows the hydrogen concentration in the base as a function of anneal time for an anneal temperature of 590°C. The hydrogen concentration decreases by an order of magnitude after annealing for 6 min. For longer anneals, the hydrogen signal is below the SIMS background level ($\sim 1 \times 10^{18}$ cm^{-3}). This data indicates that a relatively short, low temperature anneal can be used to eliminate hydrogen from the base material.

To study the effect of annealing on the dc performance, three samples were annealed at 570°C for 4, 8 and 12 minutes. Large area dc devices were then fabricated from these samples and an unannealed "as-grown" sample.
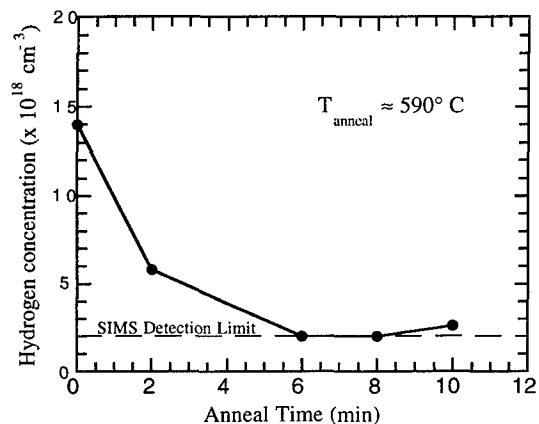
Figure 2 [H] in base of an InP/InGaAs HBT as a function of the anneal time as measured by SIMS. The anneal temperature was 590°C.
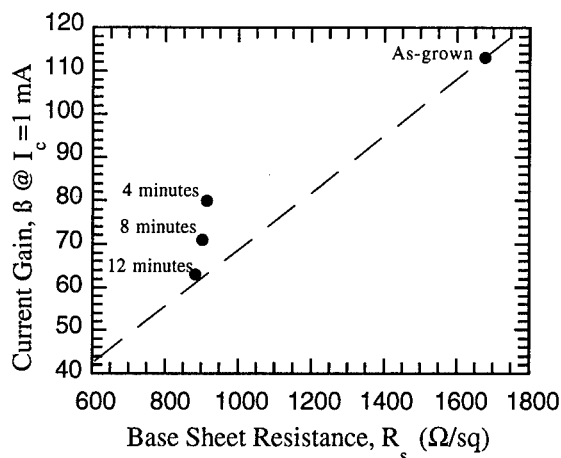
Figure 3 The dc current gain of large area HBTs as a function of base sheet resistance for various annealing times at 570°C. The dashed line represents a constant ß:Rs ratio.

Figure 4 Dependence of f_t and f_{max} on annealing time. The anneal temperature was 600°C.

The results are shown in Figure 3. For the as-grown case and the sample annealed for 12 minutes, the ß:R_{sb} ratios are nearly identical. In addition, the base ideality factor improved from ~1.3 to ~ 1.2 as the anneal time increased (not shown). This indicates that annealing does not severely degrade the junction or material quality. In fact for anneal times under 12 min, the ß:R_{sb} ratio is slightly higher than at the endpoints. Thus, it appears that a small amount of hydrogen or a short anneal may have a beneficial effect on the dc performance. However, it is also possible that longer anneals degrade the device performance for other reasons, canceling the beneficial effects of removing the hydrogen.

The effect of hydrogen on the high frequency performance is shown in Figure 4. As expected, f_{max} increases with annealing time. This is explained by the decrease in the base resistance as hydrogen is removed from the base. However, f_t also increases as hydrogen is eliminated, indicating that the base transit time is decreasing as the hydrogen concentration decreases. This behavior gives important insight into the role of hydrogen in InGaAs. If hydrogen simply passivates carbon acceptors, forming an electrically neutral CH complex, (as is commonly observed in C-doped GaAs) the base transit time would be expected to decrease with anneal time as more carbon atoms are ionized. However, if the hydrogen acts as a scattering center such as an ionized H$^+$ donor, then its presence in the base could degrade the base transit time. After annealing, the total number of scattering centers in

the base would decrease rather than increase, causing the base transit time to decrease. The data clearly show this trend. The degradation of the base transit time due to hydrogen is in accordance with Colomb et al[4] who found that the minority carrier mobility in heavily carbon-doped InGaAs increased dramatically after hydrogen was annealed out of the sample. It is possible that hydrogen is not a donor, but instead that the HC complex is not neutral. However, this explanation requires the HC complex to cause more scattering than an activated carbon ion.

Further evidence of hydrogen acting as a donor is shown in Figure 5 which is reproduced here from Ref. 7. The figure shows the majority carrier mobility of single layers of carbon-doped InGaAs as a function of doping level before and after the hydrogen has been removed. For annealed hole concentrations below 1×10^{19} cm^{-3}, the mobility decreases after annealing, but for higher carbon concentrations, the mobility increases after annealing. This suggests that for carbon concentrations below 1×10^{19} cm^{-3}, hydrogen incorporates as a CH complex that passivates the carbon acceptor. When the hydrogen is removed, the hole concentration increases, the number of ions increases, and the mobility decreases. For higher carbon concentration, at least some of the hydrogen appears to act as a compensating donor. The hole concentration and mobility increase after annealing, suggesting that the total number of ionized impurities decreases. This data suggests that the first ~3-4 x 10^{18} cm^{-3} hydrogen atoms incorporated act to passivate carbon or other defects in the base, while subsequent hydrogen incorporation may be in the form of H$^+$ donors.

507
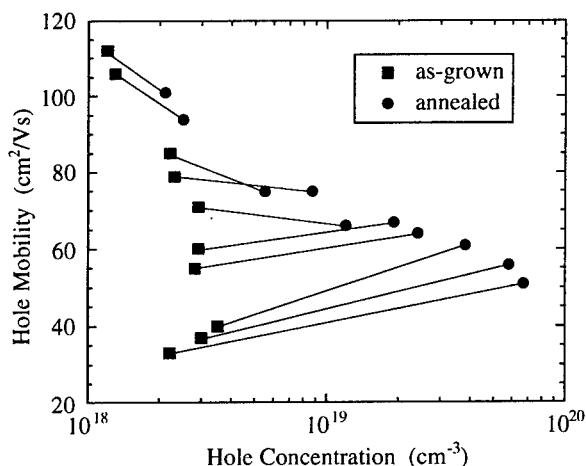
Figure 5 Majority carrier mobility as a function of hole concentration of single layers of carbon-doped InGaAs before and after annealing to remove all the hydrogen.[7]

Recently, hydrogen acting both as a donor and as a passivator in GaAs has been observed.[8] These studies also suggest that hydrogen donors are removed at lower temperature than hydrogen bonded to carbon. This model suggests a possible explanation for the data found here. If the H donors have a lower activation energy than the H passivators, then the base sheet resistance may decrease more quickly than the dc current gain since the hydrogen which is more difficult to remove may passivate defects that enhance base recombination. As the passivating hydrogen is removed, the current gain may degrade significantly. Figure 3 suggests this type of effect. Therefore, a small amount of hydrogen may benefit device performance by improving the ß:Rsb ratio (although it may not be suitable from a reliability standpoint). The high frequency performance shows that the 6 min. and 9 min. anneals are nearly identical, indicating that a small amount of passivating hydrogen may not significantly effect the base transit time, which is reasonable if any remaining hydrogen forms an electrically neutral HC complex.

Conclusions

An *ex-situ* annealing process has been used to remove hydrogen from the base of InP/InGaAs HBTs and to study the effect of hydrogen on device performance. An anneal at 590°C for 10 min was used to completely eliminate hydrogen from the

base, and lower the base sheet resistance by a factor of two without degrading the material quality. This is a critical technique for maximizing the base hole concentration and optimizing the performance of LP-MOCVD grown InP/InGaAs HBTs.

As expected, f_{max} increases as hydrogen is removed and the base sheet resistance decreases. The f_t also increases significantly after annealing, verifying the findings of Ref. 4 which show that hydrogen degrades the minority carrier mobility. These results suggest that a large portion of the hydrogen incorporates as an ionized donor and that a smaller portion may passivate carbon acceptors or other defects in the base region. It appears that a small amount of hydrogen may passivate defects in the base and result in an optimal $\beta:R_{sb}$ ratio. Thus, although it might be difficult to control precisely, removing only the hydrogen donors and leaving the passivating type of hydrogen may optimize device performance. Unfortunately, this small amount of hydrogen may be undesirable with respect to device stability.

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OPTIMIZATION OF InGaAs/InAlAs/InP HEMT GATE RECESS PROCESS FOR HIGH FREQUENCY AND HIGH POWER APPLICATIONS

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Introduction

We have optimized the gate recess etch process for our W-band high power 0.15 μm gate length InGaAs/InAlAs/InP HEMT's. A 640 μm single-stage MMIC amplifier built on this device demonstrated an output power of 130 mW with 13% power added efficiency at 94 GHz. This results represent the best output power fixture data to date measured from a single InP-based HEMT MMIC at this frequency.

I. Background

High power and high efficiency millimeter-wave power amplifiers are the key enabling component for the development and deployment of next generation communication and electronic warfare systems. For examples, highly efficient radiating elements are required for W-band phased arrays for smart munitions and asset protection systems to minimize the overall array DC power and thermal design requirements. On the other hand, very high transmitter power at 94 GHz will be needed for missiles to increase the standoff distance or the interceptor ranges while improving the precision to hit. To satisfy the demand, there has been intensive development of high power MMIC amplifiers using GaAs-based pseudomorphic HEMT's (PHEMT's)[1-6] and InP-based InAlAs/InGaAs HEMT's[7] for 94 GHz operations and tremendous progress has been achieved.

InP-based InAlAs/InGaAs HEMT's have demonstrated the highest cutoff frequency and lowest noise figure for any three-terminal solid-state devices[8-9] due to their enhanced carrier confinement and superior transport properties. Very high gain InP HEMT MMIC LNA's have been realized at frequencies as high as 140 GHz[8]. Because of its high gain, InP HEMT has also demonstrated higher power added efficiency (PAE) than GaAs-based PHEMT for the same output power level at 94

GHz[7], even though the former has lower breakdown voltages.

Because of the relative immaturity of InP HEMT development, the reported output power of InP HEMT amplifiers has been limited to about 50 mW[7,10]. In this paper, we report the optimization of gate recess process which enabled the development of a 640 μm single-stage InP HEMT MMIC amplifier. This amplifier delivered 130 mW output power with 13% PAE at 94 GHz. This result represents the best output power fixture data to date measured from a single InP-based HEMT MMIC at this frequency.

II. Gate Recess Optimization

The inset of Fig. 1 shows the schematic of our 0.15 μm gate-length, double doped, double heterostructure InGaAs/InAlAs/InP HEMT. In the past few years, we have improved the material structure, delta doping density, ohmic contact layer, substrate thickness, and compact device layout to achieve an excellent power and efficiency combination -- 54 mW with 20% PAE at 94 GHz[7]. In this work, we systematically investigated the relationship between gate recess depth and RF device output power level.

Gate recess depth is an important variable in device process optimization. The gate recess depth

can be optimized by referencing to V_{gp} (the gate voltage where peak g_m occurs) as measured after gate metallization. For a given material profile, the deeper the recess, the more positive the V_{gp}. We have systematically investigated the relationship between V_{gp} and device DC and RF performance. As illustrated in Fig. 2, when we changed V_{gp} from +0.25 V to -0.13V by varying recess depth, device peak g_m varied from 900 mS/mm to 680 mS/mm. Associated with the change was the increase in maximum channel current, I_{max} (measured at V_{gs}=0.4 V), from 450 mA/mm to 650 mA/mm. The lower g_m in devices with shallower recess (more negative V_{gp}) is due to the increased $(d + \delta d)$, where d is the InAlAs Schottky barrier thickness and δd is the effective distance of the two dimensional electron gas (2DEG) to the barrier. A g_m of 900 mS/mm at V_{gp} = 0.25V is slightly lower than that (typically >1000 mS/mm) of a single-doped low noise HEMT of similar V_{gp}. This might be because the lower doping plane in the double-doped structure moved the 2DEG slightly away from the barrier, effectively increased δd. The lower I_{max} in the more positive V_{gp} device is due to the channel depletion caused by the closer Schottky contact. The DC current-voltage characteristics of a device with V_{gp} = -0.13 V are shown in Fig. 1.

Figure 3 shows the relationship between V_{gp} and the total output power of two single-stage MMIC amplifiers with total gate peripheries of 160 µm and 320 µm, respectively. The output power data were measured in fixture at 94 GHz with input power levels such that the power gain was 4 dB. The DC bias conditions were optimized for maximum output power. As can be seen, as the recess depth was varied such that V_{gp} increased from -0.13 V to +0.25
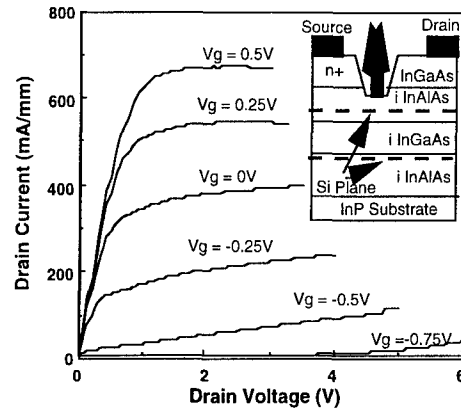
Fig 1.   A 0.15 µm gate length InP-based HEMT   and   its   current-voltage characteristics.

V, the output power of the 320 µm single-stage amplifier dropped from >20 dBm to 12.5 dBm. The output power dropped especially fast as V_{gp} became positive. Similar trend was observed from the 160 µm amplifier which had a different matching network. The reasons for the reduced output power in the positive V_{gp} devices might be two folds. First, the low I_{max} reduces the output current dynamic range, resulting in lower output power, since the output power is proportional to I_{max}X(breakdown voltage - knee voltage). Second, the positive V_{gp} reduces the input voltage swing range. Since the forward turn-on voltage for InAlAs-metal Schottky contact occurs at ~0.5 V, an input voltage swing over 0.5 V will induce large gate current, significantly reducing the gain and output power. The input and output matching circuitry may also affect the output power
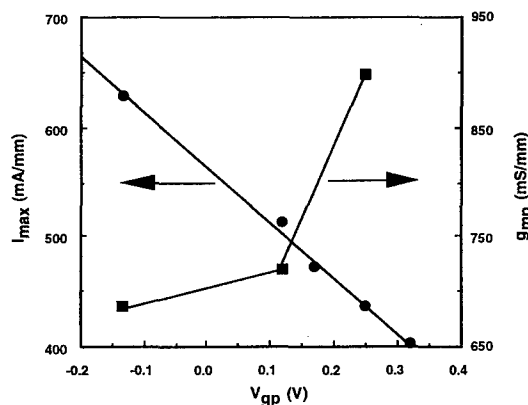
Fig. 2.   Peak g_m and I_{max} as functions of V_{gp} for 0.15 µm gate InGaAs/InAlAs HEMT with various gate recess depth.
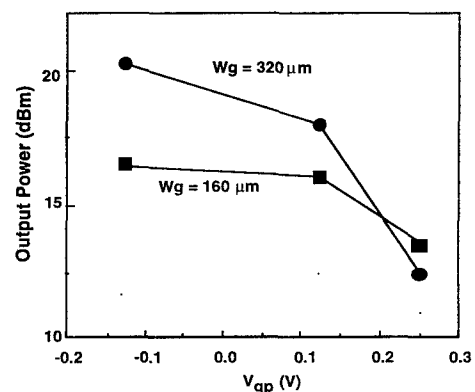
Fig. 3. RF output power of single-stage 160 µm and 320 µm amplifiers as functions of Vgp.

510

level. However, the effect is not significant enough to cloud the previous conclusion.

III. Amplifier Performance

Based on the recess optimization results, we have fabricated and characterized a 640 μm single-stage MMIC amplifier with device V_{gp} being targeted at -0.1 to -0.15 V. The amplifier was fabricated using TRW's established InP HEMT MMIC process[11,12]. We used 2 mil thin substrates which allowed us to reduce the size of the via holes and place them closer to the source. This not only lowers parasitic source inductance but also offers improved thermal conductivity. We derived the output matching impedance of the MMIC's based on simulations. Rigorous design and analysis methodology, including accurate device modeling and full-wave electromagnetic (EM) simulation of passive structures ensured the optimization of gain and bandwidth.

The photograph of a 640 μm single-stage amplifier is shown in Fig. 4. When biased at a V_{ds} of 2.7 V, the amplifier delivered an output power of 130 mW with 13% PAE and 4 dB associated gain (Fig. 5). To our knowledge, this is the highest power ever achieved from a single InP-based HEMT MMIC amplifier at 94 GHz.

Figure 6 compares the power and efficiency performance of various InP HEMT MMIC's and GaAs HEMT MMIC's measured in fixture at 94 GHz. InP-based InAlAs/InGaAs HEMT's clearly
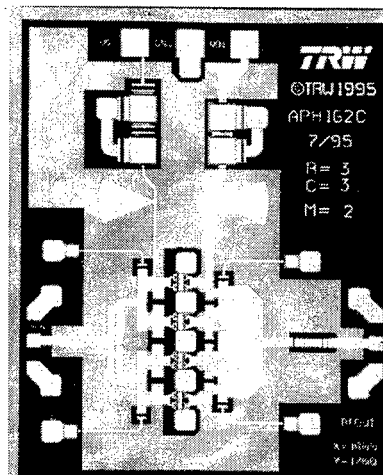
Fig. 4. Photograph of a 640 μm single-stage InP HEMT MMIC amplifier.

outperformed their GaAs-based counterparts in PAE for the same output power levels and demonstrated their potential for high efficiency and high power applications at millimeter wave frequencies.

Acknowledgment
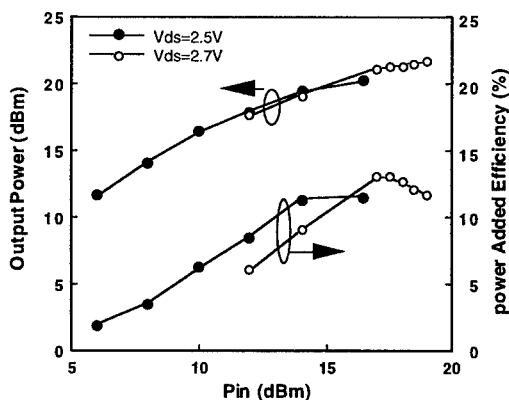
Fig 5. Output power and PAE as functions of input power measured from a 640 μm single-stage InP HEMT MMIC amplifier in fixture at 94 GHz.
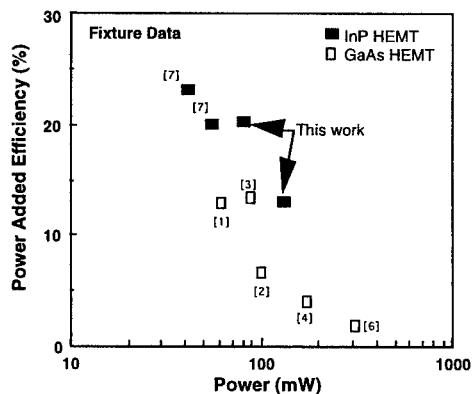
Figure 6: Comparison of PAE vs. output power for various GaAs-based PHEMT and InP-based HEMT MMIC amplifiers at 94 GHz.

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Processing and Interface Analysis of CdS-Passivated InP

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Introduction

The success of silicon is largely due to the availability of CMOS technology, which is made possible by the nearly perfect electrical and chemical properties of the oxide/semiconductor interface. Conversely, the lack of an adequate surface passivation technology for the III-V semiconductors has severely curtailed analogous MIS device technology development, restricting the options for compound semiconductor circuit design. Recently, we have developed a cadmium sulfide-based surface treatment that results in a chemically stable (100) n-InP surface with nearly ideal MIS diode C-V response.[1,2] Despite the fact that the CdS deposition process is simple and can easily be integrated into many manufacturing processes, the interface chemistry of the CdS/InP system is complex. We have used x-ray photoelectron spectroscopy (XPS) to investigate this interface, with corresponding C-V analysis of the SiO_2/CdS/InP interface region. Interface stoichiometry and electrical response were measured at several different deposition conditions in order to determine optimum growth conditions for the CdS interfacial layer. Fabrication, electrical response, and high frequency response of an ion-implanted depletion-mode InP MISFET were also investigated.

I. Background

Our investigation into the use of CdS as a passivating layer for InP-based MIS devices was largely motivated by earlier successes in the fabrication of InP-based MISFETs treated with sulfur-bearing solutions.[3] Sulfur was found to improve device response by filling phosphorus vacancies at the surface, resulting in a thermodynamically favored and stable In_2S_3 passivating layer.[4] We have found that chemical bath deposition (CBD) of thin layers of CdS passivates InP in much the same way. The CdS layer bonds to the InP surface by way of In-S, with the resulting In_2S_3 layer protected by the CdS layer immediately above it. A favorable valence band offset (-1.06 eV), large band gap (2.42 eV), and good lattice matching all enhance the unique passivating effect of CdS on InP. CBD CdS has been shown to grow in the hexagonal phase on (111) InP, while the cubic phase is preferred on (100) InP.[5,6] Epitaxial growth of CdS has been found to be quite sensitive to InP surface preparation and bath concentrations. Similarly, our investigations have shown the passivating effect of the CdS layer on InP is dramatically affected by reactant concentrations and InP surface preparation.

Our previously reported standard deposition conditions include a pre-treatment in 0.033 M thiourea ($CS(NH_2)_2$) and 12.3 M NH_3 at 85°C for 15 min. XPS analysis of samples prepared in this manner shows evidence of In-S bonding at the surface, with a notable absence of native oxides.[7] We have observed using our previously reported standard CdS deposition conditions (0.028 M thiourea, 0.014 M cadmium sulfate ($CdSO_4$), and 11 M NH_3 for 3 min at 85°C) that some CdS films had a non-specular appearance. SEM and Auger electron spectroscopy (AES) analysis indicate crystallites of $Cd(OH)_2$ present on the surface. $Cd(OH)_2$ is an intermediary

in the formation of CdS.[8] Subsequently prepared MIS samples showed poor C-V response. It was found that these crystallites could be effectively removed by post-treating the sample in 0.033 M thiourea and 12.3 M NH_3 at 85°C for 15 min. In an effort to avoid non-specular film growth and the resulting need for post-treatment, the effect of variations in CdS growth conditions on surface chemistry and resulting MIS C-V response was investigated.

II. Experimental

All samples were pre-treated 15 min at 85°C in a 0.033 M thiourea, 12.3 M NH_3 solution. Samples were immediately immersed in the room temperature CdS deposition solution following pre-treatment. The CdS is deposited from an aqueous solution of thiourea, $CdSO_4$, and NH_3. Samples were prepared at the deposition conditions listed in Table 1. Lower $CdSO_4$ and NH_3 concentrations were examined in order to decrease the amount of $Cd(OH)_2$ in solution. For all CdS depositions the thiourea concentration was 0.028 M and the temperature was 85°C.

Following CdS deposition, SiO_2 was deposited for 3 min at 260°C and 3 Torr.[9] Silane was used as an overpressure during sample heating. Front and back contacts for MIS samples were formed by thermal evaporation of Al and In, respectively. All MIS samples were annealed overnight at 350°C in N_2. A small piece for XPS analysis was removed from each sample before SiO_2 deposition.

Table 1. CdS deposition parameters.

	[NH$_3$]	**[CdSO$_4$]**	**pH**	**Dep. Time**
A	1 M	2.5×10^{-6} M	11	1-25 min
B	1 M	2.5×10^{-6} M	10	10-25 min
C	11 M	2.5×10^{-6} M	12.3	3-24 min
D	11 M	0.014 M	12.3	3 min

513

III. XPS Results and Discussion

In order to determine the chemistry of the passivated InP surface following thiourea/ammonia pre-treatment and CdS thin film deposition, XPS analysis was performed on a Physical Electronics PHI 5100 using non-monochromatic Mg K_α radiation at 1253.6 eV. The diameter of the analysis area is 800 μm. A pass energy of 11.75 eV was used for all detail scans. The spectra were corrected for charging effects by referencing the C $1s$ peak to 284.8 eV. After Shirley background subtraction, Gaussian-Lorentzian peaks were fitted to the spectra for non-linear least squares optimization. The elemental peak areas were corrected using standard sensitivity factors.[10] For fitting the In $3d_{5/2}$ peak, results obtained on vacuum-cleaved InP were used as a guide, with a FWHM for the substrate component of 1.15 eV and a Gaussian-to-Lorentzian ratio of 2.2. The polar angle of analysis, θ, was 45°. A mean free path of 25 Å was assumed.

For all samples, the In $3d_{5/2}$ peak was fit with a substrate component at 444.5 eV and a component shifted 0.7 eV from the substrate peak. This component may be attributed to In-O or In-S bonding, but due to the observed S $2p$ sulfide signal, we attribute the shifted component to In-S. For pure In_2S_3 samples, the separation between the In $3d_{5/2}$ and S $2p$ peak has been reported as 283.2 eV,[11] which is close to our value (445.2 - 161.7 = 283.5 eV).

An important measure of the quality of the InP surface is the degree of P deficiency. P vacancies can act as traps which impair the C-V response of subsequently fabricated devices. Figure 1 shows the area ratios of the In $3d_{5/2}$ substrate component to the P $2p$ component at 128.8 eV. The ratios are plotted versus Cd/In, which is a measure of relative CdS thickness. There is a general trend of increasing P/In(-P) with increasing CdS layer thickness. This increased value of
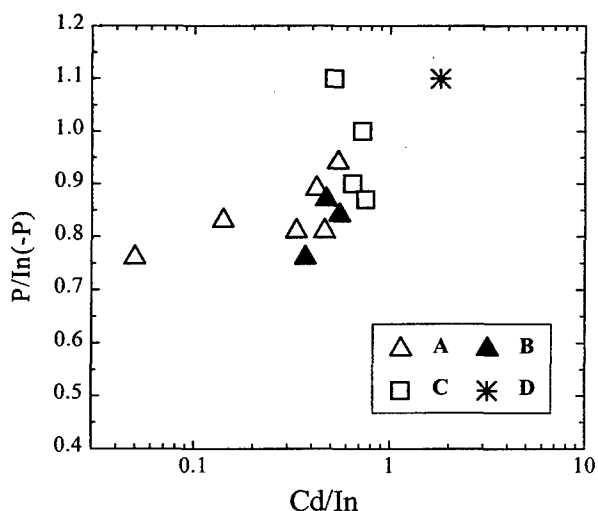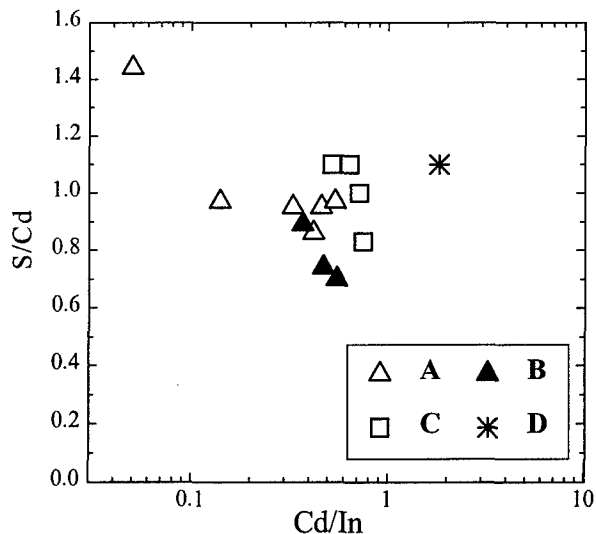
Figure 2. S/Cd ratio for the samples prepared as in Table 1.

P/In(-P) is not yet understood. While depositions at low [NH₃] (A and B) give P/In(-P) ratios of 0.8–0.9, both the standard growth (D: 11 M NH₃, 0.028 M CdSO₄) and the 12 min growth (C: 11 M NH₃, 2.5x10⁻⁶ M CdSO₄) have equivalent P/In(-P) ratios.

The binding energies of the Cd $3d_{5/2}$ and S $2p$ peaks of all samples were 405.1–405.5 eV and 161.6-161.8 eV, respectively, in agreement with previously reported data on single-crystal and thin-film CdS samples.[10] The presence of Cd-P bonding in the samples could not be verified due to the lack of either a good standard or reference data. The existence of this species cannot be excluded, therefore, and a complete understanding of the chemistry at the CdS-InP interface will require more experimentation. Figure 2 shows the area ratios of the S $2p$ peak to the Cd $3d_{5/2}$ peak for samples prepared as in Table 1. The high value of S/Cd at lower thicknesses is due sulfur deposited during the pretreatment.

IV. MIS Results and Discussion

Figure 3 shows the optimum C-V response obtained from samples prepared with CdS deposition conditions as given in Table 1. C-V response for MIS samples was measured at 1 MHz using an HP 4275A multi-frequency LCR meter; quasistatic measurements were made with a Keithley 595 meter. Interface-state densities were calculated by the method of Castagné and Vapaille,[12] using both high-frequency and quasistatic C-V data.

Figure 3(a) shows the optimum C-V response for condition A obtained with a growth time of 15 min. The CdS interlayer thickness is ~24 Å. The hysteresis of this sample, 0.05 V, is one of the lowest measured for samples prepared using any of the deposition conditions. The quasistatic and high-frequency C-V responses are very close at gate voltages

Figure 1. Ratio of P/In(-P) for the samples prepared as in Table 1.

Figure 3. 1 MHz and quasi-static C-V response for (a) 15 min, **A**, (b) 25 min, **B**, (c) 12 min, **C**, and (d) 3 min, **D**, where **A**,**B**,**C**, and **D** are the deposition conditions listed in Table 1.

V. MISFET Fabrication and Response

The depletion-mode InP-channel MISFETs reported in this study were fabricated from ion-implanted SI-InP (CrystaComm). Si was implanted at doses of 5×10^{12}, 7.5×10^{11}, and 7.5×10^{11} cm^{-2} with energies of 25, 75, and 100 KeV, respectively. Wafers were pre-treated as previously described then capped with 100 nm of SiO$_2$. An 800°C, 30-second anneal was used to activate the implant. Hall measurement after the activation anneal gave sheet carrier concentrations of 8.5×10^{12} cm^{-2}. After stripping the SiO$_2$ cap with HF, mesas and channel recesses were formed with H$_3$PO$_4$:H$_2$O$_2$:H$_2$O (1:1:4). Studies of MIS capacitors fabricated from n-type InP wafers showed UV cleaning of processed samples to be beneficial before sulfur pre-treatment and CdS deposition. After cleaning, samples are passivated, and a 25 nm gate oxide is deposited. TiAu gate metal is aligned to the recess with a liftoff process. AuGeNi ohmic contacts are placed after removing the SiO$_2$ and CdS passivation layer in the contact openings. As with the MIS capacitors, processed wafers were annealed overnight in N$_2$ at 350°C.

Good device characteristics were obtained with a CdS passivation layer deposited from a dilute CdSO$_4$ solution (Growth A). Condition A was selected because of the low hysteresis and D_{it} obtained for MIS samples. Common-source I-V characteristics of a 1 µm x 250 µm gate device are shown in Fig. 4. Accumulation with positive voltage and depletion with negative bias imply the Fermi level is not pinned by an excessive density of interface states. Low output conductance (G_O=0.8 mS/mm) and good pinch-off are observed for V_{DS}=5 V. Breakdown occurs in 1 µm gate-length devices at V_{DS}>20 V. Drain current and transconductance are shown in Fig. 5 for a 1 µm x 125 µm gate device with V_{DS}=4V. The

near -0.2, indicating a very low density of traps near this surface potential. D_{it} values for this sample calculated by the high-low method had a minimum value of 6×10^{10} eV^{-1}cm^{-2}, while Terman analysis gave $\sim 1 \times 10^9$ eV^{-1}cm^{-2}.

Figure 3(b) shows the optimized response for condition **B** with a deposition time of 25 min. The CdS layer is ~ 23 Å. The response is similar to the response of **A**. Both deposition conditions are the same but the pH of **B** is adjusted to 10 by the addition of NH$_4$Cl. Lowering the pH lowers the overall deposition rate of the reaction. The hysteresis is again low (0.08 V), with a minimum D_{it} of 3×10^{11} eV^{-1}cm^{-2} using the high-low method, and 3×10^{10} eV^{-1}cm^{-2} by Terman analysis.

Figure 3(c) shows the optimum response obtained under growth condition **C** with a deposition time of 12 min. The CdS thickness is ~ 35 Å. The hysteresis is 0.16 V with a minimum D_{it} of 2.5×10^{11} eV^{-1}cm^{-2} calculated using the high-low method. The sample of Fig. 3 (d), condition **D**, has similar response, but with reduced hysteresis (0.1 V) and D_{it} (1×10^{11} eV^{-1}cm^{-2}). The sample shown in Fig. 3(d) was the only sample with a non-specular surface, hence requiring post-treatment prior to oxide deposition.

Samples grown with high [NH$_3$], **C** and **D**, exhibit better quasistatic response than samples fabricated with lower [NH$_3$], **A** and **B**. While sample **C** has a thicker CdS interlayer than samples **A** and **B**, increasing the CdS growth times of **A** and **B** did not yield samples with an improved quasistatic response over that shown in Fig. 3 (a) and (b). Samples prepared with lower [NH$_3$] showed smaller hysteresis than those prepared at higher concentrations. The low-frequency behavior of all samples shows that the Fermi level is unpinned, allowing the InP surface to be biased from accumulation to inversion.

Figure 4. Common source I-V characteristics for a CdS-passivated InP depletion-mode MISFET.

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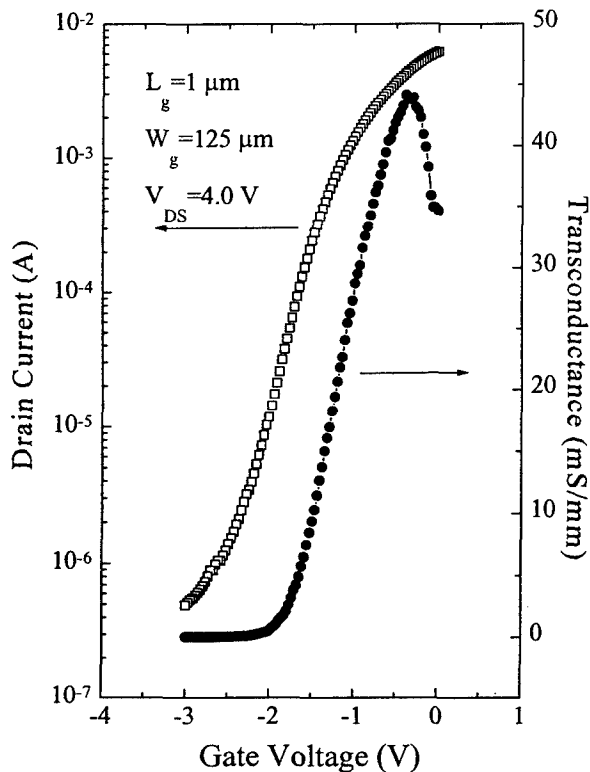
Figure 5. Common-source drain current and transconductance for a CdS passivated InP depletion-mode MISFET.

implanted device demonstrates hard pinch-off with $I_D < 1$ μA. A maximum transconductance of 45 mS/mm is shown, but transconductances as high as 70 mS/mm were observed.

Uniformity and performance are sensitive to channel recess. The recess is not only necessary to remove the highly doped surface layer, but to remove surface damage due to the high-temperature activation anneal. To investigate the damage caused by the activation anneal, test capacitors were prepared with the same capping procedure and subjected to the activation anneal. Approximately 15 nm of the surface had to be removed before capacitors of acceptable quality were obtained. The photoluminescence intensity for capped and annealed n-type samples recovered after similar etch depths. The conductance-voltage $(G-V)$ method was used to estimate the interface-state density of large-area FETs (40 μm x 125 μm). G_p vs. ω data revealed D_{it} to be below 10^{12} eV^{-1}cm^{-2}.

Microwave performance of insulated-gate devices was evaluated with an HP8510C network analyzer. 1 μm x 250 μm gate devices were designed with a ground-signal-ground geometry to facilitate microwave probing. S-parameters were measured between 100 MHz and 20 GHz. Figure 6 shows the matched transducer power gain, $G_{tm} = |S_{21}|^2$, and maximum unilateral transducer power gain, G_{tumax}. Data was taken with V_{DS}=4V and V_{GS}=0V. From the plot of G_{tumax} vs. f we obtain a maximum frequency of oscillation, f_{max}, of 9 GHz. Using $g_m = -S_{21} / (2 \cdot Z_0)$ gives a transconductance of 60 mS/mm, which corresponds well with the static value measured from the slope of the I_D vs. V_{GS} curve.
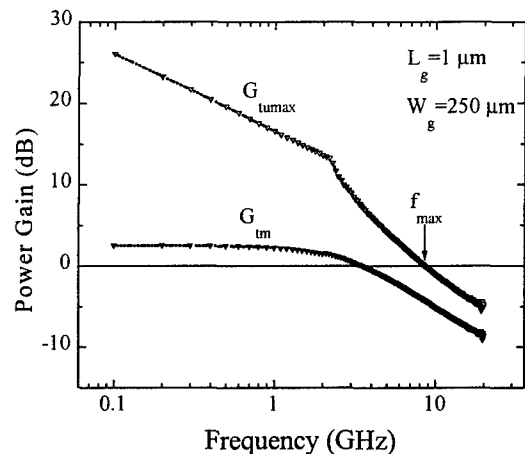
Figure 6. G_{tm} and G_{tumax} vs. Frequency for a CdS-passivated InP depletion-mode MISFET.

VI. Conclusions

We have investigated the use of CdS interlayers grown by CBD at several deposition conditions. All conditions studied were shown by XPS to produce relatively stoichiometric CdS layers. Evidence of In-S bonding was seen for all conditions. C-V response of all samples showed a passivating effect on InP by the CdS layers. Samples prepared with higher [NH$_3$] had a lower density of interface states throughout the gap, while samples prepared at lower [NH$_3$] showed reduced hysteresis. Ion-implanted MISFETs prepared with CdS passivating layers showed good transconductance (60 mS/mm) with f_{max} of 9 GHz. The ability to deposit CdS layers at a variety of deposition conditions allows integration of this technology into a variety of III-V fabrication processes.

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Formation of Pinning-Free Schottky Barriers on InP and Related Materials by Novel In-Situ Electrochemical Process and Its Mechanism

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Introduction

Recently the so-called InP-based materials such as InP, $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ have become important materials for high speed electronic and optoelectronic devices. A common drawback of these materials is, however, that Schottky barrier heights (SBHs) on n-type materials are generally low. Typical SBH values are 0.45eV, 0.60eV and 0.20eV for n-InP, $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$, respectively. Technologically low SBH values are problematic and impose severe limitations on the realizability of MESFETs and MSM photoditectors, and performance and reliability of HEMTs. In an attempt to overcome this difficulty, we have recently found that the SBH value of the Pt/n-InP Schottky diode can be increased up to 0.86 eV by using a novel in-situ electrochemical process,[1] and have succeeded in realization of well-behaved InP MESFETs[2] for the first time.

The purpose of the present paper is further to understand and optimize the electrochemical process in view of its possible application to formation of fine Schottky gate electrodes for InP-based HEMTs utilizing InAlAs/InGaA s/InAlAs/InP heterostructures. First, electrodeposition conditions and metal selection were optimized for InP for higher SBHs. Then, applicability of the electrochemical process for formation of Schottky gate was confirmed directly on HEMT wafers. Finally, the possible mechanism for the observed SBH increase is briefly discussed.

I. Experimental

The in-situ electrochemical process consists of the anodic etching of the semiconductor surface followed by the metal electro-plating on the semiconductor. The electrolyte bath contains three electrodes, i.e., a semiconductor electrode for metal deposition, a Pt counterelectrode and a reference saturated calomel electrode (SCE). The potential of the semiconductor electrode is controlled by the potentiostat. The etching and the plating can be done either in d.c. mode or in pulsed modes in the same electrolyte. Etching mode or deposition mode can be done by changing the polarity of the voltage supply. Potential waveforms are schematically shown in Fig.1. In this study, etching was already done in the pulsed modes. Generally, use of pulses

instead of direct currents facilitates the accurate control of etching or plating thickness and also improves the efficiency of plating because of avoiding the problem of H_2 evolution at the surface.[1]

The electrolyte contains metallic ions for plating. In this study, various metals were deposited by using the following electrolytes.

Pt: 1M HCl(200ml)+H_2PtCl_6(1g)+NH_4OH [pH=1]
Co: 1M HCl (200ml)+$CoSO_4$ (10g) + NH_4OH [pH=1]
Ni: 1M HCl (200ml)+$NiSO_4$ (24g)+$NiCl_2$ (3g)+NH_4OH [pH=2]
Ag: 1M HCl (200ml) + AgCl (1g) [pH=0]

As semiconductor materials for Schottky contacts, n-type InP(100) bulk wafers, $In_{0.52}Al_{0.48}As$ epitaxial layers, $In_{0.53}Ga_{0.47}As$ epitaxial layers and standard InAl As/InGaAs/InAlAs/InP HEMT wafers were used. The latter epitaxial layers were grown on (100) n+InP substrates or semi-insulating InP substrates by standard molecular beam epitaxy (MBE). GeAu/Ni contact layer for electrical current supply was evaporated on the either back or front side of samples and annealed in H_2 for 5min at a temperature of 350°C. Photoresist and EB-resist patterns were used as the mask for selective etching and metal deposition. Just before starting the electrochemical process, samples were chemically etched in order to remove the native oxides.

For the analysis of the interfacial and the electrical properties of Schottky contacts, scanning electron

(a)

(b)
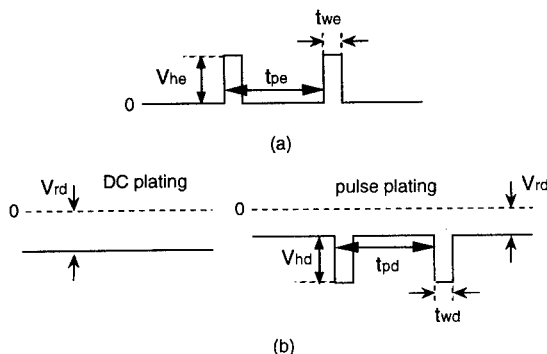
Fig.1 Potential waveforms for (a) etching and (b) plating

(a) 300nm (b) 300nm

(c)

(d)
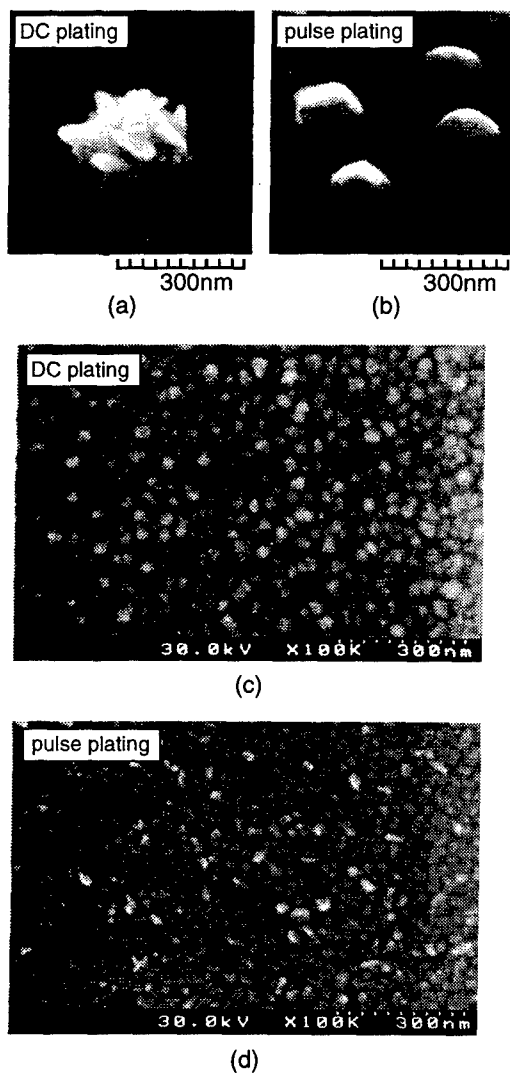
Fig.2 SEM images of the Pt-deposited InP surfaces. (a) and (b): initial phases, and (c) and (d): final phases.

microscopy (SEM), atomic force microscopy (AFM), X ray photoelectron microscopy (XPS), Raman spectroscopy, current-voltage (I-V) and capacitance-voltage (C-V) studies were performed. The SBH values and the ideality factor (n) were obtained by using a standard thermionic emission model with the effective Richardson constant of 9.6 cm^{-2} K^{-2}, 16.5 cm^{-2}K^{-2} and 5.04 cm^{-2}K^{-2} for n-InP, n-In$_{0.52}$Al$_{0.48}$As and n-In$_{0.53}$Ga$_{0.47}$As, respectively.

II. Electrochemical Process Optimization for High SBHs

A. Surface Topology

For realization of high SBHs, optimization of the electrochemical process was made on InP, changing
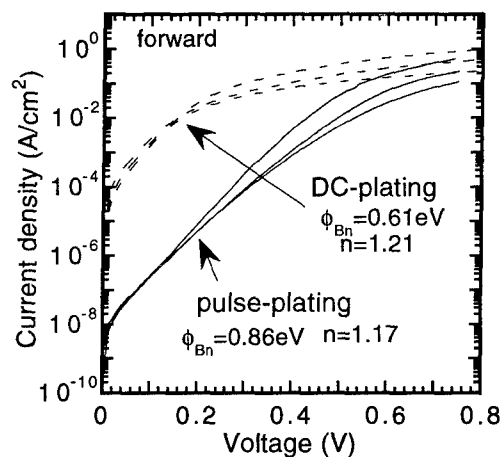
Fig. 3 Forward I-V Curves of Pt/n-InP diodes.

electrical supply waveforms and Schottky metal species.

According to observation by AFM and SEM, the topography of the electrodeposited InP(100) surface was found to be very sensitive to the electrical supply waveforms. For example, SEM image taken on the initial phase of d.c. deposited and pulse deposited InP surfaces are shown in Figs.2(a) and (b). As seen in Fig.2(a) and (b), small Pt grains with a diameter of 30-300nm are formed. The shape and size of the Pt grain are determined by the electrical supply waveforms and metal species. Further deposition does not increase the grain size but increases the number of saturated grains, as shown in Figs.2(c) and (d), which eventually merge and produce a relatively smooth surface. However, grain size, their uniformity and existence of or non-existence of islanding were formed to be extremely sensitive to electrical waveforms and metal species. Most homogeneous surface with small grains were obtained in this study by the pulsed model with V_{hd}=1.0V, t_{pd}=0.4ms and t_{wd} 4μs as shown in Fig.2.

B. Electrical characteristics of Schottky diodes

Corresponding to the difference in surface morphology, large dependence of SBH on electrical supply waveform was observed. As an example, Fig.3 shows the I-V characteristics of Pt/n-InP Schottky diodes formed by the d.c. and pulse electrochemical process. These data were taken on the Schottky diodes whose surface morphology is shown in Fig.2(c) and (d). Pulse-plated diodes gave approximately 300meV higher SBHs than the d.c. plated diodes.

The metal dependence of SBH measured on pulse-plated n-InP Schottky diodes is shown in Fig.4. As seen in Fig.4, SBH is strongly dependent on metal, indicating that Fermi level pinning is largely relaxed in these diodes. The largest SBH was obtained by plating Pt which has the largest metal workfunction of 5.65eV.

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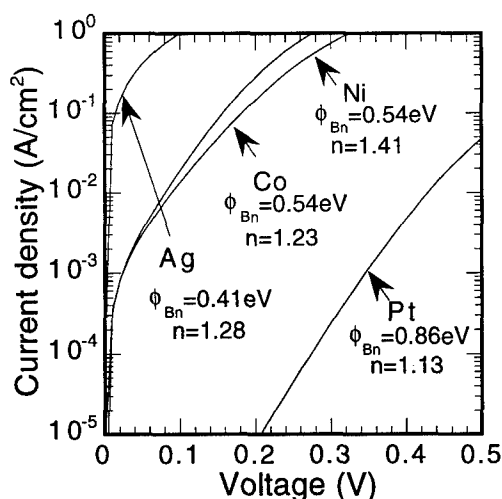
Fig.4 Metal dependence of I-V curves on the pulse-plated
n-InP Schottky diodes.
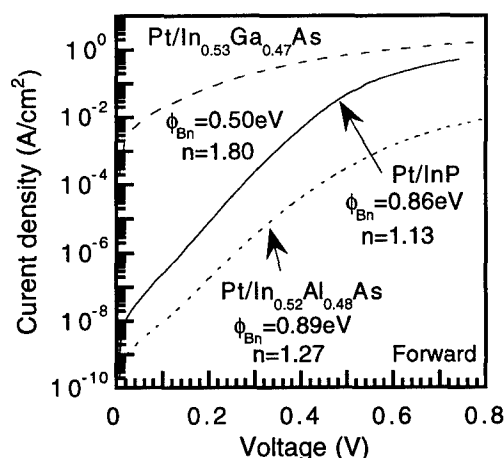
Fig.5 Typical I-V curves of Pt Schottky diodes for
InP-related materials.

C. Application of Optimal Pulse Plating to InP based materials.

The empirically optimized pulse plating process of Pt was then applied to $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$. The resultant I-V curves including those for InP are summarized in Fig.5.

All of the Schottky diodes formed by the electrochemical process showed nearly ideal thermionic emission characteristics.

The electrochemical process for InP achieved a high SBH of 0.86eV with a small n value of 1.13. This SBH value of the electrochemical diode agreed with that obtained by C-V method. This indicates that the electrochemical process realizes intimate Schottky contacts without near-surface modification of the band profile.

For Pt/n-$In_{0.52}Al_{0.48}As$ diode, an enhancement SBH value of 0.89 eV with a low n value of 1.27 was realized by the electrochemical process. This is much higher than the conventional value of 0.60eV.

Similarly for Pt/n-$In_{0.53}Ga_{0.47}As$, the electrochemical
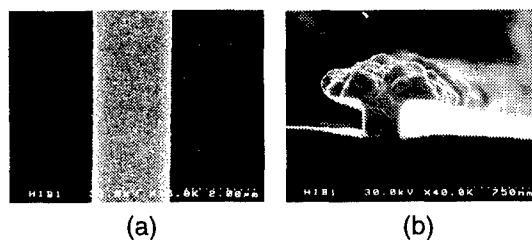
Fig.6 SEM images of Pt gates with (a) 2-μm and
(b) 0.4-μm patterns.

process also produced a high SBH value of 0.50eV. This is much higher than the conventional value of 0.20eV.

D. Application to fine gate formation

In order to see the feasibility of the present electrochemical process for applying fine gate formation for FET devices, Pt gates were formed on HEMT wafers by the optimized-pulse electrodeposition process where the smallest grain size and uniformity were achieved. SEM images of Pt gates are shown in Fig.6(a) and (b) for gate lengths of 2μm and 0.4μm, respectively. As shown in Fig.6(a), Pt is plated following 2μm gate pattern. On the other hand, mushroom type gate was formed very simply in the case of 0.4μm gate pattern by increasing the plating time, as shown in Fig.6(b). These results show that the present process is very promising for fine gate formation on InP-related materials.

III. M-S Interface Analysis and Possible Mechanism of SBH

A. XPS and Raman study

In order to understand the mechanism for the observed SBH enhancement, XPS and Raman studies were performed to the Pt/n-InP contacts formed by the electrochemical process.

XPS in-depth profile analysis using Ar ion sputtering indicated that an intimate contact without interfacial oxide layers is realized by the electrochemical process.

The Raman spectra obtained from the Pt-electroplated surfaces are shown in Fig.7. As shown in Fig.7, no appreciable Raman shift of InP LO phonon peak was observed from the electroplated surfaces. Since Raman shifts are related to the presence of stress, this result shows that the surface formed by the electrochemical process is remarkably free from stress.

B. Possible mechanism for enhancement of SBH

The SBH values determined from I-V characteristics in this study for InP are plotted vs. metal workfunction in Fig.8. Previous data[1] we obtained by vacuum deposition are also indicated in Fig.8. In this study, much enhanced SBHs were realized on n type-InP-based materials by the in-situ electrochemical process, particularly pulse-plated Pt.

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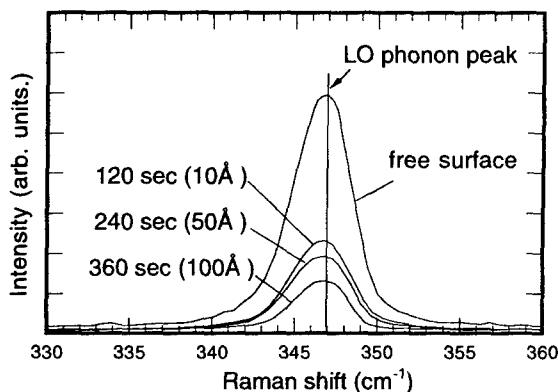
Fig.7 Raman spectra of the pulse-plated Pt/InP interfaces
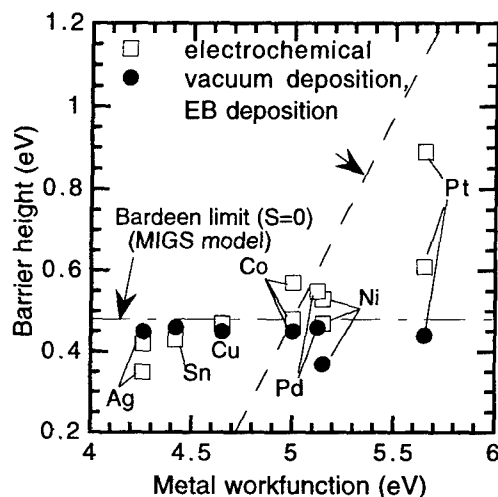
Fig.8 Metal workfunction dependence of SBHs for n-InP

Fig.9 Disorder induced gap state (DIGS) model

The DIGS continuum has continuous energy and spatial distribution of gap states of acceptor type and donor type with a charge neutrality level E_{HO} as shown in Fig.9(b). The position of E_{HO} agrees with that of the charge neutrality level in the MIGS model.

Since the EB evaporation process for the formation of the M-S contacts namely possesses a high processing energy, large disorder is produced at the semiconductor surface due to high-energy metal atoms. Such a process produces high-density DIGS states which pin the Fermi level at E_{HO}. On the other hand, the electrochemical process needs only 500-700meV as the processing energy which is much lower than that of the EB evaporation process. In the initial phase of the Pt plating on n-InP, nm-size Pt grains were formed with no indication of large island formation through the migration of metal atoms and such situation produced a damage- and stress-free interface as indicated by the Raman study. This realizes a nearly pinning-free situation where the DIGS density becomes low by the electrochemical process.

According to the metal induced gap state (MIGS) model.[3,4], which is most widely accepted at present, penetration of the evanescent metal-wavefunction into the semiconductor produces the gap states and causes the Fermi level pinning. The MIGS model explains the SBH values formed by the standard vacuum deposition process, but can not explain the present enhanced SBH.

One possible explanation for the high SBH values is the formation of some kind of interfacial layer which provides additional dipoles. However, the present XPS studies clearly showed that the electrochemical process produced the intimate M-S contacts without any oxide layers. Furthermore, the agreement SBH values obtained between I-V and C-V methods indicated that these diodes possessed no transition layer which modifies the band profile at the interface.

We believe that the highly process-dependent result can be explained by the disorder induced gap state (DIGS) model[5,6] for Fermi level pinning.[7] According to the DIGS model, the formative process of the M-S interface induced a disordered semiconductor layer with the DIGS continuum near the M-S interface as shown in Fig.9(a).

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Real-time Monitoring of Heteroepitaxial $Ga_xIn_{1-x}P$ Growth on Si(001) by P-Polarized Reflectance

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Abstract

We report the application of the real-time optical monitoring techniques p-polarized reflectance (PR) and laser light scattering during low temperature growth of epitaxial $GaP/Ga_xIn_{1-x}P$ heterostructures on Si(001) and GaAs(001) substrates by pulsed chemical beam epitaxy (PCBE). The high surface sensitivity of PR allows to follow growth processes with sub-monolayer resolution during the sequential precursor exposure of the surface that causes periodic alterations in composition and thickness of a surface reaction layer (SRL), the effect of which is monitored by PR as a periodic fine structure. This fine structure is superimposed on interference fringes, resulting from back reflection at the substrate-layer interface with increasing layer thickness. The amplitude modulation and the turning points in the fine structure are accessed and compared to experimental results, showing that an average complex dielectric function of an ultra-thin SRL can be quantified, independent of the average thickness of the surface reaction layer. The PR response during the growth of $Ga_xIn_{1-x}P$ correlates as a function of the interference fringe position with the Ga:In composition.

Introduction

The increasingly complexity of electronic and optoelectronic structures and the trend toward smaller device dimensions requires more stringent tolerances in the control of thickness and composition of tailored artificial materials and structures. The understanding of surface reactions chemistry during the deposition process involving organometallic chemical precursor molecules becomes essential for optimizing the growth process. Surface-sensitive optical real-time sensor techniques are very well suited for this task since their application is not limited to a high vacuum environment. Optical real-time process techniques have been successfully applied during the last decade, focusing on the monitoring of either bulk-film properties [1-4] or surface processes by reflection high energy electron diffraction (RHEED), or reflectance difference spectroscopy (RDS[5-7]). For the characterization of both, bulk and surface, we added recently p-polarized reflectance spectroscopy (PRS) and demonstrated its capability during pulsed chemical beam epitaxy (PCBE) of III-V heteroepitaxial growth. Single wavelength PR and laser light scattering (LLS) data are obtained simultaneously during heteroepitaxial film growth under pulsed chemical beam epitaxy conditions, as described previously [8-13].

Experimental

PR and LLS data are simultaneously obtained to monitor heteroepitaxial film growth under pulsed chemical beam epitaxy conditions. The surface of the substrate is exposed to pulsed ballistic beams of tertiary-butyl phosphine [TBP, $(C_4H_9)PH_2$], triethylgallium [TEG, $Ga(C_2H_5)_3$] and trimethylindium [TMI, $In(CH_3)_3$] at typically 350°C-400°C to accomplish nucleation and overgrowth on Si or GaAs substrates by an epitaxial GaInP film. The fluxes of the pre-

cursor and hydrogen are established by mass flow controllers and are directed via computer-controlled valves to either the reactor chamber or a separately pumped bypass chamber. The switching of the sources is synchronized with the data acquisition of the PR (λ=632.8nm at 75 deg) and LLS signals in order to correlate the changes in the reflected intensity to the changes in the optical properties of the heteroepitaxial stack that encompass chemistry-induced changes in the surface composition and changes due to the thickness and optical properties of the epitaxial film. Typical growth rates under the chosen pulsed chemical beam epitaxy (PCBE) growth conditions are in the order of 1Å/s, with TBP:TEG flux ratios in the range 30:1 to 40:1 and a constant hydrogen flux of 5 sccm in the background. The GaAs substrates are ex-situ chemically etched in Br:Methanol (0.02%) solution, follow by a DI-$H_2$0 rinse, a NH_4OH:$H_2$0 (1:1) dip and a final DI-$H_2$0 rinse prior loading in the growth chamber. Further details on the experimental conditions are given in previous publications[8-11,14-17].

Results and Discussion

Figure 1 shows a typical evolution of the PR signals during GaP growth on a Si(001) substrate. The pulsed supply of the precursor causes of fine structure oscillation in the PR signal (see insert in fig. 1) which can be analyzed in more detail using the first derivatives of the PR signals. In the experiments here, the precursor cycle sequence is 3 sec, composed of a TBP pulse (0.0-0.8 s), a pause, a TEG pulse from 1.5-1.8 s, followed by a second pause. A continuous flow of H_2 (5 sccm) is supplied during the complete cycle sequence.

The fine structure observed in the PR signal can be understood as the optical response to the alternative supply of precursors, where one oscillation in the fine structure corresponds to a complete precursor cycle. The start of an oscillation (marked with dashed lines in the insert in fig. 1) coincides with the leading edge of the first precursor pulse in the cycle sequence. As shown in fig.

1, the amplitude in the fine structure undergoes periodic changes during deposition time. The amplitude increases on the raising flank of the interference oscillation with a maximum at the top, and then decreases on the falling flank. The relative locations of these decreases and increases in the fine structure amplitude and the film interference oscillation strongly depend on the chosen growth conditions, such as precursor pulse width and height, pulse sequence time, or supply of additional activated hydrogen. Characteristic features can be identified using the first derivative of the PR signals, shown in fig. 1.
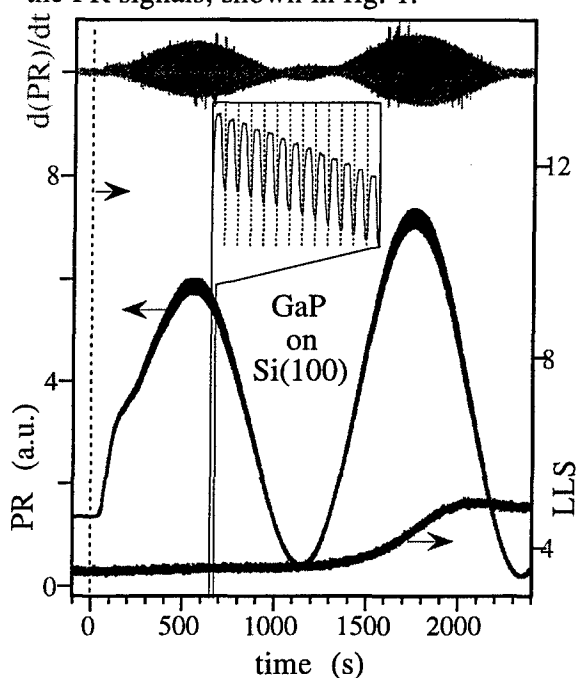
Figure 1: PR, LLS and d(PR)/dt evolution for heteroepitaxial GaP growth on Si under PCBE conditions at 350°C. PR is monitored under an angle of 75 deg. The insert shows an enlargement of the fine structure as a response to the sequential precursor exposure of the surface

The envelope function of d(PR)/dt reveals two important features: (1) the zero crossing points in d(PR)/dt mark the positions where the response to the first precursor pulse changes sign (turning points) and (2) during steady-state growth conditions, the d(PR)/dt envelope evolution undergoes period

oscillations, where one oscillation consists of a long period with a large amplitude and a short period with a small amplitude. The ratio of these periods and their amplitude depends on the chosen precursor dose and exposure times.

The mathematical modeling of the fine structure under the simplified assumption of a periodically in phase modulated SRL with an average dielectric function $\hat{\epsilon}_1$[11,18] describes the overall observed evolution of the PR signal, using Fresnel's equations and a four-layer (ambient / surface layer / film / substrate) stack model. A more detailed model that accounts for changes in both thickness and dielectric function of the SRL during one precursor cycle, requires a correlation of structure in the PR intensity to changing of defragmentation products and their concentrations in the surface reaction layer, which is discussed in more detail elsewhere [19].

Figure 2 shows the simulated four layer stack reflectivity, $R_4(t)$, built up by the substrate Si with $\epsilon_3(\lambda=632.8nm)$ = (15.25, 0.17), the growing GaP film with $\epsilon_2(\lambda=632.8nm)$ = (11.1, 0.01) and an average growth rate of 0.85Å/sec, a periodically modulated SRL with $\epsilon_1(\lambda=632.8nm)$ = (9.5, 2.5) and a maximal thickness of $d_{1max}=5$Å, and an ambient with ϵ_0= 1. Also drawn in are the calculated difference between the four-layer and the three layer stack reflectance, $[R_4(t)-R_3(t)]$, and the derivative $dR_4(t)/dt$. The values for the average dielectric function of the SRL are chosen such that it matches typical experimental results for GaP on Si(001) monitored at an angle of incidence of 75 deg (see fig. 2). Under these specific growth conditions $Re(\epsilon_1)$ is smaller than $Re(\epsilon_2)$ with a significant absorption of $Im(\epsilon_1) = 2.5$.

Figure 3 shows the temporal evolution of the PRS and LLS signals during the growth of $Ga_xIn_{1-x}P$ on Si(001). The flow ratio TMI:TEG was set nominally 1:4 with a TEG:TBP ratio 1:40. The cycle sequence time is 6 sec, where the surface is sequentially exposure to two TBP pulses from
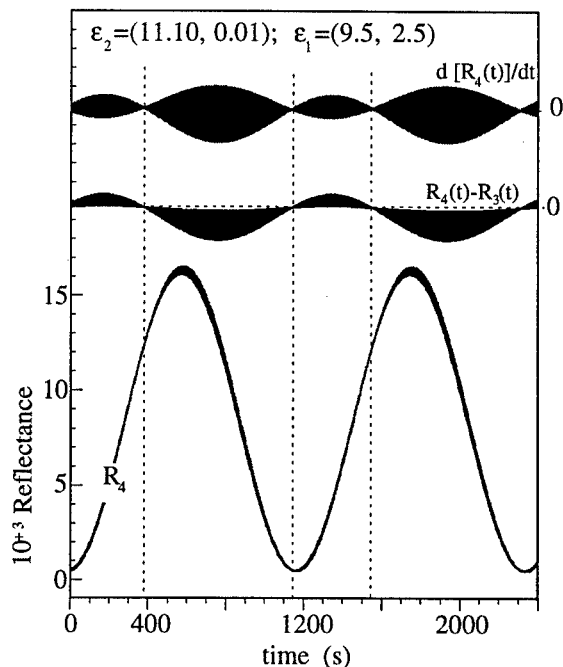
Figure 2: Simulation of the temporal evolution of the PR signal in a four layer stack model. Also shown are the first derivative of the PR signal and SRL contributions to the reflectance (see text).
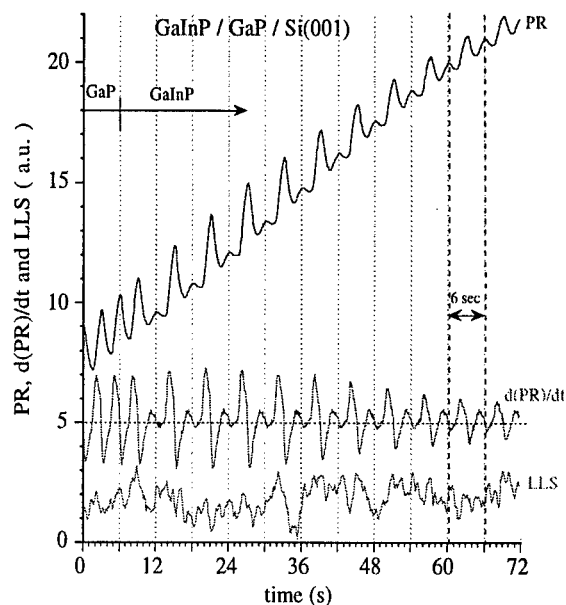
Figure 3: PR, LLS and d(PR)/dt evolution during $Ga_xIn_{1-x}P$ growth on Si substrate at 400°C.

0.0-0.8s and 3.0-3.8s, one TEG pulse from 1.5 - 1.8 s and one TMI pulse from 4.5 - 4.8 s. Also shown (lower curve) is the evolution of the LLS intensity during the deposition

process and the derivative, $dR_4(t)/dt$, of the PR signal. The begin of each cycle sequence is marked by a dashed line.

Fig. 4 shows the evolution of the PR signal during the growth of lattice-matched $Ga_{0.5}In_{0.5}P$ on GaAs(001) (flow ratio TMI:TEG=1:1), the first derivative of the PR signal and the precursor cycle sequence. The begin of each cycle is marked by a solid line and the begin of a precursor pulse as a dashed line. The fine structure amplitude differs for the TEG and TMI exposure due to their different induced SRL thickness and SRL composition. The PR response to the TMI is increased compared to the PR response shown in Fig. 3, where the flow ratio TMI:TEG was =1:4. Comparison with ex-situ composition analysis[17] shows that the ratio of PR responses to TMI and TEG exposure correlates with the Ga:In composition. However, since the PR response-ratio for a given Ga:In composition depends on the position of the PR interference fringe, a simulation of the PR signal over an extended interference fringe is required to extract the composition of the film.
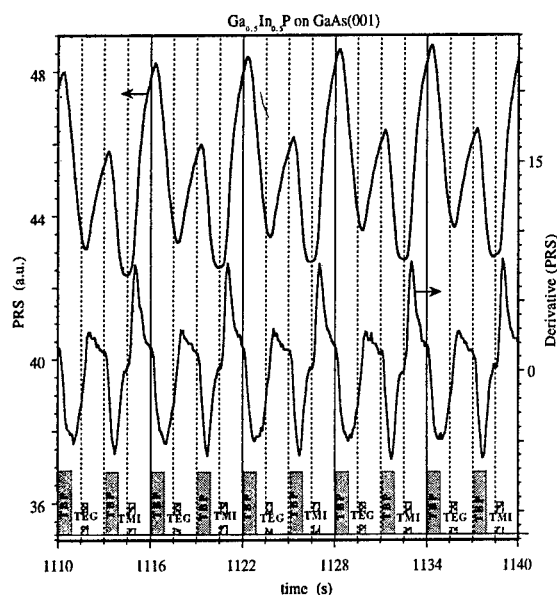
Figure 4: PR, LLS and d(PR)/dt evolution during GaInP growth on GaAs substrate at 400°C.

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NEW SCANNING PHOTOLUMINESCENCE TECHNIQUE FOR MAPPING THE LIFETIME AND THE DOPING DENSITY : APPLICATION TO CARBON DOPED InGaAs/InP LAYERS AND HETEROSTRUCTURES

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Introduction

Lifetime and doping characterization of selected layers in epitaxial structures as, for example, p-doped layers encountered in the base of Heterojunction Bipolar Transistors (HBTs) is of great importance for the successful development of these devices. Various techniques exist for the evaluation of such characteristics, including time-resolved photoluminescence and Hall measurements. There is, however, lack of a single, fast, non-destructive, quantitative technique that can provide combined lifetime and doping information and that allows, in particular, spatially resolved measurements with high resolution, as well as, wafer-scale mapping evaluation. This paper addresses these issues and demonstrates the feasibility of the proposed approach by successfully applying it to carbon doped InGaAs.

I. Background

Carbon doped (p-type) InGaAs/InP heterostructures are of great importance for the development of reliable high performance HBTs necessary for microwave systems and Optoelectronic Integrated Circuits (OEICs). This is due to low diffusion rate of C-atoms during the epitaxial growth of complex structures, device processing and operation (1-4). However, carbon is of amphoteric nature and the presence of hydrogen reduces carbon incorporation and passivates the incorporated C-acceptors (2-5). Consequently, the growth of InGaAs(C) strongly depends on both the growth method and conditions (3,5). In addition, in such a complex situation, a possible anisotropy of the growth parameters (susceptor temperature, hydrodynamic pattern and other reactor geometrical effects) may critically affect lateral uniformity of the deposited layers. Therefore, the properties and the uniformity of InGaAs(C) layers must be tightly controlled in order to optimize the growth conditions and to ensure best process quality and reproducibility.

The characterization technique proposed in this work permits to address the above issues as shown by its application to the spatially resolved evaluation of minority-carrier lifetime and doping density of single InGaAs(C) layers on InP substrates and InP/InGaAs(C)/InP heterostructures. Both, high spatial resolution (about 1 μm) and wafer scale mappings were carried out with a large number of measured points (e.g. 200 x 200).

II. Principle

The principle of our new method is based on Spectrally Integrated Scanning Photoluminescence (SI-SPL) measurements carried out at room temperature at few different excitation levels (6). The data obtained are treated by theoretical models of the PL emission, developed due to numerical solution (3D modeling) of the continuity equations with the boundary conditions adapted to the type of the examined structure. In order to accelerate the data treatment procedures, in the case of cartographic measurements with a large number of measured points, we also developed analytical models based on the approximation of the 3D simulation results. These models are useful not only for low resolution measurements (when the excitation spot is much larger than the diffusion length, the one dimensional ambipolar continuity equations can be applied and usually solved analytically) but, in particular, for high resolution measurements, when the lateral diffusion of carriers cannot be neglected (laser spot comparable or lower than the diffusion length). By fitting the theoretical curve to the measured data (PL intensity vs. excitation level for each point of the surface), the spatial distribution of both the lifetime and the doping density can be determined and plotted. This is due to the fact that in InGaAs(C) with moderate doping ($<10^{18}$cm^{-3}) both contributions of the linear and of the quadratic regimes to the PL signal can be easily observed. We have shown previously (6,7) that the

quadratic response of the PL intensity depends mainly on the effective carrier lifetime and the linear response depends both on the carrier lifetime and doping density. Thus, these two parameters can be extracted. In the case of samples with higher doping ($>10^{18}cm^{-3}$), the contribution of the quadratic regime is very weak. However, taking into account the predominant effect of the Auger recombination in highly doped InGaAs layers (with reasonably good quality), these two parameters can also be extracted only from the linear part of the PL signal. For calculations, we used the unsaturated Auger recombination model (8).

III. Experimental

A. Samples

Experiments were carried out on InGaAs(C)/InP and InP/InGaAs(C)/InP heterostructures grown by:

1) Chemical Beam Epitaxy (CBE) ; triethylgallium, trimethylindium and precracked arsine and phosphine were used as group III and group V sources ; the source of carbon was carbontetrabromide.

2)Low-Pressure Metal Organic Chemical Vapor Deposition (LP-MOCVD) in a vertical mass transport reactor ; all-methyl metal organic sources (TMIn, TMGa) were used for group III sources and arsine for group V ; liquid CCl_4 was used as a carbon source with H_2 as a carrier gas. Some of these samples were post-growth annealed (600°C, 10sec, Ar atmosphere).

B. Measurements

The SI-SPL measurements were carried out at room temperature using SCAT SPEC IMAGEUR of SCANTEK (France). The PL signal was excited with an He-Ne laser (minimum spot size below $1\mu m$), spectrally integrated using broad band interference filters and detected with a wavelength extended InGaAs photo-detector. The SPL measurements were performed at few different excitation levels, which were selected by an acousto-optic device. The data obtained were stored in a four dimensional matrix (x-position, y-position, excitation level, PL intensity) and treated by the dedicated software. In particular, by fitting the theoretical function to the experimentally obtained PL intensity vs. excitation level, for each point measured on the surface, the spatial distribution of both the carrier lifetime and the doping density were extracted and plotted.

The developed technique was validated by comparison with the lifetime obtained by time resolved photoluminescence, excited by a mode locked Ti-Sa laser and detected with a synchroscan streak camera. The doping density were also evaluated by both SIMS and Hall effect measurements.

IV. Results and discussion

Examples of the results obtained on InGaAs layers with moderate doping ($3x10^{17}cm^{-3}$) are shown in Figs. 1 and

2. Figs. 2a and 2b indicate clearly the contributions of both linear and quadratic regimes to the PL signal in these layers. The slope of the lines shown in Fig. 2b depends on the lifetime, whereas their intersection with the I_{PL}/I_{ex} axis depends on both the lifetime and the doping density.
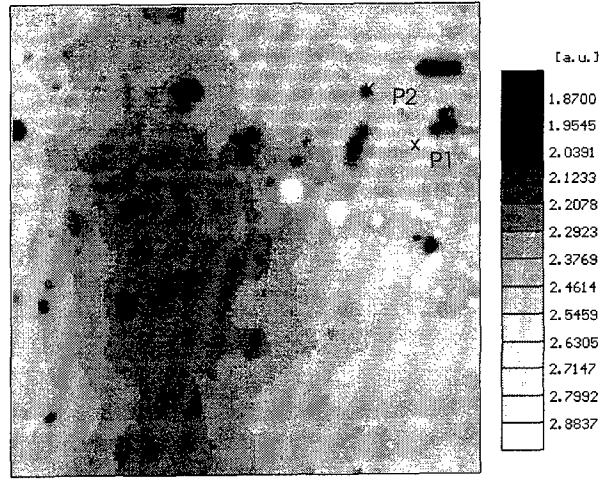
Fig.1. Spectrally Integrated SPL image obtained on an InP/InGaAs(C)/InP structure (with moderate C-doping) grown by CBE. The dark spots in this figure correspond to the presence of threading dislocations (7). The origin of the bright spots in this particular sample remains unknown.
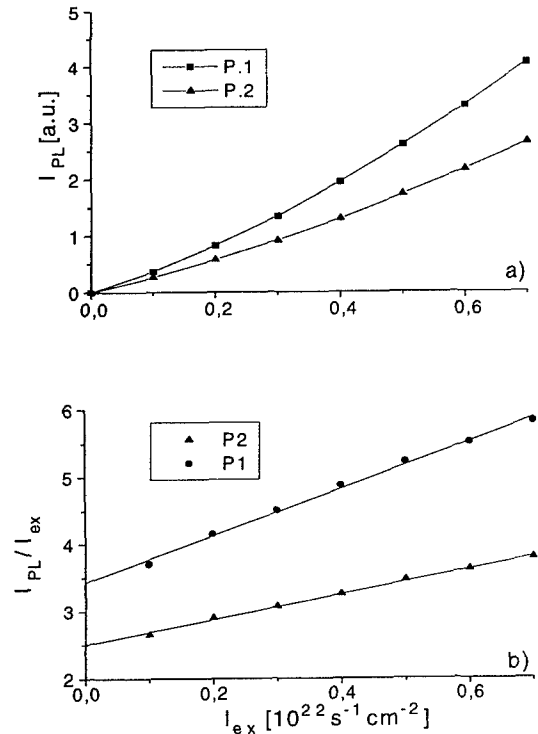
Fig. 2 (a) PL intensity (I_{PL}) and (b) normalised PL intensity (I_{PL}/I_{ex}) plotted vs. excitation level (I_{ex}) for two different points on the surface (P1 and P2 indicated in Fig. 1). This InP/InGaAs(C)/InP structure with a moderate doping was grown by CBE.

Thus, in agreement with our theoretical model, the local lifetime of minority carriers can be determined from the slope of the linear approximation of the measured data, plotted in the scale I_{PL}/I_{ex} vs. excitation level (I_{ex}) and, consequently, the local doping density can be calculated from the intersection of this line with the I_{PL}/I_{ex} axis.

The results of complementary measurements (PL transient, Hall) of the average lifetime and of the doping density on this sample were in good agreement (within 20%) with those obtained by our new SPL technique.

The results of high resolution measurements obtained on the same sample (Fig. 3) indicate that close to threading dislocations, the effective lifetime of carriers decreases but the doping density remains unchanged.
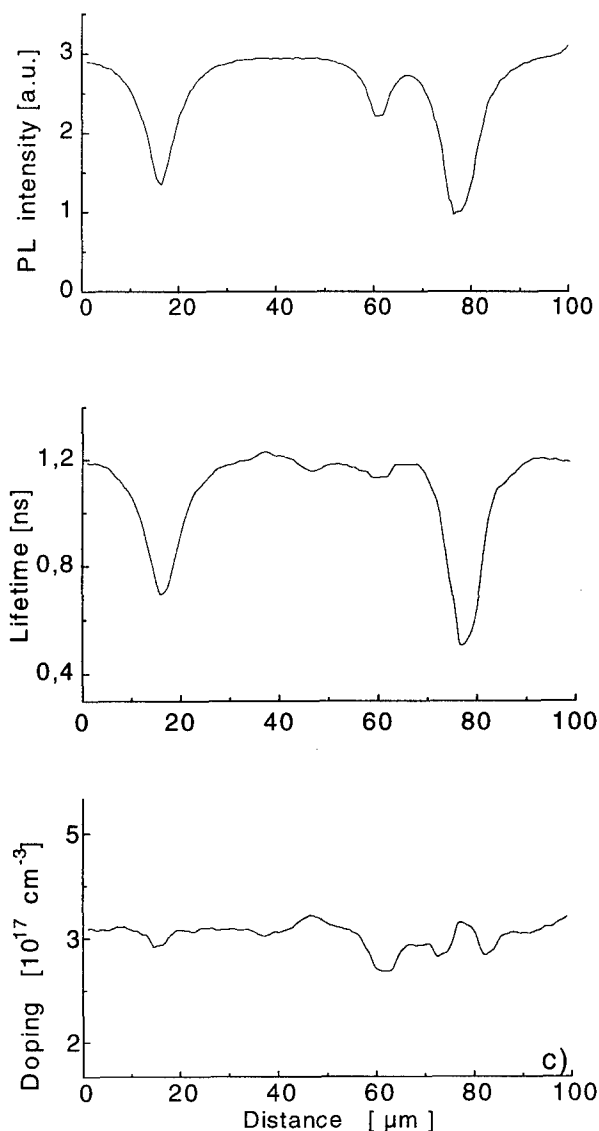
The results shown in Fig. 4 summarize the average lifetime and doping values obtained on InGaAs(C) layers (about 0.5 μm thick) grown by MOCVD on InP substrates. The lifetime of minority carriers in these layers was calculated from SPL data using two different models. We supposed first that the effective non-radiative lifetime in the layers is dominated by bulk recombination (low surface recombination velocity « s »). We also made the assumption of a high, diffusion limited, surface recombination velocity. It appears from Fig. 4, that post growth annealing of MOCVD InGaAs(C) layers induces both, an increase of the bulk non-radiative lifetime and of the surface recombination velocity. In addition, we found in post growth annealed samples (these results are not shown here) significant changes of the morphology of SI-SPL images and a decrease of the overall PL intensity. Thus, post growth annealing reduces the density of bulk recombination centers, however, it also results in thermally induced surface degradation (7).

An increase of the hole mobility was already observed after annealing of MOCVD grown InGaAs(C) layers (4, 5), which indicates that complex defects involving excess hydrogen may contribute to the majority carrier scattering. These defects may also act as non-radiative recombination centers. Thus, the observed increase of the lifetime in the bulk of post growth annealed InGaAs layers could be explained by the reduction of the density of complex defects involving excess hydrogen.

The effect of annealing on the lifetime of minority carriers in the bulk of MOCVD InGaAs(C) layers is of minor importance in highly doped samples (the lifetime of carriers is usually dominated by Auger recombination) and in the layers grown by CBE (lower incorporation of hydrogen atoms at our growth conditions).
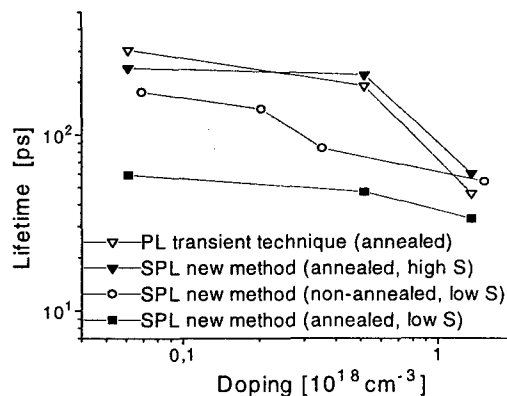
Fig.4. Average lifetime measured by our SPL method and by PL transient technique on InGaAs(C)/InP samples with various C- doping (MOCVD growth).

Fig.3. Distribution of the PL intensity, of the extracted lifetime and of the doping density across a line which cross threading dislocations (which corresponds to low PL signal). This InP/InGaAs(C)/InP structure was grown by CBE.

In highly doped samples ($>10^{18}$cm^{-3}), the lifetime of carriers is controlled by Auger recombination. Also in the case of such samples we found a good agreement between the lifetime and the doping density determined by our SPL method and by transient PL techniques (Fig. 5). An example of cartographic measurements is shown in Fig. 6.
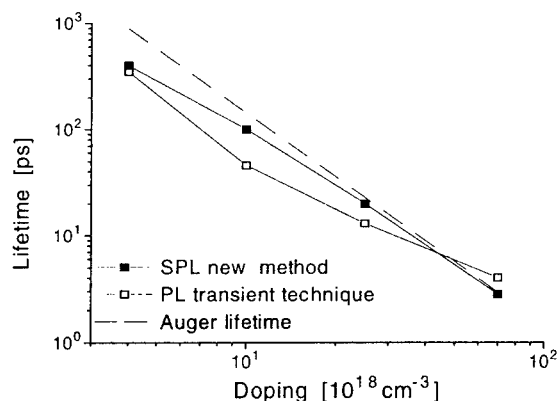
Fig.5. Average lifetime measured by our SPL method and by PL transient technique on heavily C-doped InP/InGaAs(C)/InP samples (CBE growth). The Auger lifetime was calculated as in Ref.(8).
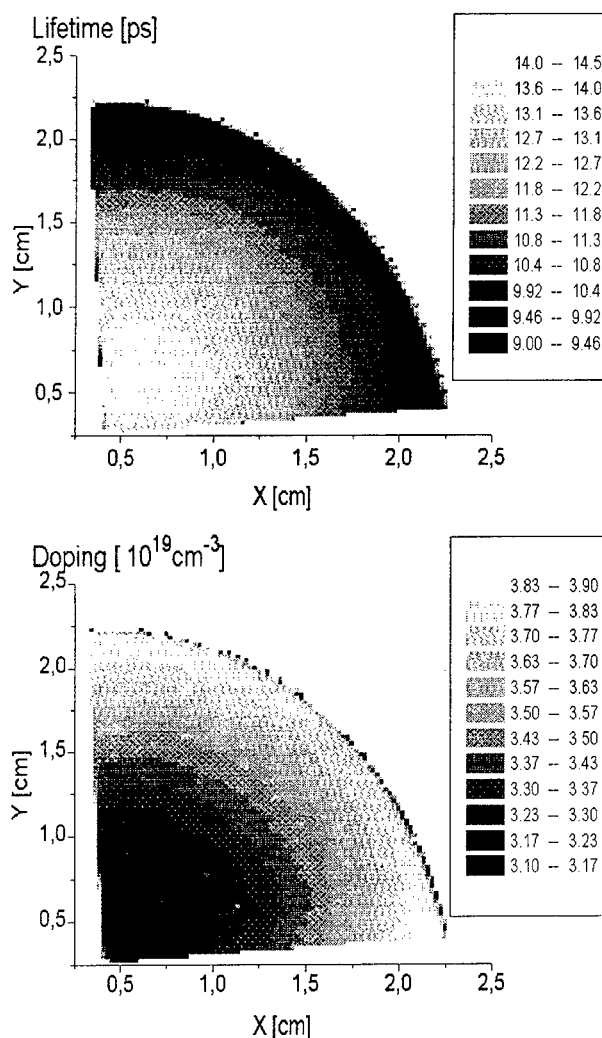
Finally, we found good agreement between the average hole concentration deduced from our SPL technique and complementary measurements (SIMS, Hall) performed before and after post growth annealing of MOCVD grown InGaAs(C) samples. The observed increase of hole concentration, can be attributed to hydrogen de-passivation of C-acceptors (3-5) and possibly the displacement of carbon atoms from group III site to V site (5).

V. Conclusions

We introduced and validated here a new scanning photoluminescence method for mapping the lifetime and the doping density in Carbon doped InGaAs layers and InP/InGaAs/InP heterostructures. High spatial resolution (about $1\mu m$) and wafer scale mappings can be carried out at room temperature in a fast and non-destructive way. The technique covers a wide range of C-doping levels (up to $10^{20}cm^{-3}$) and of lifetime values (down to $10^{-12}s$).

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Fig.6. Lifetime and doping mapping measured by our SPL technique on an InP/InGaAs(C)/InP structure (CBE growth).

PHOTOLUMINESCENCE AND RAMAN PROPERTIES OF MOCVD-GROWN $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ LAYERS UNDER DIFFERENT GROWTH CONDITIONS

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Introduction

Two sets of $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P/GaAs$ were prepared by metalorganic chemical vapor deposition, and a combined photoluminescence (PL) and Raman scattering investigation was performed. Variations of PL bands and Raman lines were observed from one set of samples with x~24% and grown with different pressures and dopants. Both the PL and Raman measurements confirmed the Al-compositional variations of the second set of samples, with x~18% and grown under different low pressures and H_2 flows, to be around 1%. It is found that the Raman spectral features are more sensitive to the epitaxial growth parameter variations. The line shape analysis leads to information about the sample crystalline quality and the optimum growth conditions, which is coincident with the qualitative analysis of the growth process. This study offers us a useful way to optimize the parameters to produce high crystalline quaternary InGaAlP materials.

I. Background

The quaternary alloy $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$, lattice-matched with GaAs substrate, has a direct band-gap transition in the wavelength range between green and red and is very useful for optoelectronic applications such as visible light emitting diodes (LEDs) and laser diodes (1-2). A great deal of effort has been made for the growth and investigation of this important quaternary semiconductor and its device applications in recent years. Atomic ordering occurs under certain conditions during the epitaxial growth of InGaAlP by metalorganic chemical vapor deposition (MOCVD), resulting in the reduction of the alloy bandgap and the room temperature (RT) photoluminescence (PL) emission peak (3). It is important to control and optimize the growth conditions to produce high quality InGaAlP epilayers, which is the task of this study.

II. Experimental

The epitaxial growth of InGaAlP was performed by low pressure (LP) MOCVD using two EMCORE *TurboDisc* systems: Discovery 180 (D180) and Enterprise 400 (E400). These systems employ the vertical growth configuration and a high speed rotating disk able to handle multiple wafers. The system design was made according to hydrodynamic symmetry and flow dynamics of the rotating disk reactor (RDR), which ensures growth to be laterally uniform, abruptly switchable, and robust against variations in process parameters. High purity trimethyindium (TMIn), trimethygallium (TMGa) and trimethyaluminum (TMAl) metalorganic sources were used to supply In, Ga and Al, respectively, and PH_3 was used for the P source. High purity H_2 was used as the carrier gas. Details can be found in Refs. (4-5). We have grown two sets of $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ films on (100) n^+-GaAs substrates oriented 15° off towards (110), under different growth conditions. The film thickness varied between 0.8-1.1 μm, and were determined by optical reflectance interference fringes and scanning electron microscope cross-sections. The growth parameters for these two sets of experimental samples appear in the figures and text of next section.

Room temperature (RT) photoluminescence (PL) was measured by a home-made system consisting of an Ar^+ laser (514.5 nm), a single grating spectrometer (HR 640), photomultiplier tube, and lock-in amplifier detection electronics. Raman scattering was performed in the backscattering configuration with the excitation of 632.8 nm from a He-Ne laser by a Renishaw Raman Microscope-100.

III. Results and Discussion

Figure 1 shows the RT PL bands of four $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ films (x~24%) grown on GaAs with a growth temperature of 690°C and under different pressure, τ, and dopant conditions. It can be seen that the PL peak of Si-doped InGaAlP shifts towards the shorter wavelength (higher energy) slightly as the growth pressure increased from τ = 35 to 55 Torr and shifts further more as τ increased to 70 Torr, and that the Si-doped and Te-doped InGaAlP layers grown under the same pressure (55 Torr) have similar PL peak energies but quit different band shapes. Three Si-doped InGaAlP films have PL full width at half maximum (FWHM) values of 62, 60 and 76 meV for τ = 35, 55 and 70 Torr, respectively. Moreover, the Te-doped InGaAlP sample has a smallest FWHM of 44 meV, narrower than all the Si-doped samples, while its PL peak is close to that of the Si-doped InGaAlP grown under the same pressure.
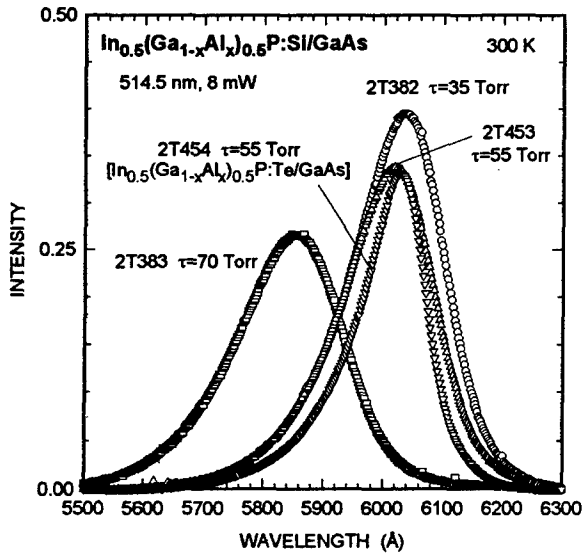
Figure 1   Photoluminescence spectra of three $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$:Si and an $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$:Te grown on GaAs, at 690°C and with different low pressures.

Figure 2 exhibits Raman spectra of these four InGaAlP films, showing four major bands, which are AlP-, GaP- and InP-like longitudinal optical (LO) phonon modes, and an InP-/GaP-like mixed transverse optical (TO) band, respectively (6-7). The different Raman shifts of these peaks reveal the compositional variations among these four quaternary samples. Three Si-doped InGaAlP films have their main Raman bands located at similar Raman shift positions, indicating only a small amount of Al-composition variations. The Te-doped sample apparently has an Al-composition or ordering characteristics quit different from the other three Si-doped samples. For all the four samples in Fig. 2, the forbidden TO modes are stronger than or comparable to the corresponding LO modes in intensity.

Figure 3 shows RT PL spectra from another set of $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ (x~18%) films grown on 15° off (100) n^+-GaAs. They were Si-doped and grown at a higher temperature of ~740°C, under different low pressures and H_2 carrier flows. Table I lists their PL peak positions in eV and FWHMs in meV. The direct bandgap of $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ has the relationship with x (1):

$$E_\Gamma \text{ (eV)} = 1.91 + 0.61x, \qquad (3.1)$$
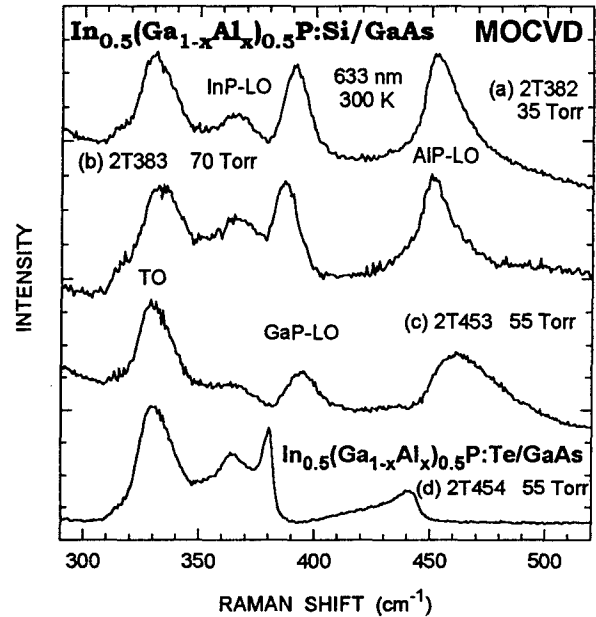
Figure 2   Raman spectra of three $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$:Si and an $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$:Te grown on GaAs, at 690°C and with different low pressures.
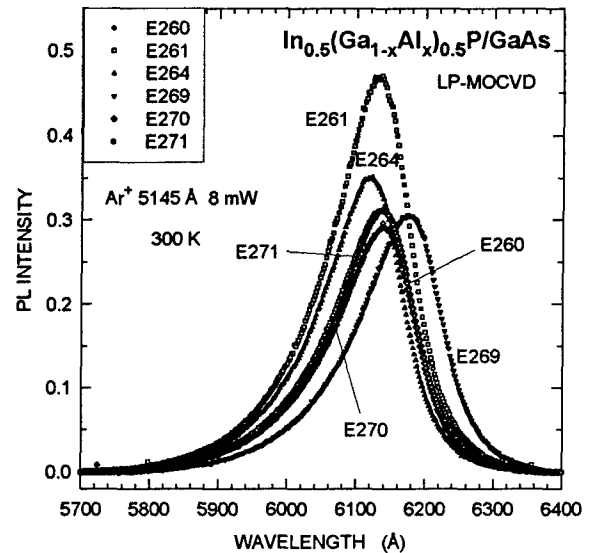
Figure 3   Photoluminescence spectra of six $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ grown on GaAs, at ~740°C and with different low pressures and H_2 carrier flows.

and we may obtain the Al-composition variation with the bandgap and also the measured PL peak as

$$\Delta x = \Delta E_\Gamma / 0.61 = \Delta E(PL\ peak) / 0.61. \qquad (3.2)$$

From the data in Table 1 and using Eq. (3.2), we obtain the x variation of this set of six $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ samples to be less than 1.5%. Their FWHMs are ranging between 44 and 47 meV, smaller than the first set of Si-doped samples. These may be due to that the composition range of the second set is smaller than the first set and that the growth parameters of the second set samples are more optimized. Because the PL bands and FWHM values in the second set of samples vary slightly, we use Raman scattering to further distinguish them.

Table 1. PL data and Raman fits data of E260-E271

Sample	PL (eV)	FWHM (meV)	ω_{GaP-LO} (cm^{-1})	FWHM (cm^{-1})	I_{GaP-LO} /I_{TO}	order of quality
E260	2.019	44.3	383.32	5.54	0.72	{6}
E261	2.022	45.8	383.37	5.20	1.05	{4}
E264	2.025	46.0	383.09	5.04	1.88	{3}
E269	2.008	46.6	383.65	5.45	1.08	{5}
E270	2.019	45.2	383.12	5.05	2.31	{1}
E271	2.020	47.2	383.30	4.92	1.89	{2}
Average	2.017	45.7	383.3	5.2		
error	±0.009	±1.5	±0.3	±0.3		

Figures 4 shows Raman spectra of the second set of $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P/GaAs$ (x~18%) grown at ~740°C with different low pressure and H_2 carrier flow values. Curve fits of Lorentzians on six spectra in Fig. 4 were performed, with an example shown in Fig. 5. In this way, we are able to obtain more accurate Raman line peak positions and integrated intensity ratios. Some of these analytical data are given also in Table 1, such as the frequency, ω_{GaP-LO}, and FWHM of the GaP-LO phonon, and the integrated intensity ratio between the allowed GaP-LO phonon and the forbidden TO phonon, I_{GaP-LO}/I_{TO}. Kondow et al. (7) have studied the frequency dependence of AlP-, GaP- and InP-LO modes on Al composition x of $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ (0≤x≤1) from Raman scattering. From their Figure 4 in (7), we may obtain a variation relationship between the Al composition x and the GaP-LO phonon frequency:

$$\Delta x / \Delta\omega_{GaP-LO} \sim 0.03 / cm^{-1}. \qquad (3.3)$$

Combining with the error bar of GaP-LO phonon frequencies in Table 1, we obtain a variation of x of six $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ samples to be less than 1%, better than but close to our estimation from PL data using Eq. (3.2).

According to the Raman selection rule on a zincblende crystal with the (100) surface, the TO phonon is forbidden and the LO mode is allowed. The disorder or mis-orientation in the measured material may relax the above selection rule (8). Therefore, we may use the intensity ratio between the allowed LO and forbidden TO modes to characterize the film quality (8). Here, the integrated intensity ratio between the allowed GaP-LO phonon and the forbidden TO phonon, I_{GaP-LO}/I_{TO}, is found more varied and sensitive to different growth conditions than the PL and Raman line widths, from Table 1, and therefore, is adopted as a merit of a measure of the crystalline quality of InGaAlP films. A lower I_{GaP-LO}/I_{TO} ratio indicates poorer quality of the sample while a higher I_{GaP-LO}/I_{TO} value indicats better sample perfection. According to this, we list the order of quality for these six InGaAlP films in the last column of Table 1.
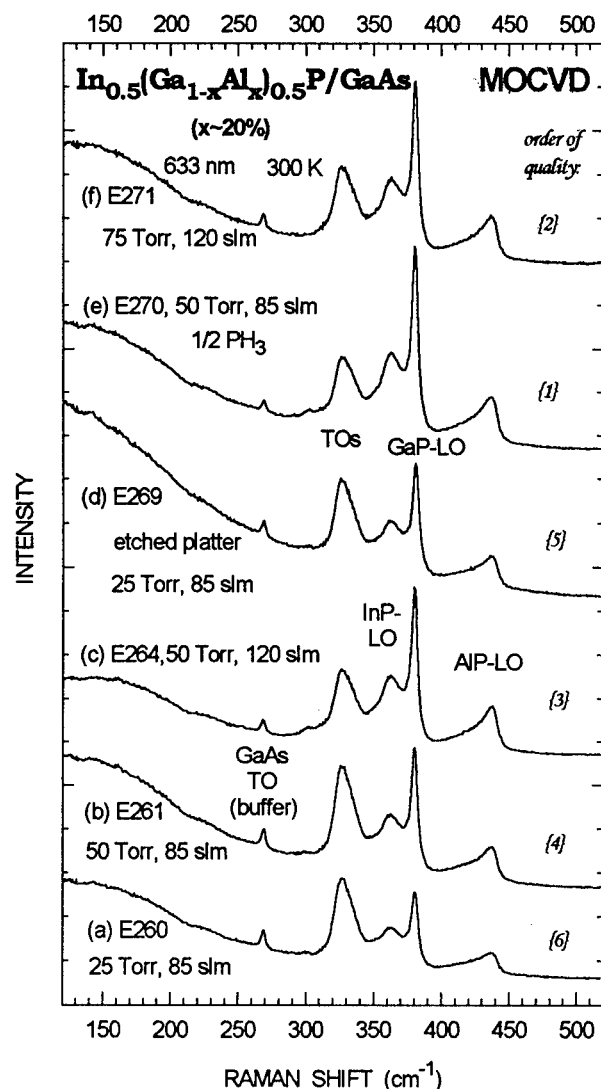
Figure 4   Raman spectra of six $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P/GaAs$ (x~18%) grown at ~740°C with different low pressure and H_2 carrier flow values.
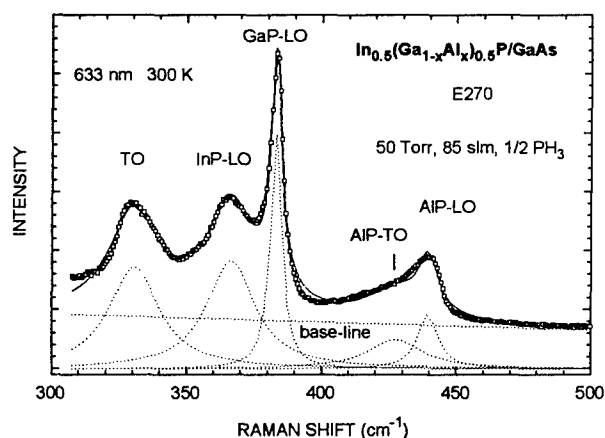
Figure 5   Raman spectrum and Lorentzian fits of an $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P/GaAs$, E270. The open square symbols are the experimental data, the solid line is the theoretical fitting results with its five Lorentian components represented by dot-lines.

    Further qualitative analyses may help us understand this order better. Starting from the spectrum of Fig. 4 (a) with a low pressure of 25 Torr and a H_2 flow of 85 slm, we have the forbidden TO stronger than all the allowed LOs in line intensity, indicating a poor quality of this sample. An increase of the pressure to 50 Torr, keeping a same H_2 flow of 85 slm, in Fig. 4 (b), may enhance the chemical reaction and improve the resulting film quality, leading to the TO mode intensity slightly weaker than the allowed GaP-LO. From (b) to (c), we kept the pressure of 50 Torr, but increased the H_2 flow from 85 slm in (b) to 120 slm in (c). This may further enhance the chemical reaction and improve the film quality, with the I_{GaP-LO}/I_{TO} ratio increasing from 1.05 to 1.88. Keeping a H_2 flow of 120 slm and increasing the pressure from 50 Torr in (c) to 75 Torr in (f), we obtained only a slight improvement of the I_{GaP-LO}/I_{TO} ratio from 1.88 to 1.89. This means that it would not help much as increasing the pressure beyond 50 Torr. Returning to the case (a), we maintained the pressure of 25 Torr and the H_2 flow of 85 slm to be same, but etched the wafer carrier platter which may improve the heat contacts of the wafer with the carrier. As shown in Fig. 4 (d), we have the GaP-LO slightly higher than the TO mode and an I_{GaP-LO}/I_{TO} ratio of 1.08, similar to the case (b) with a small improvement to the case (a). Therefore, re-starting from (b) with a pressure of 50 Torr and a H_2 flow of 85 slm, we decreased the supply of the P source by halving the amount of PH_3, i.e., decreasing the V/III ratio, and we obtained a much improved Raman spectrum in Fig. 4 (e) with the GaP-LO mode much stronger than the TO phonon in intensity and a highest I_{GaP-LO}/I_{TO} ratio of 2.31, indicating the best growth conditions among these six samples.

    In conclusion, we have grown two sets of $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P/GaAs$ with the Al composition of near 24% and 18%, respectively, by low pressure MOCVD

employing the *TurboDisc* RDR technology and performed a combined photoluminescence and Raman scattering investigation on them. Variations of the room temperature photoluminescence band and Raman lines were observed from one set of samples grown with different pressures and dopants. Both PL and Raman measurements confirmed the compositional variations of the second set of samples, grown under different low pressures and H_2 flows, to be near 1%. It is found that the Raman spectral features are more sensitive to the sample growth parameter variations. The line shape analysis of line width and integrated intensity ratio leads to information about the order of the sample crystalline quality and the optimum growth condition. The combined PL and Raman measurements and analysis on LP-MOCVD grown $In_{0.5}(Ga_{1-x}Al_x)_{0.5}P$ /GaAs offer us a useful way to optimize the parameters for the growth of high quality crystalline quaternary semiconductor materials.

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Fluorine Diffusion in Step-doped InAlAs Layers on InP Substrate

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Abstract

The quantitative relation between fluorine (F) accumulation and Si donor concentration in n-InAlAs layers on InP substrate was investigated for several kinds of step-doped InAlAs samples using secondary ion mass spectroscopy. From the depth profile of F and Si donor in a periodic i-/n-InAlAs sample, we found that F accumulates only in n-InAlAs layers, passing through i-InAlAs layers. Also, we found that the amount of F accumulation in an n-InAlAs layer depends on the Si doping concentration. The experimental results can be explained by considering two states of F. In one state, F is bound to a Si donor and immobile, and in the other it is free and can diffuse.

I. Introduction

InP-based heterojunction FETs (HJFETs) have demonstrated excellent DC and RF performance due to high electron mobility at room-temperature and sufficiently large two-dimensional electron gas concentration. Extremely encouraging current gain cut-off and maximum oscillation frequencies in excess of 300 GHz and 600 GHz, respectively, have been reported. [1][2] However their commercial use has been greatly restricted because of thermal instability of their device characteristics. Recently it has been understood that one origin of the thermal instability is fluorine (F) which compensates Si donors in the n-type InAlAs layer. [3-7] However, the quantitative relation between F contamination and Si donor have not been fully understood. In this work, to investigate these points, we measured the depth profiles of F in step-doped InAlAs layers on InP substrates. We found that F accumulates only in a n-InAlAs layers, passing through i-InAlAs layers, and the amount of F accumulation is mainly determined by Si doping concentration. In order to explain these experimental results, we propose a model and demonstrate its consistency with the experimental results.

II. Experiments

Figures 1(a), 1(b), and 1(c) show the step-doped InAlAs structures employed in this work. The epitaxial layers were grown on (100) oriented semi-insulating InP substrate by solid source molecular beam epitaxy at 450 °C. Sample A,

shown in Fig. 1(a), consists of 5 periods of 50 nm thick i-InAlAs layer and 50 nm thick n-InAlAs layer with Si doping concentration (N_{Si}) of 3×10^{18} cm^{-3}. Samples B and C, shown in Figs. 1(b) and 1(c), have sequential 100 nm thick n-InAlAs layers with N_{Si} of 6×, 3×, 1×, 3×, and 6×10^{18} cm^{-3}, and of 1×, 3×, 6×, 3×, and 1×10^{18} cm^{-3}, respectively. All layers were lattice-matched to an InP substrate. To bring about F diffusion in large quantities, the surfaces of these samples were intentionally contaminated with F atoms by exposing the surface to an HF vapor for 30 sec, and then the samples were annealed at 280 °C for 1 hour in an N_2 atmosphere. Secondary ion mass spectroscopy (SIMS) measurements were conducted using Cs^+ primary ions at 3 keV in order to investigate F concentration in epi-layers.

III. Results

Figure 2 shows SIMS profile of sample A. The solid and dashed lines indicate F and Si concentrations, respectively. The concentrations at the region from the surface to a depth of 0.05 μm should not be taken account because they reflect surface contamination. The F concentration (N_F) resembled a damped oscillation and its peaks were observed only in the n-InAlAs layers. From this profile it is found that F passes through an i-InAlAs layer and accumulates in an n-InAlAs layer. Clearly a simple diffusion model,

$$\frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2},$$
(1)

(a)

i-InAlAs		50nm	
n-InAlAs	Si:3×10^{18}cm^{-3}	50nm	}×5
InGaAs/InAlAs buffer			
InP substrate			

(b)

n-InAlAs	Si:6×10^{18}cm^{-3}	100nm
n-InAlAs	Si:3×10^{18}cm^{-3}	100nm
n-InAlAs	Si:1×10^{18}cm^{-3}	100nm
n-InAlAs	Si:3×10^{18}cm^{-3}	100nm
n-InAlAs	Si:6×10^{18}cm^{-3}	100nm
InPsubstrate		

(c)

n-InAlAs	Si:1×10^{18}cm^{-3}	100nm
n-InAlAs	Si:3×10^{18}cm^{-3}	100nm
n-InAlAs	Si:6×10^{18}cm^{-3}	100nm
n-InAlAs	Si:3×10^{18}cm^{-3}	100nm
n-InAlAs	Si:1×10^{18}cm^{-3}	100nm
InPsubstrate		

Fig. 1 Sample structures with step-doped InAlAs layers of (a) sample A , (b) sample B and (c) sample C .
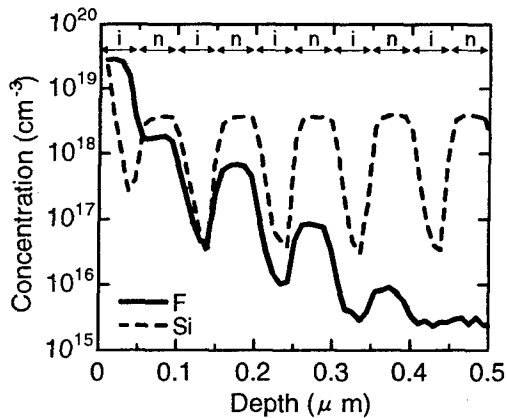
Fig. 2 Depth profile of sample A after HF treatment and anealing at 280 °C for 1 hour.

Fig. 3 Depth profile of (a) sample B and (b) sample C after HF treatment and annealing at 280 °C for 1 hour.

is insufficient to explain the discontinuous F concentration at the interface between i-InAlAs and n-InAlAs layers, because in this model the concentration gradient generally decreases with distance from the source on the surface.

To further investigate the relation between the amount of F accumulation and Si doping concentration (N_{Si}), we measured the depth profiles of samples B and C after the same treatment as sample A. SIMS profiles of samples B

and C are shown in Figs. 3(a) and 3(b). In Fig. 3(a), neglecting the concentrations in the region from the surface to a depth of 0.05 μm, N_F in the 1st layer was flat and was less than N_{Si}. At the interface between 1st and 2nd layers, N_F suddenly decreased. In the 2nd layer, N_F was flat and was less than N_{Si} again. The ratios between N_F and N_{Si} in the 1st and 2nd layers were approximately the same value of 0.67. This suggests that N_F saturates at a level which depends on N_{Si}. At the interface between 2nd and 3rd layers, it suddenly decreased again. It should be noted that although in the 3rd layer, N_F decreased gradually, it increased at the interface between 3rd and 4th layers. The same phenomenon was observed at the interface between 4th and 5th layers. As noted previously, such a phenomenon can not be explained by a simple diffusion model. In Fig. 3(b), though there was no flat N_F region, increases in N_F at the interfaces between

534

the 1st and 2nd layers and between the 2nd and 3rd layers were observed, similar to the interface between the 3rd and 4th layers in Fig. 3(a). These results indicate that F tends to accumulate in a high doping concentration layer.

IV. Discussion

From these results, we propose a new model that there is the two states of F: free and bound. In this model, we assume that only free F (F_f) can diffuse in InAlAs layer, and F_f changes into bound F (F_b) at the trapping (scattering) center which is generated by positively charged Si donor. Furthermore, we assume one F can be trapped at the center, so that the maximum concentration of F_b should be equal to N_{Si}. F_b can changes into F_f by escaping from the center, given thermal energy. We consider F transport in InAlAs as a repetition of these three processes (diffusing thermally, trapping at the center, and escaping from the center). This model can be expressed by,

$$\frac{\partial N_{Ff}}{\partial t} = -\frac{N_{Ff}\left(1-\dfrac{N_{Fb}}{N_{Si}}\right)}{\tau_1} + \frac{N_{Fb}}{\tau_2} + D\frac{\partial^2 N_{Ff}}{\partial x^2} \qquad (2)$$

and

$$\frac{\partial N_{Fb}}{\partial t} = +\frac{N_{Ff}\left(1-\dfrac{N_{Fb}}{N_{Si}}\right)}{\tau_1} - \frac{N_{Fb}}{\tau_2}, \qquad (3)$$

where N_{Ff} and N_{Fb} are concentration of F_f and F_b at time of t and at the position of x, τ_1 and τ_2 are relaxation times from F_f to F_b and from F_b to F_f. Eqs. (2) and (3) indicates transport equations for F_f, and F_b, respectively. In Eq. (2), the 1st term on the right hand side is a trapping rate of F_f. This term must contains the probability that a trapping center is unoccupied ($1-(N_{Fb}/N_{Si})$). The 2nd term is a escaping rate of F_b. The 3rd term in Eq. (2) is the pure diffusion term. In Eq. (3), the 1st and 2nd terms on the right hand side are the same as in Eq. (2) with the opposite signs. A diffusion term does not exist
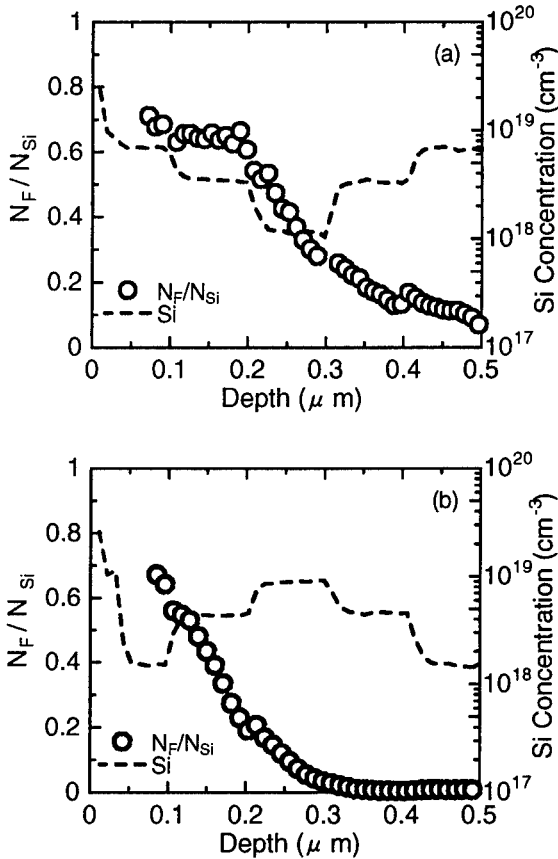
Fig. 4 Plots of N_F normalized by N_{Si} of (a) sample B and (b) sample C.
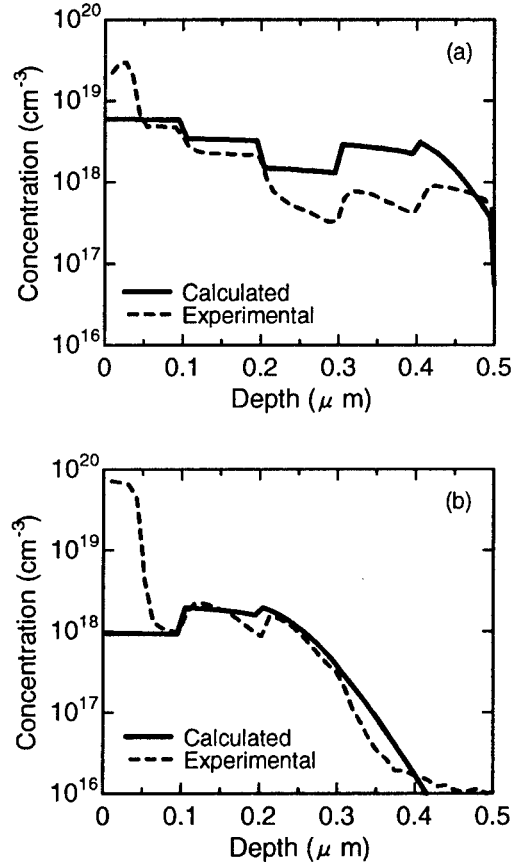
Fig. 5 Calculated F profiles for (a) sample B and (b) sample C.

535

in Eq. (3) because F_b is assumed to be bound.

Figures. 4(a) and 4(b) show the depth profile of N_F normalized by N_{Si} of samples B and C. At the interfaces, the N_F/N_{Si} profiles turned out to be almost smooth. It is found that N_F/N_{Si} remains constant at a interface between InAlAs layers with different N_{Si} while F diffuses. In our model, the small gap of N_F/N_{Si} at the interfaces means that a large amount of F exist in the state of F_b.

Figures 5(a) and 5(b) show the calculated F profiles for sample B and C according to our model. For simplicity, it was assumed that F diffuses symmetrically from the surface to both the epi-layer and atmosphere. The calculated results in Figs. 5(a) and 5(b) are obtained by $D=3.0\times10^{-13}$ cm^2/s, $\tau_1=1.0\times10^1$ s, and $\tau_2 = 5.0\times10^2$ s. In Fig. 5(a), the calculated N_F (N_F-calc) at the 1st and 2nd layers is good agreement with the experimental N_F (N_F-ex), and N_F-calc from the 3rd to the 4th layers can be described qualitatively the shape of N_F-ex which gradually decreased in the 3rd layer and drastically increased at the interface between the 3rd and the 4th layers. Also in Fig 5(b), N_F-calc describes qualitatively all over the shape of N_F-ex. Thus it is found that the model is appropriate to explain the main feature of F diffusion in InAlAs layers.

V. Summary

In summary, we have observed contaminated F profiles in the step-doped InAlAs layers of the various samples. It was found that F passed through i-InAlAs layer and accumulated in the following n-InAlAs layers, and that the amount of accumulation of F in n-InAlAs layer depends on the Si doping concentration. It must be assumed that F is trapped by the center generated by Si donor, and that concentration of a trapping center is equal to Si doping concentration. Therefore we proposed a model, in which F in InAlAs consist of free and bound F, and demonstrated that the experimental results are explained by the model.

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Zn⁺, Zn⁺/P⁺ and Zn⁺/As⁺ Implanted InP: Study of Electrical and Symmetry Properties

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InP is known to be characterized by a low activation efficiency of p-type dopants [1]. Some attempts have been previously undertaken to use the coimplantation of P^+ ions in order to improve the activation efficiency of Be and Mg in InP [2-4]. The goal of this work was to study the activation efficiency of Zn impurity coimplanted with P^+ and As^+ ions in n-InP as well as the peculiarities of crystal lattice recovering during annealing. The latter was investigated by optical second harmonic generation (SHG) method which proved to be a versatile and sensitive probe of symmetry properties of InP near-surface layers.

LEC-grown (100)-oriented n-InP single crystals (n= 2×10^{16} cm^{-3}, μ = 3550 cm^{-2} V^{-1} s^{-1}) were implanted with Zn^+, Zn^+/P^+ and Zn^+/As^+ ions at doses 5×10^{13}, 5×10^{14} and 5×10^{15} cm^{-2}. The ion energies used (150, 75 and 163 keV for Zn^+, P^+ and As^+ ions, respectively) provided an overlap of the implant-depth profiles. Free carrier concentration and mobility were determined by Hall effect measurements. For SHG experiments a Q-switched Nd/YAG laser operating at λ_ω=1064 nm was used. The reflected SHG signal $\lambda_{2\omega}$=532 nm was detected by standart boxcar-integrator techniques.

The influence of P^+ and As^+ coimplantation was found to depend upon the dose of implantation (D) and temperature of annealing (T_{ann}). Decrease of Zn impurity activation was evidenced in samples coimplanted with P^+ and As^+ ions and annealed at temperatures between 400 and 600 °C. At the same time an improvement of Zn activation was reached after dual implantation at moderate doses and sample annealing at T_{ann} > 700 °C (Table 1). These results were explained taking into account two competitive mechanisms for defect formation in P^+ and As^+ implanted InP. One of them is the formation of P_{In} and As_{In} donor-like centers stable up to 600 °C. The second mechanism implies the formation of indium vacancies which are easily filled in by Zn atoms at T_{ann} > 700 °C.

During SHG experiments the second harmonic signal has not been detected from as-implanted samples of InP indicating a full amorphization of the near-surface layers. The evolution of crystall lattice recovery with T_{ann} was evidenced by analysing the rotational dependencies of SHG intensity. Unlike Zn^+ implantation, dual implantation was established to provide a complete restoration of the crystallinity of the near-surface layers at T ≥ 600 °C (Fig. 1). The proposed explanation of this effect takes into account the stoichiometric disturbances which in the case of P^+ and As^+ coimplantation facilitates the annealing of radiation defects.

Table 1. Electrical parameters of InP layers after implantation and annealing at 750 °C

D, cm^{-2}	Ions	Sheet hole density, cm^{-3}	Mobility, $cm^2 V^{-1} s^{-1}$	Activation, %
5 x 10^{13}	Zn$^+$	2.3 x 10^{13}	71	46
	Zn$^+$/P$^+$	2.7 x 10^{13}	61	54
	Zn$^+$/As$^+$	3.1 x 10^{13}	84	62
5 x 10^{14}	Zn$^+$	2.0 x 10^{14}	55	40
	Zn$^+$/P$^+$	2.4 x 10^{14}	46	48
	Zn$^+$/As$^+$	2.5 x 10^{14}	81	50
5 x 10^{15}	Zn$^+$	2.5 x 10^{14}	50	5
	Zn$^+$/P$^+$	i-type		
	Zn$^+$/As$^+$	i-type		
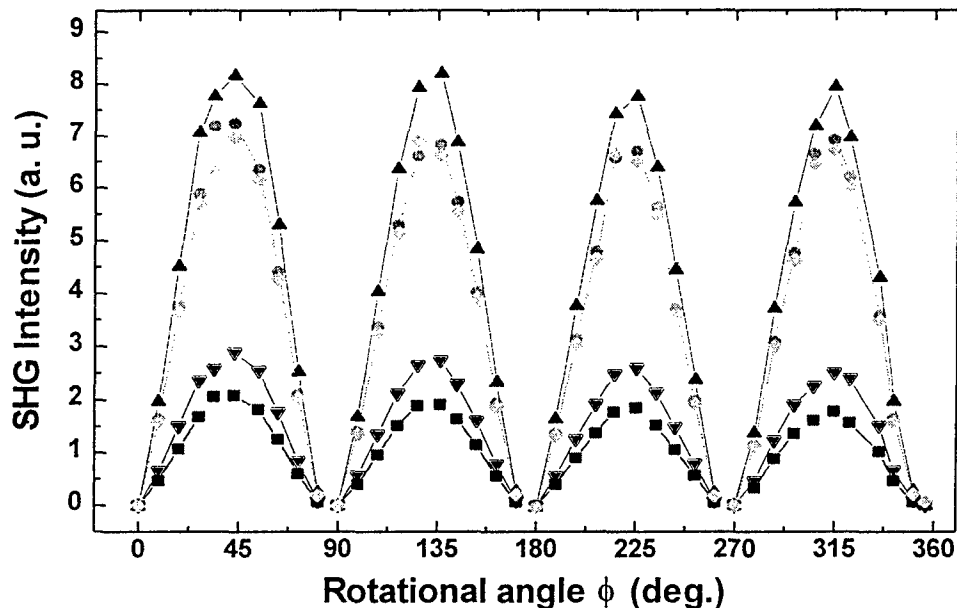
Figure 1. Rotational dependence of SHG signal from initial InP sample (●) and InP samples implanted with: (▼) Zn$^+$, D = 5 x 10^{14} cm^{-2}; (▲) Zn$^+$/As$^+$, D = 5 x 10^{14} cm^{-2}; (■) Zn$^+$, D = 5 x 10^{15} cm^{-2}; (◆) Zn$^+$/As$^+$, D = 5 x 10^{15} cm^{-2} and annealed at T_{ann} = 600 °C. The incident beam was polarized in the plane of incidence and the SHG signal with a polarization perpendicular to the plane of incidence was detected.

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May 12-15th 1997

Commercialisation of InP based epitaxy: State of the art and beyond!

by

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Over the last decade, InP technology and its related Materials have grown enormously in strategic importance as the technology has facilitated the explosive growth in optical fibre telecommunications, which in turn has spawned a huge communications revolution.   In addition, InP based materials have been exploited for many other applications such as long wavelength IR detector arrays, gas sensing applications, imaging, solar cells, high speed HEMT and HBTs, high power FETs and several other mm and microwave devices.

Fundamental to the operation of these devices is the availability of high quality and cost effective epitaxy and this presentation will review the state of the art in InP based epitaxy, and what lies ahead in terms of further technical developments.   In particular, the different technologies used for producing InP epi wafers will be reviewed together with current capabilities in terms of base materials quality, uniformity, repeatability, materials combinations available, and device performance.   Clearly as the InP industry matures, the tolerances required for the implementation of various systems will become even tighter, as will the need for manufacturing strategies capable of improving yields, reproducibility and thereby reducing costs.   These strategies will be reviewed together with analysis of the industry which will be used to identify the driving forces in the marketplace both today and in the future.

MOCVD Growth of Heavily *P*-type Doped InGaAs Using Bismethylcyclopentadienyl-Beryllium

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Introduction

Beryllium (Be) has been investigated as p-type dopant for InGaAs layers grown using bismethylcyclopentadienyl-beryllium ($(MeCp)_2Be$) by low-pressure metalorganic chemical vapor deposition. It is found that hole concentration is in proportion to the $(MeCp)_2Be$ flow rate, which results in excellent doping controllability. Moreover, the doping efficiency of $(MeCp)_2Be$ is one order of magnitude higher than that of diethylzinc (DEZn). The hole concentration of Be-doped InGaAs increases with increasing growth temperature in the temperature range from 570 to 625°C. Heavily Be-doped InGaAs layers with specular surface morphology have been attained with a hole concentration in excess of $10^{19}cm^{-3}$ by optimization of growth condition. $(MeCp)_2Be$ is promising precursor as p-type dopant source for optoelectronic devices.

I. Background

Most of optoelectronic devices require abrupt doping profiles and high quality hetrointerfaces of InP/InGaAsP. Zinc (Zn) has been the most common p-type dopant for the InP and related materials grown by metalorganic chemical vapor deposition (MOCVD) [1,2]. There has been, however, a problem on its doping controllability due to the large diffusion coefficient. From a diffusivity viewpoint, beryllium (Be) is an attractive dopant. The diffusion coefficient of Be in GaAs has been reported to be at least one order of magnitude less than that of Zn [3].

We have previously reported the Be-doping for a p-type InP layer using bismethylcyclopentadienyl-beryllium ($(MeCp)_2Be$). It has been found that there is no significant Be diffusion in undoped InGaAsP/ Be-doped InP structure [4].

Heavily Be-doping of more than $10^{19}cm^{-3}$ in InGaAs is necessary to obtain low ohmic resistance as the contact layer of the long wave length laser diodes. However, there are few reports on Be-doping in InGaAs grown by MOCVD, except one for diethylberyllium (DEBe) [5]. In the case of DEBe, it has been hard to control its doping level with good reproducibility, since the hole concentration increases in proportion to the second power of its flow rate. This doping behavior of Be is explained by the formation of dimeric DEBe molecules as an intermediate product.

In this paper, we report successful Be-doping in the InGaAs layer with good controllability using $(MeCp)_2Be$ which has little intermediate reaction. Be-doping characteristics and Be-incorporation mechanism in InGaAs grown by MOCVD is discussed as a function of growth temperature, growth rate and V/III ratio.

II. Experimental Procedure

Be-doped InGaAs layers lattice-matched to InP were grown by a low pressure MOCVD at 50 Torr. Fe-doped, semi-insulating (100) oriented InP substrates were used. The source materials were trimethylindium (TMI), triethylgallium (TEG) and arsine (AsH_3; 10%). $(MeCp)_2Be$, which was kept at 20°C, was used as Be source. The vapor pressure of $(MeCp)_2Be$ at 20°C, which is about 0.05 Torr, is about two orders of magnitude lower than that of DEBe. The melting point and boiling point of $(MeCp)_2Be$ are -29°C and 68°C, respectively. The flow rates of TMI (at 24°C) and TEG (at 19°C) were 1.18×10^{-4} mol/min and 5.65×10^{-5} mol/min, respectively. The growth temperature was changed from 570 to 625°C. The growth rate was varied between 1.8 and 3.4μm/hour, and the V/III ratio ranged from 9 to 45. For comparison Zn-doped InGaAs layers were also grown under the same growth condition, using diethylzinc (DEZn) as Zn source.

The electrical properties of Be-doped InGaAs layers were measured by the Van der Pauw technique. The

concentrations of Be atoms in the InGaAs layers were analyzed by secondary ion mass spectrometry (SIMS). The surface morphology of Be-doped InGaAs layers were observed using Nomarski interference contrast photomicrographs.

III. Results and discussion

Fig. 1 shows the hole concentration of Be-doped InGaAs grown at 590°C, as well as the concentration of Be atoms as a function of $(MeCp)_2Be/III$. The hole concentration increases in proportion to the $(MeCp)_2Be$ flow rate. This suggests that $(MeCp)_2Be$ molecules directly decompose into Be atoms without formation of dimers. As shown in this figure, a maximum carrier concentration as high as $1.3 \times 10^{19} cm^{-3}$ is achieved for $(MeCp)_2Be$. It is found that the hole concentration of the samples are almost identical to the Be atomic concentration measured by SIMS. This suggests that the electrical activity of Be is almost unity. Fig. 1 also shows the hole concentration of Zn-doped InGaAs as a function of DEZn/III. The doping efficiency of $(MeCp)_2Be$ is one order of magnitude higher than that of DEZn.

Fig. 2 shows the growth temperature dependence of the hole concentration for Be-doped InGaAs. As shown in the figure, the hole concentration increases with increasing growth temperature, since the decomposition of $(MeCp)_2Be$ on the surface is promoted at a higher temperature.

On the contrary, the carrier concentration of Zn-doped InGaAs decreases with increasing growth temperature, which is accounted by the desorption of Zn from the surface. The activation energy for $(MeCp)_2Be$ and DEZn doping are 0.7 eV and - 8.8 eV respectively.
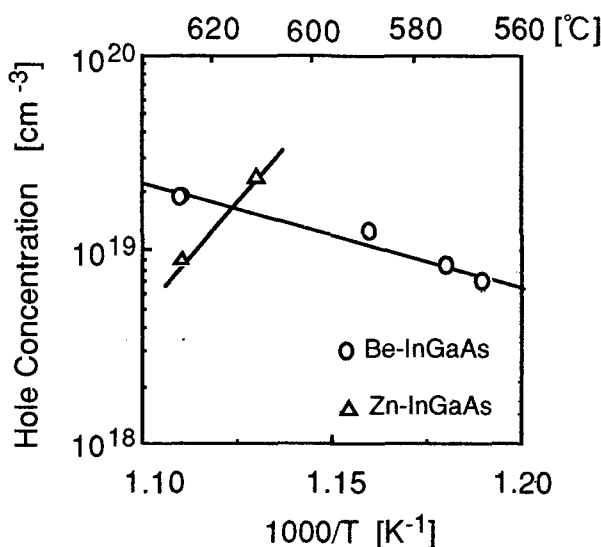
Fig. 2. The growth temperature dependence of the hole concentration for Be-doped InGaAs and that for Zn-doped InGaAs.
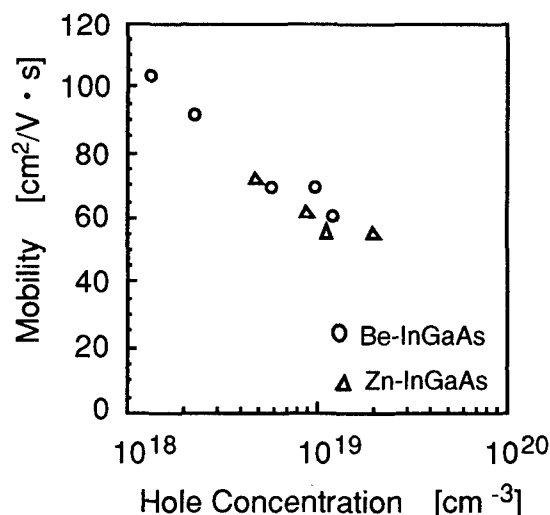
Fig. 3. Mobility as a function of the hole concentration for both Be-doped and Zn-doped InGaAs layers grown under identical conditions.

Fig. 1. Carrier concentration of Be-doped InGaAs (open circles) and Zn-doped InGaAs (triangles), as well as concentration of Be atoms (closed circles) as a function of $(MeCp)_2Be/III$ or DEZn/III.

V/III ratio		9	18	36	45
Surface Morphology	100 μ m ◄►				

rough surface | specular surface

Fig. 4. The surface morphology of Be-doped InGaAs layers grown at various V/III ratios.

Growth rate		1.8	2.8	3.4
Surface Morphology	100 μ m ◄►			

rough surface | specular surface
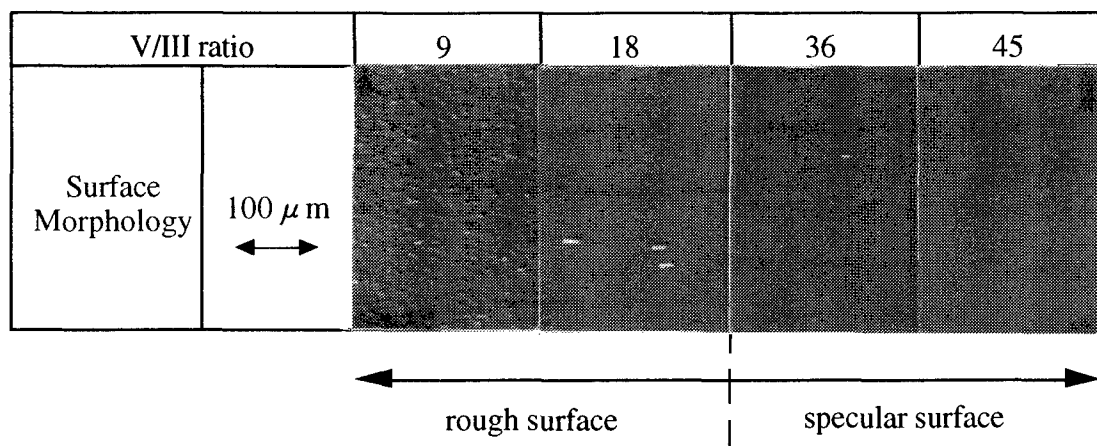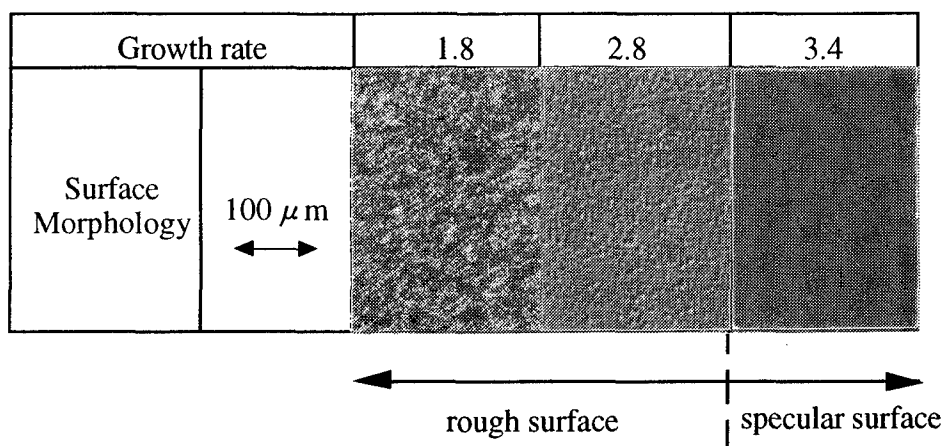
Fig. 5. The surface morphology of Be-doped InGaAs layers grown at various growth rates.

Fig. 3 shows the mobility as a function of the hole concentration for both Be-doped and Zn-doped InGaAs layers grown under identical conditions. It is clear that the mobilities of Be-doped InGaAs layers are similar to those in Zn-doped ones. This means that no deterioration of crystalline quality occurred in Be-doped InGaAs.

Next, we investigated the surface morphology of Be-doped InGaAs layers grown under various growth conditions. In the study described below, the carrier concentration was fixed to $1 \times 10^{19} cm^{-3}$.

First, the surface morphology of Be-doped InGaAs layers grown at various AsH_3 flow rates with constant $(MeCp)_2Be/III$, has been observed. Fig. 4 shows the photographs of surface morphology of Be-doped InGaAs layers grown at various V/III ratios. The samples grown with a V/III ratio of higher than 36 exhibit specular surface morphology, while those with a V/III ratio below 18 show rough morphology. Considering that the surface migration of growth species is suppressed with increasing the AsH_3 flow rate, we assume that the main factor concerning the surface morphology is the surface migration of Be atoms.

In order to further examine the effect of the surface migration of Be atoms, we investigated the change of the surface morphology with increasing growth rate. We have grown Be-doped InGaAs layers at various growth rates by changing the flow rate of group III element with constant $(MeCp)_2Be/III$ flow ratio. The reslting surface morphology is shown in Fig. 5. The samples grown with a growth rate of higher than 3.4 µm/hour show specular surface morphology, while those with a growth rate below 2.8 µm/hour show rough surface morphology.

542

Finally the growth temperature dependence of the surface morphology was also investigated. A lower - growth temperature should also suppress the surface migration. Be-doped InGaAs layers were grown at various growth temperatures with constant growth rate and V/III ratio, and the surface morphologies were compared. As expected, the surface morphology is improved with decreasing growth temperature.

Therefore, assuming that the formation of Be-clusters plays an important role, all our experimental results can be explained consistently. As shown above, the surface morphology degraded in the condition where the surface migration of Be is promoted (namely, low V/III ratio, low growth rate, and high growth temperature conditions). From this fact, it is suggested that the surface migration of Be is the causes of a degradation in surface morphology. Our finding is supported by experiments on Be-doped InP. The surface morphology of Be-doped InP by metalorganic molecular beam epitaxy (MOMBE) has been investigated by M.A.Cotta et al. [6]. They observed the surface degradation in samples grown at high growth temperature and high Be flux. Their result has indicated that the Be atoms formed clusters due to the higher surface migration.

IV. Conclusions

Be-doping characteristics in InGaAs layers grown by MOCVD using $(MeCp)_2Be$ has been investigated. It is found that hole carrier concentrations are in proportion to the $(MeCp)_2Be$ flow rates, which results in excellent doping controllability. The mobility of Be-doped InGaAs is comparable to that of Zn-doped InGaAs, which shows that no deterioration of crystalline quality occurred in Be-doped InGaAs. The doping efficiency of $(MeCp)_2Be$ is one order of magnitude higher than that of DEZn. The carrier concentration of Be-doped InGaAs increases with increasing growth temperature in the temperature range from 570 to 625°C, since the decomposition of $(MeCp)_2Be$ on the surface is promoted at a higher temperature. The surface morphology of Be-doped InGaAs layer is improved with decreasing growth temperature, with increasing growth rate, or with decreasing V/III ratio. From these facts, it is suggested that the surface migration of Be atoms is the causes of the degradation in surface morphology.

In conclusion, Heavily Be-doped InGaAs layers with excellent surface morphology have been attained with a carrier concentrations in excess of $10^{19}cm^{-3}$ by optimization of growth condition. $(MeCp)_2Be$ is promising as p-type dopant source for the InP related materials grown by MOCVD.

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All Solid Source Molecular Beam Epitaxy using Valved Cracking Cells

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Introduction

Uniform growth of $Ga_xIn_{1-x}As_yP_{1-y}$ lattice matched to InP is demonstrated with molecular beam epitaxy using all solid sources. Elemental indium and gallium, and arsenic and red phosphorus in conjunction with valved cracking cells are utilized as column III and V sources. Photoluminescence emission measurements show better than 1% reproducibility and a best case wavelength uniformity of 6.5 nm for the quaternary. Fabry-Perot cavity, multi-quantum well, 1.3 μm emission lasers having excellent light-current characteristics were fabricated. The best devices show a transparency current density as low as 55 A/cm^2 per well and slope efficiency greater than 0.5 W/A.

I. Background

Molecular beam epitaxy (MBE) was established as a technology for monolayer precision growth with very low unintentional impurity incorporation. Although it has been used for the growth of many different alloys (e.g., III-V, II-VI, IV), its principle application has been the III-V arsenides. Even though MBE is presently recognized as the technique of choice for the commercial manufacture of high-speed III-V electronic devices, it is also used for production of 70% of the world's compact disk lasers and 100% of the hall (speed) sensors.

The early focus on arsenide growth, as opposed to the phosphides, is attributed to the lack of a suitable solid phosphorus source. The first reported MBE growth of phosphides was by Cho[1] et al in 1970. Heated GaP was used for generating a P_2 growth flux. Although growth was demonstrated, rapid phosphorus depletion was observed. Accordingly, GaP was considered unsuitable as a phosphorus source. Red phosphorus was also investigated, but only a P_4 flux was produced. Furthermore, high chamber pressures subsequent to growth were observed.[2] This was due to a lack of control the red to white allotrope transformation, which would ultimately prohibit its use as a source. Consequently, a gaseous source, PH_3, derived from hydride phase epitaxy was employed for phosphide growth[3] some seven years later. This particular phosphorus supply has proven adequate for MBE growth, but its primary drawback remains; it is highly toxic and highly flammable. Subsequent to this, organometallic sources were successfully used,[4] but these are just as flammable and nearly as toxic. Inflammable and non-toxic are desirable source characteristics. To this end, all solid source MBE was pursued.

The two zone valved arsenic cell was first used by Miller[5] et al whereupon growth of GaAs was demonstrated. A similarly designed two zone valved cell was later used with phosphorus.[6] Unlike the arsenic cell though, the beam flux originating from this cell was not stable or reproducible.[7] This was a direct consequence of a red to white allotrope transformation occurring when hot P_4 vapor came into contact with the cooler regions within the cell. Briones[8] and coworkers employed a cold wall to dynamically stabilize the P_4 flux. Using a three zone valved cell, Baillargeon and Cho[9] were able to controllably generate α-white phosphorus, in-situ, from an amorphous red phosphorus source for growth. The resultant beam flux proved to be stable and reproducible so long as the white phosphorus supply existed.

II. Experiment

All growths were carried out with a Riber 2300 system using Ga, In, Si and Be beam fluxes supplied via standard Riber 35 cc ovens. The As flux was derived from either an EPI VC-IV or modified VC-III valved cell. The As cells have two separately controllable temperature zones, oven and cracker region. The cracker sections are constructed of a catalytic material, either Ta or Re, for dissociating As_4 into dimeric vapor. To generate a sufficient growth flux, the As oven generally must be heated above 350 °C. A cracker temperature in excess of 800 °C is required for dimer generation. Temperatures between 500 - 600 °C result in a tetramer beam flux.

544

The P flux originated from either a Riber KPC40 or KPC250 valved cell. The P cell differs substantially from the As in both design and operation. The P cell consists of three separately controllable temperature zones: red phosphorus oven, white phosphorus condenser/reservoir and cracking region. The P_2 flux is generated by dissociating P_4 vapor within the cracking zone. The white phosphorus supply is generated, in-situ, by heating the red phosphorus oven from 360 - 390 °C, and condensing its vapor at a temperature below 100 °C, with the output valve closed.[10] The primary differences between KPC40 and KPC250 are oven volume and output valve conductance. The former has a 35 cc volume and a maximum output valve conductance of 20 *l/s*. The later has a 250 cc volume and 0.5 *l/s* valve conductance. Consequently, the KPC40 can be operated with the reservoir at room temperature during growth while the KPC250 oven and reservoir must be heated in order to generate a sufficient growth flux. A red phosphorus consumption rate of 0.09 gms/hr, for an average beam equivalent pressure (BEP) of 1.5×10^{-6} Torr, was previously determined using a two zone valved cell.[11] More recently, we measure this usage rate to be 0.5 gm/hr for an average BEP of 1×10^{-5} Torr with the three zone KPC series cell. This is consistent with that measured elsewhere.[12]

Starting sources in this work were of the highest purity obtainable. The In and Ga were 7N purity from Nikko Kyodo and 8N from Rhone-Poulenc, respectively. The red phosphorus source was 7N purity from Rasa Industries, although subsequent analysis revealed Si, S, C and Zn present in measurable quantities. The As was 7N5 purity from Furukawa. Substrates used for laser diode growth were epi-ready, S-doped, (100) on-axis oriented InP from American Xtal Technology. No special cleaning procedures were used prior to loading them into the growth system. The viability of all solid source MBE can be demonstrated over a broad range of applications. The primary focus of this work though, is the 1.3 μm fiber laser. More specifically, epitaxial development of uncooled laser structures for fiber-in-the-loop applications.

III. Results and Discussion

The temperature characteristics of the uncooled laser are very important. Optimum temperature performance is expected if the waveguide and barrier layer compositions are chosen such that their photoluminescence (PL) emission wavelengths are substantially shorter than 1.15 μm.[13] PL emission uniformity versus wafer position for the waveguide quaternary grown with As and P valved cells is shown in Fig. 1. The growth temperature was 500 °C. Composition variation was obtained using both PL and X-ray diffraction measurement. The total wavelength variation measured is only 6.5 nm. The Ga mole fraction varies by 1% from center to wafer edge, while the As varies by 2%. However for the specific alloy composition chosen (1.12 μm), there is an equal

change in As mole fraction with change in Ga mole fraction.[14] This dependent behavior means that the maximum As (or P) variation attributable to the valved cells is 1%. The result suggest highly uniform As_2 and P_2 beam fluxes are derived from both cells. Furthermore, any uniformity enhancement with the column III fluxes will translate into a corresponding improvement in the column V uniformity. The run-to-run wavelength reproducibility for the waveguide layer is presently 10 nm, which is less than 1%.
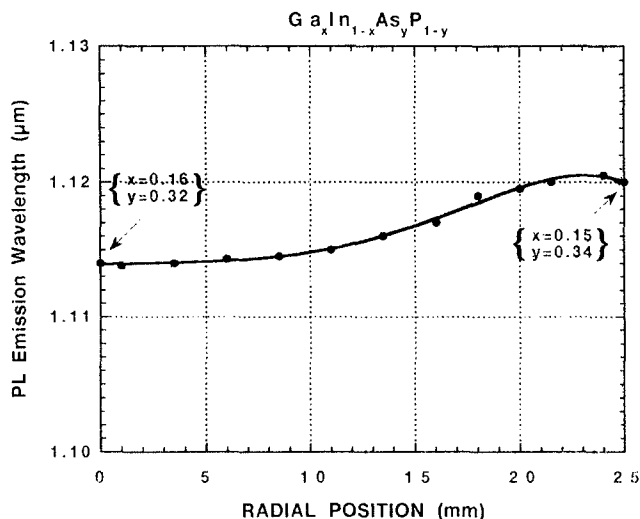
Fig. 1. PL emission uniformity, as a function of radial position across a 2 inch diameter wafer, for the quaternary used for waveguide and barrier layers. Mole fractions were determined by X-ray diffraction and PL emission.

QW emission uniformity was also studied via PL. X-ray diffraction was only used for calibrating the composition with thicker epitaxial layers. The test structures were comprised of 9- 80Å wells, 8- 100 Å barriers and corresponding waveguide layers. The composition of the waveguide and barriers layers was $Ga_{0.14}In_{0.86}As_{0.32}P_{0.68}$. The intended composition of the QW region was $Ga_{0.26}In_{0.74}As_{0.62}P_{0.38}$. This corresponds to a 0.1% compressive strain when grown on InP. A plot of PL emission uniformity for the MQW structure grown on a 2 inch diameter wafer is shown in Fig. 2. The total wavelength variation is 14.5 nm. Unlike that of a bulk layer, QW emission uniformity is a function of growth thickness as well as composition. The run-to-run wavelength reproducibility for a 9- well structure is less than 1%.

The uncooled MQW laser structure under development also has 9- 80 Å QWs, 8- 100 Å barriers and 550 Å per side waveguide layers. The PL emission wavelengths of the QW and waveguide/barrier layers are 1.32 μm and 1.12 μm, respectfully. Their respective target compositions are as described above and again in Figs. 1 and 2. The MQW

active and waveguide regions are undoped. The n-type InP cladding layer is 1 μm thick and doped 1 x 10^{18}cm^{-3} with Si. The p-type cladding layer is 1.6 μm thick. The p-doping level is graded, from 0.5 - 1 x 10^{18}cm^{-3} with Be, moving away from the waveguide/cladding layer interface toward the surface. The thickness of the graded region is 0.5 μm. Grading was done to limit free carrier absorption and not to limit dopant diffusion into the waveguide/MQW region. A 500 Å thick, p-type Ga$_{0.47}$In$_{0.53}$As contact layer doped 1 x 10^{19}cm^{-3} with Be is used.
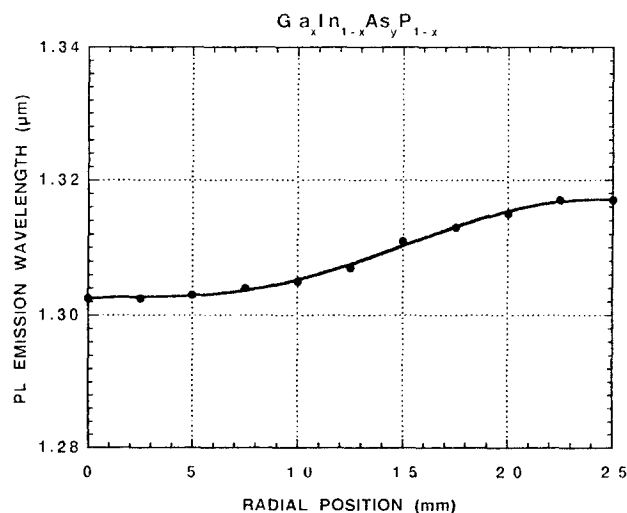
Fig. 2. PL emission uniformity of the MQW region, as a function of radial position across a 2 inch diameter wafer. The QW has a 0.1% lattice strain at 1.32 μm. The QW emission wavelength uniformity is 14.5 nm.

A growth temperature of 470 °C was chosen for the InP cladding layers and 500 °C for the MQW/waveguide region. The P beam flux is held constant at 1x 10^{-5} Torr during waveguide and cladding layer growth. This flux is adjusted slightly downward to 9.3 x 10^{-6} Torr during growth of the QWs. Accordingly, the As flux is fixed at 1.35 x 10^{-6} Torr for waveguide and barriers, and is 5.9 x 10^{-6} Torr for QW growth. All growth interruptions were limited to 10s.

A transmission electron microscope (TEM) micrograph of a working laser structure, with an active region that was grown at 485 °C, is shown in Fig. 3. The primary difference between 480 °C and 500 °C growth temperatures is the amount of P incorporated into the quaternary. As temperature increases, so does the P mole fraction. Between these two temperatures, and for the given column III compositions, P differs by about 5 at.% for waveguide and 10 at.% for the QW. The incorporation dependence of the alloy grown by solid source MBE has been published.[15]

The incorporation differences are easily accommodated by appropriate adjustment of the respective beam fluxes.
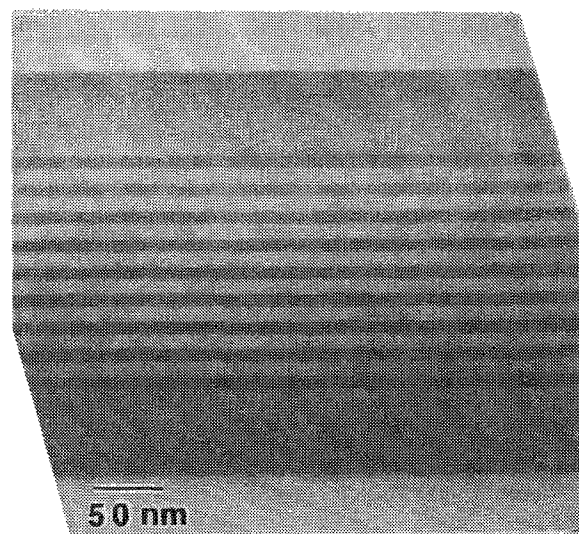
Fig. 3. TEM micrograph of a 1.3 μm laser structure where waveguide and MQW active region were grown at 485 °C. The structure consists of 9- wells, 8- barriers and waveguide region. The wells, barriers and waveguide layers are 80 Å, 100 Å and 550 Å, respectively. The QW and waveguide / barrier compositions are Ga$_{0.26}$In$_{0.74}$As$_{0.62}$P$_{0.38}$ and Ga$_{0.14}$In$_{0.86}$As$_{0.32}$P$_{0.68}$, respectfully.

Devices were fabricated from material grown structurally identical to that described. The n-type contact was alloyed while the p-type contact was a Schottky. Diodes were characterized as-cleaved, no facet coating was applied. Fig. 4 shows the dependence of threshold current density upon cavity length for MQW diodes with a different number of wells. The threshold current density increases as the number of wells decreases because the total active volume decreases. The optimum number of wells for the uncooled laser is between 8 - 9, if temperature performance is fully considered.[16] This is consistent with what we observe. All three sets of devices show nearly the same transparency current density of 55 A/cm^2 per well. This value is consistent with that measured elsewhere[12,16,17] and is presently considered state-of-art.

The slope efficiency of the 9- well devices ranged from 0.5 - 0.55 W/A for a typical 300 μm length cavity. The corresponding differential quantum efficiencies were calculated and plotted in Fig. 5 as the inverse versus cavity length. The internal quantum efficiency and internal losses extracted from this figure are η_i = 0.74 and α_i = 12.1 cm^{-1}. The internal losses are somewhat higher than expected, and this is presently under investigation.

546
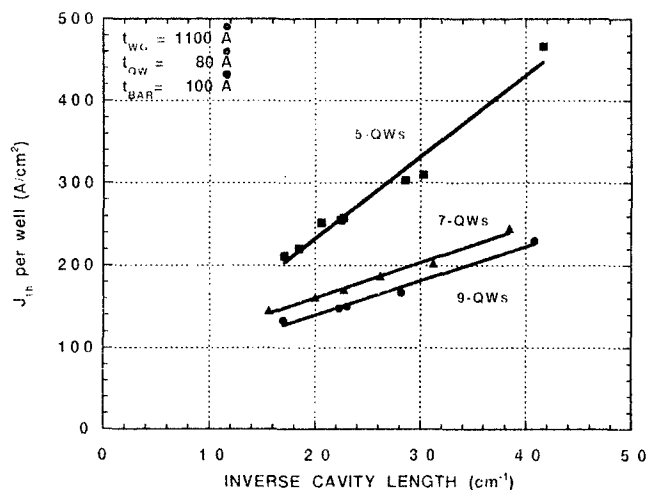
Fig. 4. Threshold current density (per well) versus inverse cavity length for the 1.3 μm uncooled laser structure with 5, 7 and 9 wells. Individual points represent the average of three diodes and the curves are a least squares fit to the data. The transparency current density is similar for all three, 55 A/cm^2 per well. The waveguide and MQW active regions were grown at 500 °C.
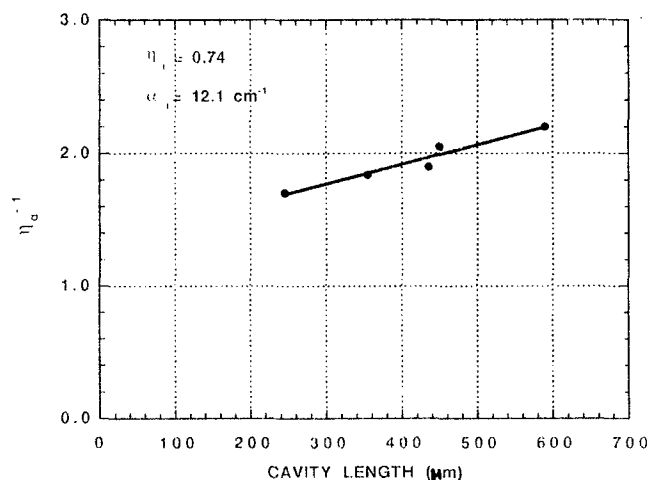
Fig. 5. The inverse differential quantum efficiency as a function of cavity length for the 9-well device structure.

IV. Conclusion

Valve cracking cells have been employed which enable use of solid phosphorus and arsenic as starting sources for MBE growth of $Ga_xIn_{1-x}As_yP_{1-y}$. An understanding and control of the red to white phosphorus transformation has been achieved. The As and P growth beam fluxes generated are stable, controllable and uniform. Growth of high quality $Ga_xIn_{1-x}As_yP_{1-y}$ materials and devices structures were demonstrated with these cells. PL measurements show that a wavelength uniformity of 6.5 nm can be achieved across a 2 inch diameter wafer. MQW laser structures fabricated show good threshold current density and efficiency characteristics with somewhat higher than expected internal losses. Devices are equivalent to those produced by other growth techniques.

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Double Heterojunction Bipolar Transistors with InP Epitaxial Layers Grown by Solid-Source MBE

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Introduction

Epitaxial layers containing phosphorus (P) find numerous applications in electronic and photonic devices such as GaInP/GaAs HBTs, InAlAs/InGaAs/InP double HBTs, GaP LEDs and InP/InGaAsP MQW lasers operating at 1.3-1.55μm. These structures have been realized traditionally either by MOCVD, GSMBE or CBE relying on highly toxic hydrides as the gas sources for phosphorus and arsenic. Solid-source MBE provides the simplest and most elegant solution for growing complex epitaxial structures; however, the unique physical properties of solid phosphorus make it difficult to grow P-containing layers. By using a recently developed phosphorus valved cracker, excellent InP heterostructures have been achieved. We have explored the use of InP active layers in InP-based HBT grown entirely by solid-source MBE and compared them to InAlAs/InGaAs HBTs.

I. Background

The excellent thermal, electronic, and chemical properties of epitaxial InP make it ideally suited for integration into HBTs lattice-matched to InP substrates. The thermal conductivity of InP is 50% higher than GaAs and >10X higher than InGaAs or InAlAs. Using InP active layers minimizes the operating junction temperature, potentially extending the device lifetime. InP offers high electron saturated velocities and high breakdown fields which together translate into better breakdown-f_t products than other bipolar technologies. From a processing point of view, InP and InGaAs exhibit excellent etch selectivity, enabling manufacturable and tailorable collector-base and emitter-base mesa profiles. For InP-based devices that do not utilize InP epitaxial layers, the availability of a P-beam enables in-situ surface preparation by maintaining an P-overpressure during cleaning rather than using an InAs-forming As$_2$ overpressure.

Phosphorus sources for solid source MBE can be obtained from the sublimation of elemental red phosphorus or from crystalline InP or GaP. The advantage of red phosphorus is that group III elements or other residual impurities originating from the sources are not present in the beam.

Red phosphorus has a very high vapor pressure (10^{-3} torr @ 150°C) and sublimates into tetramer P$_4$ molecules. P$_4$ has a low sticking coefficient to the substrate and tends to condense on the cryo panels as the white allotrope of phosporus. White phosphorus has an even higher vapor pressure (1 torr @ 70°C) than the red allotrope and is highly combustible and poisonous in atmosphere. This presents serious safety issues as the MBE chamber is brought to atmosphere and the cryo panels warm up.

To circumvent the P$_4$ condensation in the chamber, it is possible to crack the P$_4$ into P$_2$ dimers before injection into the MBE chamber. P$_2$ has near unity sticking coefficient and condenses as the friendlier red phosphorus. However, any residual white phosphorus anywhere in the path has been shown to cause severe fluctuations in the beam equivalent pressure making it impossible to reliably control the V/III ratios [1].

548

The operating principle behind the newly developed valved cracker is to convert the red phosphorus entirely into white phosphorus first and then use the white phosphorus as the P_4 source. Since the white allotrope has the highest vapor pressure, it controls the beam equivalent pressure. P_4 is then cracked to generate the uniform P_2 beam for InP growth. Excellent abrupt InP-collector HBT performance has already been reported with the valved cracker [2].

II. Epitaxial Structures & Fabrication

A series of InP-based HBT structures were grown by solid source MBE equipped with the valved phosphorus cracker to study the material and interface qualities of epitaxial InP. The InP was grown with a V/III beam equivalent ratio of 20 over a temperature range of 440-480°C. Silicon and beryllium were used as n- and p-type dopants. Fig. 1 summarizes the 5 structures that were compared. The emitter-base junction was implemented in three different ways: 1. abrupt InAlAs/InGaAs, 2. Graded In(GaAl)As, 3. abrupt InP/InGaAs. The base-collector junction was implemented either as an InGaAs homojunction or as a composite InGaAs/InP collector with pulse doping to reduce carrier blocking. In all cases, the emitter cap and subcollector layers consisted of heavily doped InGaAs to ensure low contact and access resistances. The 800Å base was Be-doped at 3×10^{19} cm^{-3} translating into a 460Ω/sq sheet resistance.

Cap	InGaAs	InGaAs	InGaAs	InGaAs	InGaAs
Emitter	InAlAs	InAlAs	InP	InAlAs	InP
Grade	InGaAlAs	-	-	-	-
Base	InGaAs	InGaAs	InGaAs	InGaAs	InGaAs
Grade	-	-	-	comp.	comp.
Coll.	InGaAs	InGaAs	InGaAs	InP	InP
S-Coll.	InGaAs	InGaAs	InGaAs	InGaAs	InGaAs

Fig. 1. Epitaxial structures for a set of InP-based HBTs containing InP, InAlAs and InGaAs.

Large area devices were fabricated using selective wet chemical etching to define the emitter and base mesas. The InAlAs and InGaAs layers were etched in a $H_3PO_4:H_2O_2:H_2O$ solution while the InP layers were removed in a $HCl:H_2O$ solution. During the mesa etching steps, no interface problems at either the InP/InGaAs or the inverted interface InGaAs/InP were observed. Phosphorus-arsenic exchange at these metallurgical junctions has been shown to create unintentional InGaAsP etch-stop layers that inhibit further etching and cause surface roughness. TiPtAu ohmic metal was used to access the emitter, base and collector layers. Smaller area transistors were contacted with interconnect metal supported on a PECVD SiO_2 dielectric.

III. Emitter-base Junction Characteristics

The different emitter-base structures yield different injection characteristics as shown in Fig. 2. The graded junction HBT exhibits the lowest $V_{be(on)}$ since there is no conduction band discontinuity, ΔE_c. The abrupt InP/InGaAs and InAlAs/InGaAs structures show larger $V_{be(on)}$ corresponding to the respectively greater ΔE_c. Figs. 3 and 4 show the near ideal Gummel characteristics for the abrupt emitter-base structures. The larger ΔE_c consistently yield higher ideality factors and ß, possibly as a result of heterostructure transport across the abrupt spike and subsequent hot electron injection, respectively. The abrupt heterojunction achieves ß ranging from 45-55 while the graded one yields ß=40. These values of ß represent bulk recombination limits that can only be obtained at this base sheet resistance if the quality of the heterointerfaces is excellent.
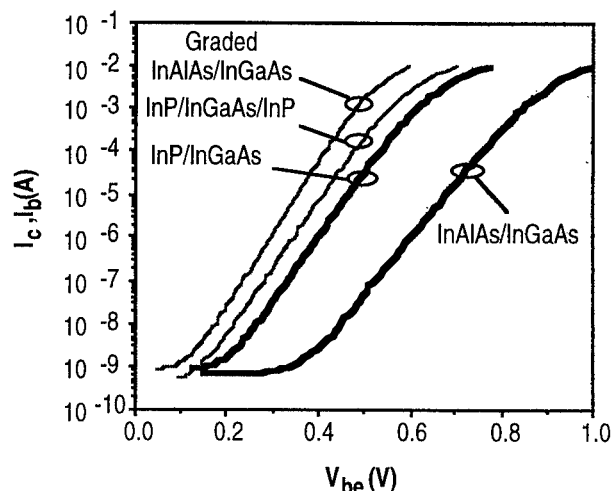
Fig. 2. A comparison of the injection characteristics for different InP-based emitter-base heterojunctions.
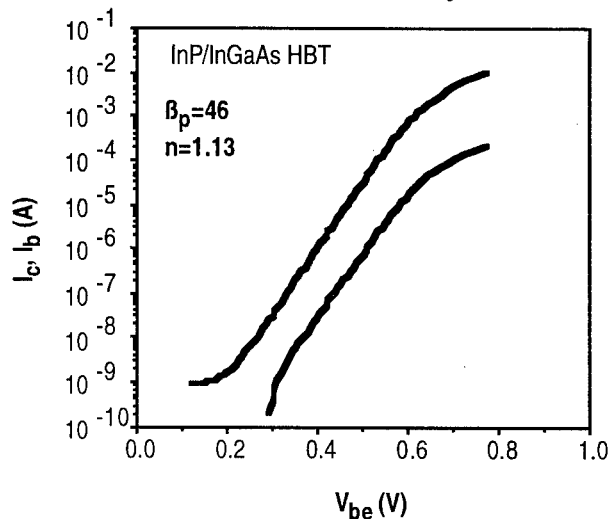
Fig. 3. Gummel characteristics for an abrupt InP-InGaAs HBT.
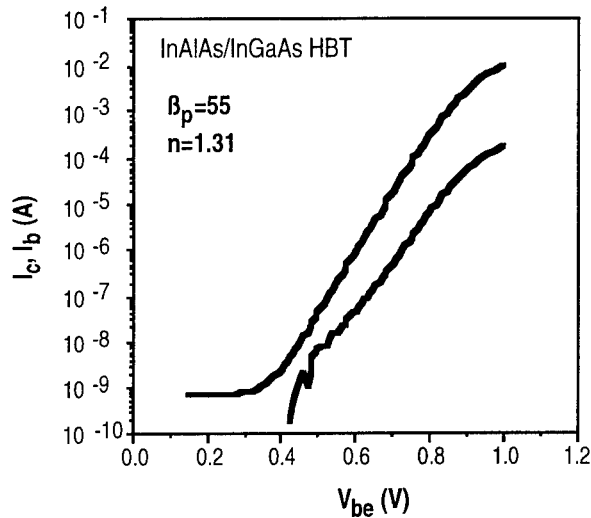
Fig. 4. Gummel characteristics for an abrupt InAlAs-InGaAs HBT.

III. Base-collector Junction Characteristics

The common emitter characteristics for InGaAs collector and composite collector HBTs are shown in Figs. 5 and 6, where both structures have InAlAs emitters. The composite collector HBT exhibits an Early voltage, V_A, >450V while it is <4V for the InGaAs collector. Similar behavior was observed when InP emitters were replaced by InAlAs.

Although composite collector structures increase the operating voltage range, they also limit the peak current density that can be achieved at low voltages. This current blocking phenomenon is a variant of the Kirk effect in conventional Si BJTs since there is a direct trade-off between breakdown and offset voltages. Fig. 7 compares the common-base performance of InGaAs versus composite collector HBTs. At Vcb=0, both structures handle $75kA/cm^2$ (30mA) without current blocking.
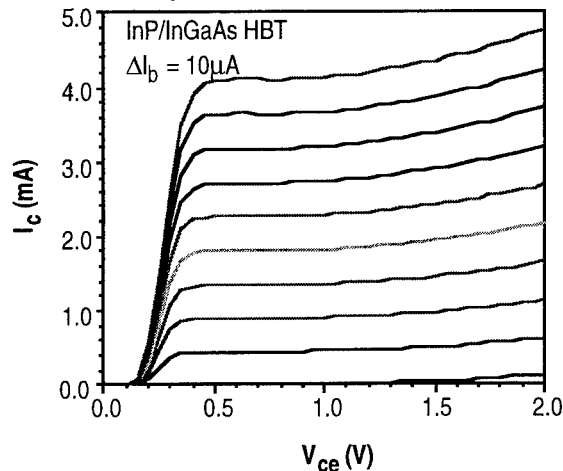
Fig. 5. Common emitter characteristics for an abrupt InP- InGaAs HBT with an InGaAs collector.
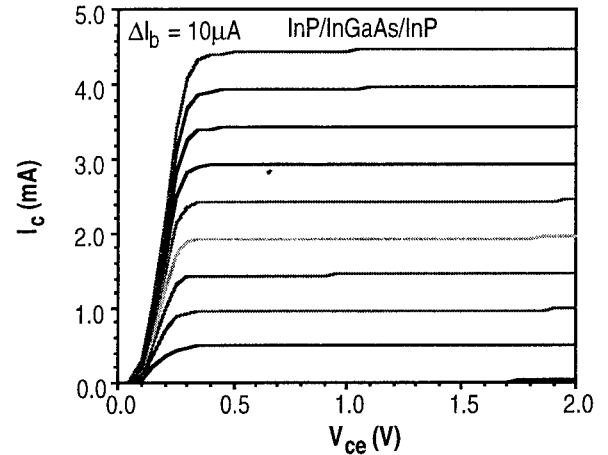
Fig. 6. Common emitter characteristics for an abrupt InP-InGaAs HBT with an InP composite collector.
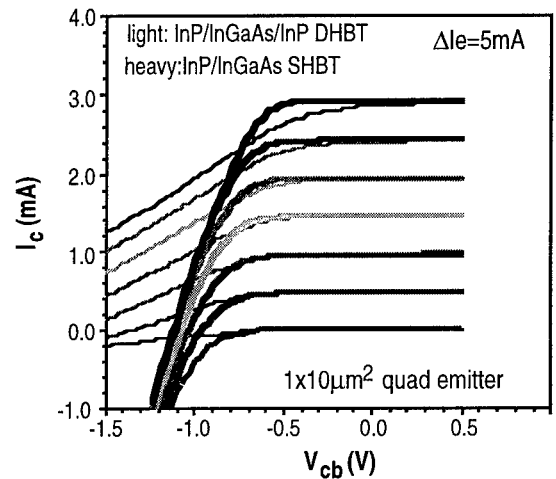
Fig. 7. Common base characteristics comparing the composite InP collector with the InGaAs collector.

IV. Conclusions

Solid source MBE is capable of producing high qualtiy InP/InGaAs heterojunctions using a valved phosphorus cracker. InP-based HBTs featuring InP emitters and collectors were compared to those containing InAlAs emitters and InGaAs collectors. The InP emitter HBTs exhibited excellent ß and no As-P intermixing. The InP collector HBTs showed 2 orders of magnitude improvement in the output characteristics. The high V_A enables high precision analog functions as well as higher voltage operation.

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BROADENED WAVEGUIDE, LOW LOSS 1.5 μm InGaAsP/InP AND 2 μm InGaAsSb/AlGaAsSb LASER DIODES.

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Introduction.

We demonstrate that free carrier absorption in cladding layers of long wavelength (λ=1.5 μm and λ=2 μm), separate confinement quantum well laser diodes limits the differential efficiency and output power for such lasers if their waveguide thickness is designed from the considerations of the maximum optical confinement factor for quantum wells. Broadening of the waveguide up to 1 μm considerably increases laser efficiency and does not increase threshold for the lasers with low and moderate output losses. Broadened waveguide design provides the record output powers at continuous and quasi-continuous operation regimes.

In 1982 W. T. Tsang [1] demonstrated, for the first time, separate-confinement-heterostructure (SCH) design for AlGaAs/GaAs quantum well (QW) lasers. During the last decade, the SCH QW design has received wide acceptance for various types of semiconductor lasers including long-wavelength 1.5 μm [2-4] and 2 μm lasers [5-7]. An analysis of the advantages of SCH structures has been given by W. Tsang in his paper [1]. According to Tsang, the incorporation of undoped waveguide layers between the QW and cladding layers increases optical confinement factor for quantum wells (Γ_{QW}) and decreases internal losses (α_{int}) caused by free carrier absorption. The waveguide thickness, W, providing the maximum Γ_{QW}, should be about 300-450 nm. At this optimum value, $W = W_0$, the internal losses due to free carrier absorption in the doped cladding layers are small relative to output losses. Tsang made this conclusion studying AlGaAs/GaAs graded refractive index (GRIN SCH) lasers with cavity lengths shorter than 1.2 mm and a cladding layer carrier concentration of 10^{17} cm^{-3}. His conclusion, although correct for the case considered in [1], has been generalized to the design of all types of SCH QW lasers. Only recently has a more complete consideration of the influence of W on the parameters of GRIN SCH and SCH lasers been done [8]. It has been demonstrated that when $W \approx W_0$ and doping levels in the cladding layers are 10^{18} cm^{-3}, the losses due to free carrier absorption are already significant for GaAs-based GRINCH- and especially for step - SCH lasers with output losses less than 10 cm^{-1}. Since loss due to free carrier absorption increases with wavelength, it becomes the dominant factor for InP- and GaSb-based, long wavelength SCH QW lasers [9, 10, 11]. In this paper, we will give a more detailed discussion of the results published in [9, 10, 11].

The transverse near-field distribution in a SCH QW laser structure can be characterized by optical confinement factors for quantum well(s) and cladding layers (Γ_{QW} and Γ_{CL}, respectively). Table 1 demonstrates the influence of W on Γ_{QW} and Γ_{CL} for three types of SCH QW laser structures. The upper row shows Γ_{QW} and Γ_{CL} for a two-step waveguide, 1.5 μm InGaAsP/InP SCH QW structure described in [9]. The laser structure consists of three compressively strained QWs, surrounded by a stepped-composition, InGaAsP waveguide. The thickness of the inner, 1.0 eV band gap waveguide layers are 30 nm for all laser structures while the thickness of the outer, 1.13 eV band-gap waveguide layers are varied from 300 to 1200 nm. Donor concentration in the n-InP cladding layer was 5×10^{17} cm^{-3}, and average acceptor concentration in the graded-doped p-cladding layer was 7.5×10^{17} cm^{-3} [9].

The second row of the Table 1 refers to a 5-QW AlGaAsSb/InGaAsSb SCH QW laser emitting at 2 μm. The structure consists of five InGaAsSb QWs, surrounded by $Al_{0.25}Ga_{0.75}As_{0.02}Sb_{0.98}$ SCH layers and $Al_{0.9}Ga_{0.1}As_{0.07}Sb_{0.93}$ cladding layers. The total waveguide thickness is varied from 120 to 880 nm [10]. The n-cladding layer was doped by Te to $n = 2 \times 10^{17}$ cm^{-3}. The first 0.2 μm of the p-cladding layer adjacent to the waveguide is doped with Be to 5×10^{17} cm^{-3}. The reminder of the layer is doped with Be at 5×10^{18} cm^{-3}.

Table 1. Optical confinement factors and measured internal losses.

Laser structure	Waveguide thickness, nm	Γ_{QW}	Γ_{cl}	α_{int}, cm^{-1}	Waveguide thickness, nm	Γ_{QW}	Γ_{cl}	α_{in}, cm^{-1}
1.5 µm InGaAsP/InP SCH 3 QW	410	0.036	0.36	5.9	1300	0.026	0.04	1.3
2 µm InGaAsSb/AlGaAsSb SCH 5 QW	320	0.105	0.38	17	880	0.075	0.07	2
2 µm InGaAsSb/AlGaAsSb SCH SQW	320	0.021	0.41		880	0.015	0.075	

The third row of Table 1 describes Γ_{QW} and Γ_{CL} for a single quantum well AlGaAsSb/InGaAsSb SCH structure that differs from the similar MQW structure only by the number of QWs [11].

The first result that follows from the data of Table 1 is that the decrease in Γ_{QW} is not proportional to the increase of the ratio W/W$_0$. When W/W$_0$ increases by 3 times, Γ_{QW} decreases less than by 30% for all laser structures of Table 1. The relatively weak dependence of Γ_{QW} on W/W$_0$ is in contrast to the superlinear decrease of Γ_{CL} with increasing W/W$_0$. The results listed in Table 1 indicate that the transverse near-field (TNF) distribution in SCH QW laser structures varies significantly with waveguide broadening.

Fig. 1 clarifies the character of TNF variation with waveguide thickness. The TNF distribution for the structure with waveguide thickness W = W$_0$ (Fig. 1a) indicates a mode that is weakly coupled to the waveguide and includes extensive wings spreading into the cladding layers. As the waveguide is broadened to 1 µm, the mode becomes strongly coupled with the waveguide with a dramatic decrease in the relative intensity of the wings. (Fig 1b).

Now consider the influence of the TNF pattern modifications on internal loss. From the data of Table 1 the losses due to free carrier absorption in 10^{18} cm^{-3} doped cladding layers is not negligible, since at W = W$_0$ more than 35% of the lasing mode is spreading into the cladding layers. For accurate estimation of the cladding losses, we used data on free carrier absorption in InP [12, 13]. In accordance with [12], the absorption coefficient in n-InP with donor concentration of 5×10^{17} cm^{-3} is less than 0.5 cm^{-1} at 1.5 µm wavelength. The corresponding losses will not be taken into account in the subsequent treatment. From the free carrier absorption spectra for p-InP [13], one finds that for an acceptor concentration of 7.5×10^{17} cm^{-3}, the absorption coefficient is 20 cm^{-1} at 1.5 µm.

In the case of GaSb–based lasers, the composition of the cladding layers is close to AlSb, and we use the free carrier absorption data for this material to estimate the losses. The free carrier absorption in n-AlSb at a wavelength of 2 µm is considerably stronger than in n-InP or n-GaAs [14], and absorption coefficient is already 10 cm^{-1} at n = 2×10^{17} cm^{-3}.
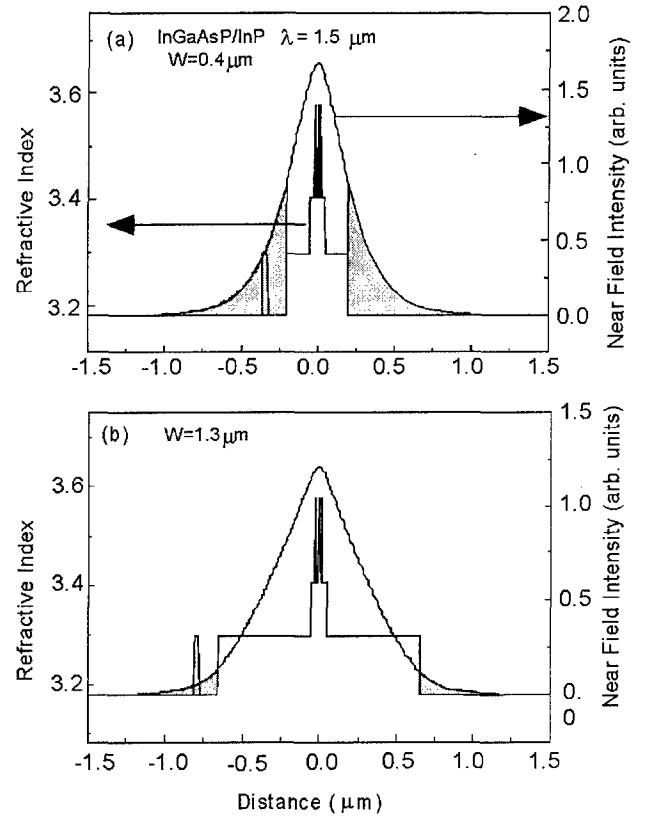
Fig. 1. *Refractive index and transverse near-field distributions for two-step waveguide 1.5 µm InGaAsP/InP SCH QW lasers with W = 0.4 µm (a) and W = 0.8 µm (b). The values of Γ_{CL} are proportional to the areas of the shadowed regions.*

The absorption coefficient in p-AlSb is also higher than in p-GaAs or p-InP, and equals 150 cm^{-1} at 2 µm wavelength for p = 5×10^{18} cm^{-3} [15].

These data on free carrier absorption, in combination with data of Table 1, allow one to compute the upper limit of the laser differential efficiencies ($\eta_{d\text{-max}}$), assuming that free carrier absorption in the cladding layers is the sole mechanism of internal losses. In this case, $\eta_{d\text{-max}}$ can be calculated as:

$$\eta_{d-\text{max}} = \eta_i \frac{\alpha_{out}}{\alpha_{out} + \sum \Gamma_i \cdot \alpha_i},$$

where $\sum \Gamma_i \cdot \alpha_i$ is the sum of losses due to free carrier absorption in all fractions of the cladding layers with different doping, $\alpha_{out} \approx \frac{1}{L} \ln\left(\frac{1}{R}\right)$ is the total output loss, and η_i is the coefficient describing both non-radiative recombination and leakage currents in the laser structures. Calculated values of $\eta_{d-\text{max}}$ for 1.5 µm and 2 µm lasers with different waveguide thicknesses are given in Fig. 2. The value of η_i was taken to be 0.8, the experimental value found in [9, 10] for both types of lasers considered. The calculations were done for $\alpha_{out} = 5$ cm^{-1} and $\alpha_{out} = 10$ cm^{-1}. These values of output losses are typical for coated and uncoated laser diodes with cavity lengths of 1-3 mm. The results of the calculations are compared in Fig. 2 with the experimental values of η_d for diodes with the same values of α_{out} [9, 10]. Fig. 2 demonstrates that free carrier absorption in the cladding layers is the main source of internal losses when $W \approx W_0$. Differential efficiencies increase considerably when the waveguide thickness exceeds W_0 by a factor of 3. The data of Table 1 describe record low internal losses of 2 cm^{-1} and 1.3 cm^{-1} for the broadened waveguide (BW) 2 µm AlGaAsSb/InGaAsSb and 1.5 µm InGaAsP/InP SCH QW lasers, respectively [9, 10]. The measured values of differential efficiencies for these lasers (data points in Fig. 2) are very high for long-cavity lasers operating at these wavelengths. Such lasers demonstrate record CW output powers at wavelengths of 1.5 µm [9] and 2 µm [10, 11].

As expected, the experimental values of η_d are lower than those calculated, since beside the cladding layer losses, η_d could be reduced due to free carrier absorption in the QWs and laser mode scattering at the hetero-interfaces. The influence of these additional loss mechanisms should become stronger as the waveguide thickness increases and the cladding losses are reduced. It is also evident that the scattering and QW losses should be higher in structures with a larger number of QWs. The data for 5 QW InGaAsSb/AlGaAsSb laser diodes (Fig. 2b) demonstrate the increase in the difference between $\eta_{d-\text{max}}$ and η_d as the waveguide thickness increases.

Attempting to reduce the residual "non - cladding" losses, AlGaAsSb/InGaAsSb broadened waveguide lasers with a single QW [11] have been investigated (see Table 1). A value of η_d as high as 53% has been obtained for 2 mm-long, facet coated lasers with $\alpha_{out} = 9$ cm^{-1} (solid triangle in Fig. 2b). This value of η_d is higher than that obtained for 2 µm InP-based lasers with the same output loss [7] or extrapolated from the earlier published [5, 6] data on η_d for 2 µm AlGaAsSb/InGaAsSb lasers. The differential efficiencies obtained for the 1.5 µm InGaAsP/InP broadened waveguide lasers (data points in Fig. 2a) are also higher than the best of the earlier published results for 1.5 µm laser with low output losses [1, 2].
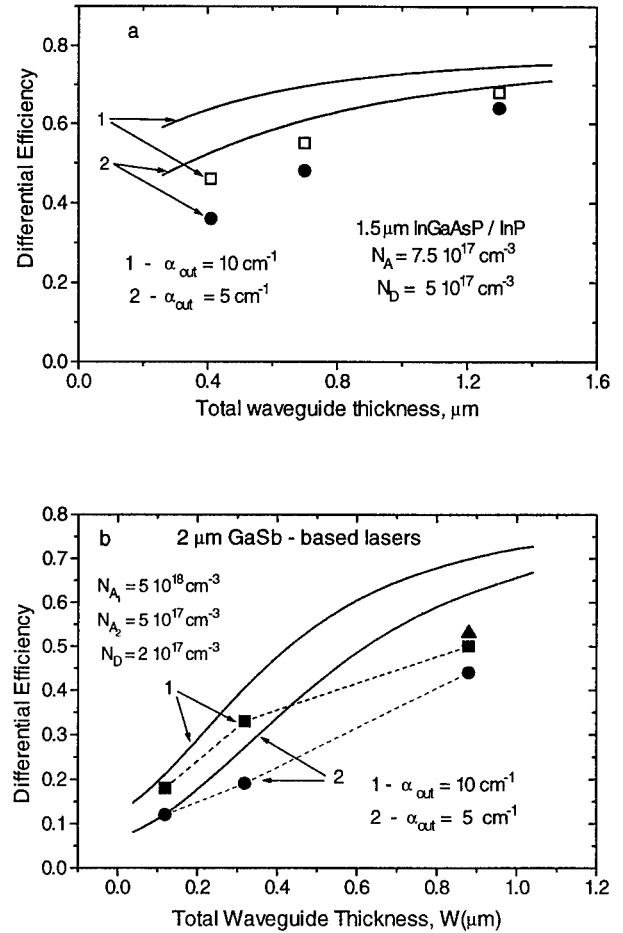
Fig. 2. *The solid lines show the upper limit of the differential efficiencies* ($\eta_{d-\text{max}}$) *as a function of W for 1.5 µm InGaAsP/InP (a) and 2 µm AlGaAsSb/InGaAsSb (b) lasers with output losses of 5 cm^{-1} and 10 cm^{-1}. Circles and squares are the experimental data for the lasers with different waveguide thickness [9, 10].*

A record low threshold current density, for a 2 µm laser, of $J_{th} = 115$ A/cm^2 was observed for AlGaAsSb/InGaAsSb SCH single QW lasers with a waveguide thickness of 0.88 µm [11]. Contrary to expectation, the decrease in Γ_{QW} with waveguide broadening does not lead to the increase of J_{th} for 2 µm or for 1.5 µm lasers. A threshold current densities of 220 A/cm^2 (73A/cm^2 per QW) was obtained from a 4 mm long 1.5 µm InGaAsP/InP laser with a waveguide thickness of 1300 nm. This is, to our knowledge, the best result for this wavelength [2, 3]. The simple calculation and experimental data show that for low output loss lasers, the negative effect caused by the decrease in Γ_{QW} with waveguide broadening completely compensated by the reduced internal losses. As a result, J_{th} does not increase with W. More detailed data on J_{th} for 1.5 µm broadened waveguide lasers are given in [9].

The broadened waveguide approach allows one to design low threshold, highly efficient laser diodes with heavily doped cladding layers. The high levels of doping in cladding layers (especially in a p-doped cladding layer where mobility is low) are essential for achieving devices with low series resistance. The 1.5 μm and 2 μm stripe laser diodes with a contact area of 0.2×2 mm, prepared from broadened waveguide structures, have a series resistance of 0.02 Ω and 0.07 Ω, respectively. The forward voltage at driving currents of about 10 A does not exceed 1.3 V for 1.5 μm lasers and 1.6 V for 2 μm lasers with such contact area.
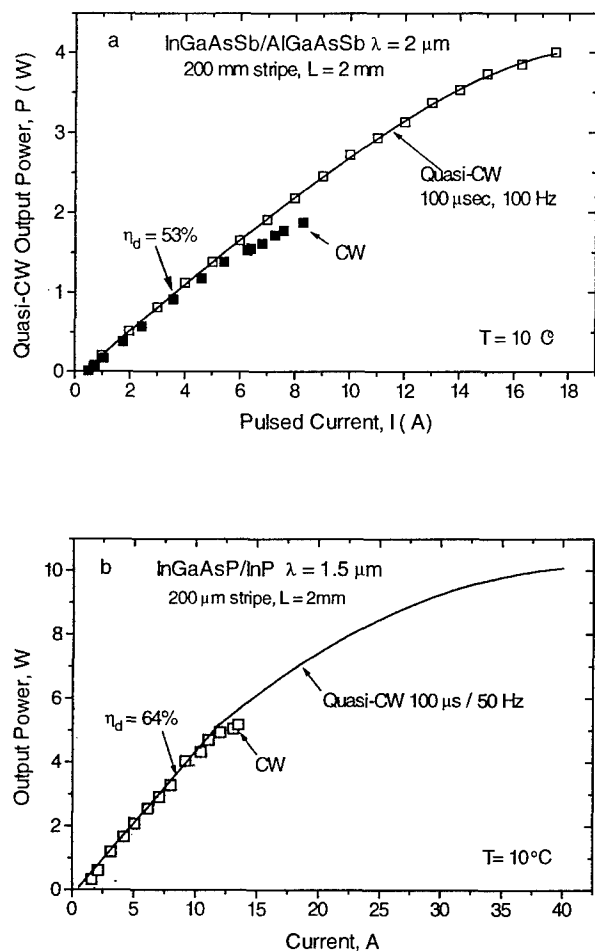
Fig. 3. *Output powers versus current in CW and quasi-CW regimes for broadened waveguide 2 μm AlGaAsSb/InGaAsSb SCH SQW (a) and 1.5 μm InGaAsP/InP SCH QW (b) lasers with high-reflective (R = 90%) and anti-reflecting (R = 3%) coatings. The lasers have a 200 μm apertures and 2 mm cavity lengths.*

As is shown in Fig. 3, the combination of features listed above provides record high continuous wave (CW) and quasi-CW output powers for 1.5 μm and 2 μm laser diodes. Fig. 3a demonstrates that 1.9 W CW and 4 W quasi-CW powers have been obtained for a 200 μm aperture, 2 mm

cavity length 2 μm AlGaAsSb/InGaAsSb SCH SQW broadened waveguide lasers. At 1.5 μm wavelength a laser with W = 1300 nm and a contact area of 0.2×2 mm achieved CW output power of 5.2 W and quasi-CW power of 10 W (Fig. 3b). These results exceed the previous achievements for high power 1.5 μm and 2 μm lasers [16, 6, 7].

In conclusion, we have shown that differential efficiencies of long wavelength, 1.5 μm and 2 μm separate confinement quantum well lasers are limited by the free carrier absorption in the cladding layers, if cladding layer doping is at the level of 5×10^{17}-10^{18} cm^{-3}, and waveguide thickness is in the ordinary range of 200-400 nm. Broadening of the waveguide up to 1 μm increases laser efficiency and does not increase threshold current densities for the lasers with output losses in the range of 2 cm^{-1} - 10 cm^{-1}. These long cavity, broadened waveguide lasers demonstrate record high output powers in continuous and quasi-continuous operation regimes.

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Low threshold InAsP/InGaP/InGaAsP/InP Strain-Compensated and Compressively-Strained 1.3μm Lasers grown by GSMBE

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Abstract

We demonstrate, for the first time, strain-compensated InAsP/InGaP/InGaAsP/InP SCH-MQW lasers grown by Gas Source Molecular Beam Epitaxy (GSMBE). Also compressively strained InAsP/InGaAsP/InP 1.3μm lasers with record low threshold current densities were obtained. The threshold current density of 210 A/cm^2 for compressively strained broad-area laser with 2.0-mm cavity was lower than the previously reported InAsP-based lasers grown by GSMBE.

I. Introduction

Laser diodes operating at 1.3-μm wavelength with low threshold current and high characteristic temperature are of great importance for application to low-cost, high performance optical telecommunication systems and optical data-links. Especially, the use of compressively-strained InAsP quantum wells with InGaAsP barriers has been the subject of considerable recent research[1]-[5]. The impetus for this research is the favorable conduction band offset of InAsP/InGaAsP as opposed to the more traditional, compressively strained quaternary wells. The limitation for this material, however, is the relatively large strain (+1.5%) that restricts the number of quantum wells, and therefore the maximum gain, that may be incorporated in a MQW laser. To overcome this problem, strain-compensation techniques

using InGaP tensile strained barriers for the quantum wells have also been paid much attention[6], [7].

In this paper, we report, for the first time, 1.3μm InAsP/InGaP strain-compensated MQW lasers grown by gas source molecular beam epitaxy (GSMBE). We also describe the record low threshold current density InAsP/InGaAsP compressively-strained MQW lasers grown by GSMBE.

II. GSMBE Growth

All laser structures were grown on (100) S-doped InP substrates in a Riber CBE32 chamber. Solid indium and gallium were used for group III sources, and AsH$_3$ and PH$_3$ were used for group V sources. Silicon and beryllium were used as n-type and p-type dopants, respectively.

The schematic diagrams of InAsP/InGaP strain-compensated
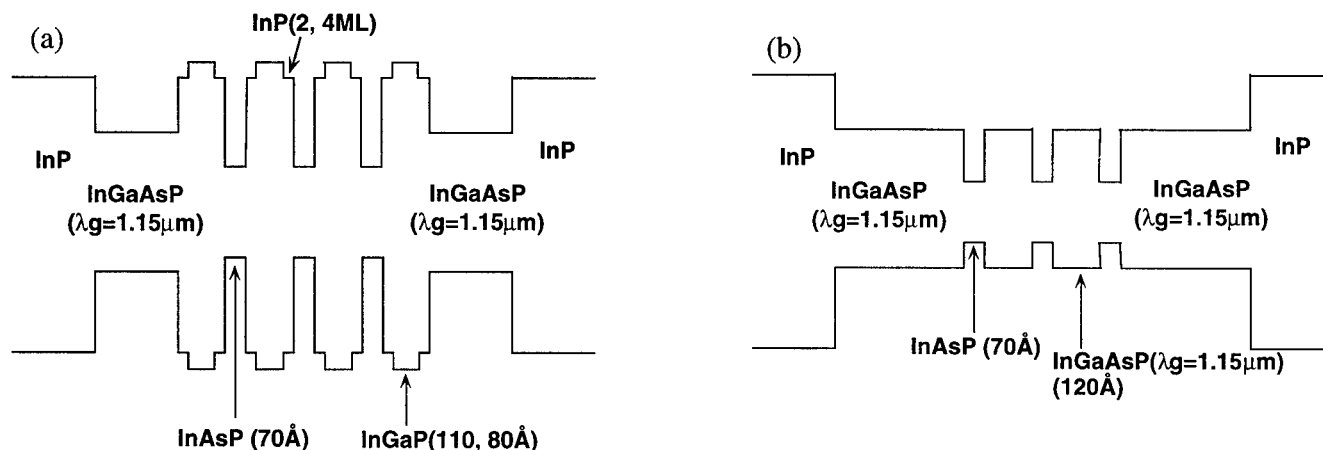
Fig. 1 Schematic diagrams of (a) InAsP/InGaP strain-compensated and (b) InAsP/InGaAsP compressively-strained MQW structures.

and InAsP/InGaAsP compressively-strained laser structures are shown in Fig. 1. The laser structures consisted of 1-μm Si-doped InP cladding layer, MQW active layer sandwiched between 1300-Å undoped InGaAsP (λg=1.15μm) optical confinement layers, 1-μm Be-doped InP cladding layer, and 650-Å InGaAsP (λg=1.15μm) contact layer. The doping profile in the n-InP layer was graded from $N_d = 3 \times 10^{18}$cm^{-3} on the n-side down to 5×10^{17}cm^{-3} at the separate confinement heterostructure (SCH) interface. On the p-side, doping profile N_a was graded from 5×10^{17} to 8×10^{18} cm^{-3} at the p contact. For the strain-compensated lasers, the MQW active region consisted of three 70-Å InAsP wells and four 110-Å (or 80-Å) InGaP barriers. The Ga mole fraction of InGaP layers was chosen so that the group III fluxes were the same as for the quaternary waveguide. Two or four monolayers of InP were inserted at the InAsP/InGaP interfaces in order to limit the formation of an uncontrolled InGaAsP layer. In case of compressively-strained lasers, 120-Å InGaAsP (λg=1.15μm) lattice matched to InP substrate was used for barrier layers instead of InGaP. InAsP MQWs were grown at 30 °C lower than the InP and quaternary layers based on an improvement in PL intensities [4].

III. X-ray Diffraction Measurements

We measured the double-crystal X-ray diffraction pattern for laser structures to estimate quantum well and barrier thicknesses
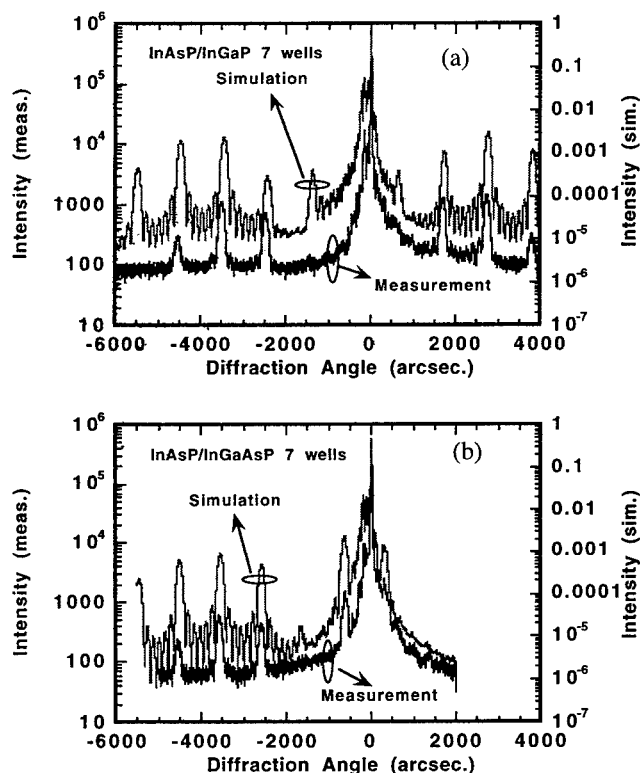
Fig. 2 Double crystal X-ray diffraction measurements results of (a) InAsP/InGaP strain-compensated MQW structures and (b) InAsP/InGaAsP compressively-strained MQW structures. Both structures have seven-wells.

and the amount of strain. Seven-well structures were grown and were used for the measurements. The measured results are shown in Fig. 2. The simulated results are also shown. Very clear and sharp satelite peaks were observed for each structure, which indicates the quantum well interfaces were abrupt. Comparison between the measured and simulated results show that the As fraction of InAsP wells was 0.51 and the Ga mole fraction of InGaP layers was 0.16. By using Vegard's law, the strain was found to be +1.6% for the InAsP well, and -1.1% for the InGaP barrier.

IV. Photoluminescence

The photoluminescence spectra of the laser structures using Ar$^+$ excitation at 488 nm are plotted in Fig.3 . For these measurements, p$^+$-InGaAsP contact and p-InP cladding layers were removed by chemical etching. The Ar$^+$ laser intensity was the same for all samples. The full width at half maximum (FWHM) was 52, 46, and 56 meV for InAsP/InGaP structures with two-monolayers of InP, InAsP/InGaP structures with four-monolayers of InP, and InAsP/InGaAsP MQW structures, respectively. This progression of FWHM indicates that the four-monolayer InP improves the interface between InAsP wells and InGaP barriers, and the sharp photoluminescence spectra indicates the high quality of InAsP/InGaP materials.

Each spectrum exhibits a knee at shorter wavelength (around 1220 nm) due to pumping of the second level in the quantum well. Prominent in the spectra of the strain-compensated lasers is a peak due to emission from the SCH waveguide region. This implies that this recombination may degrade the carrier injection efficiency into the wells, thereby reducing the internal quantum efficiency.
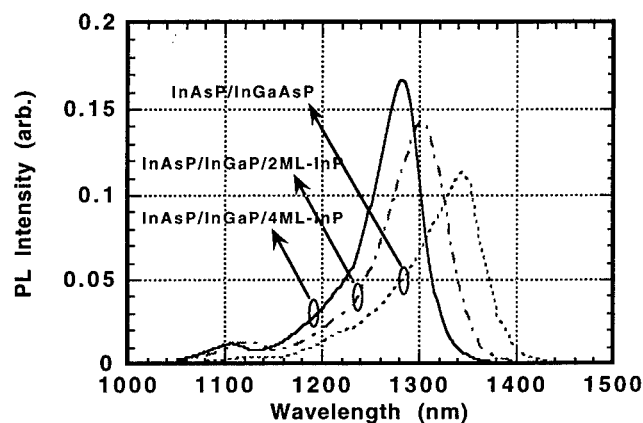
Fig. 3 Photoluminescence spectra of InAs/InP/InGaP and InAsP/InGaAsP LD wafers.

V. Laser Characteristics

We fabricated broad area lasers (110-μm ridge width) using these same structures. After forming a top-contact, the p$^+$-InGaAsP contact layer and p-InP cladding layer were removed

Fig. 4 Threshold current density as a function of inverse cavity length.
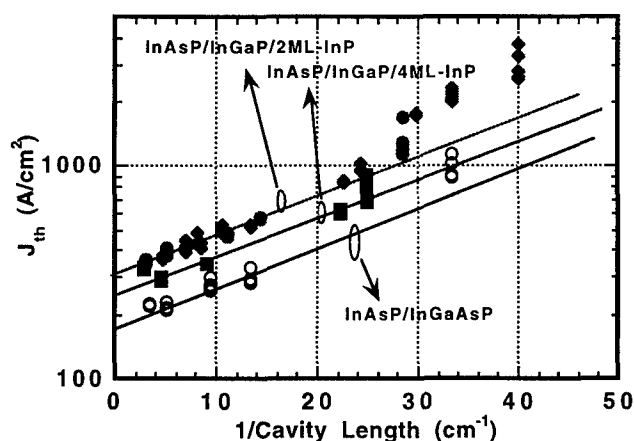
Fig. 5 Inverse external quantum efficiency as a function of laser cavity length.

Table I. The internal losses and internal quantum efficiencies for InAsP/InGaP strain-compensated and InAsP/InGaAsP compressively-strained LDs.

	J_0 (A/cm^2)	G_0 (cm^{-1})
InAsP/InGaP 3QW-110A L_B-2ML InP	72	700
3QW-70A L_B-2ML InP	75	690
3QW-70A L_B-4ML InP	85	745
InAsP/InGaAsP 3QW	85	610

Table II. The internal losses and internal quantum efficiencies for InAsP/InGaP strain-compensated and InAsP/InGaAsP compressively-strained LDs.

	α_i (cm^{-1})	η_i (%)
InAsP/InGaP 3QW-110A L_B-2ML InP	11	41
3QW-70A L_B-2ML InP	8	38
3QW-70A L_B-4ML InP	9	54
InAsP/InGaAsP 3QW	10	82

by chemical etching. Figure 4 shows the threshold current density versus inverse cavity length for both strain-compensated and compressively-strained broad area lasers. For a device length of 2 mm, we report a threshold current density of 210 A/cm^2 for InAsP/InGaAsP compressively-strained lasers. This is, to our knowledge, the best result reported for such structures grown by MBE. For InAsP/InGaP strain-compensated lasers, the threshold current density for the four-monolayer InP structure was lower than that for the two-monolayer InP structure. On the other hand, there was no difference of threshold current density between 80 and 110-Å InGaP barrier structures. We can see from these results that the suppression of the roughness of InAsP/InGaP MQW interfaces was acomplished using thick intermediate InP layers [8]. A threshold current density of 290 A/cm^2 was obtained for 2.25-mm cavity lengths. This was comparable with Ref.[6].

The threshold current density of MQW lasers is given by

$$J_{th} = \frac{N_w J_0}{\eta_i} \exp(\frac{\alpha_i + (1/L)\ln(1/R)}{N_w \Gamma_w G_0} - 1) \qquad (1)$$

where N_w is the number of wells, η_i the is internal quantum efficiency, α_i is the internal loss, L is the cavity length, R is the reflectivity, Γ_w is the optical confinement factor per well, J_0 is the threshold current density per well at transparency and G_0 is the gain per well at a current density J_0. By fitting the calculated results with measured data, we can derive J_0 and G_0. These are summarized in Table I. To compare with strain-compensated and compressively-strained lasers, strain-compensated structures show higher gain G_0 due to a larger conduction band offset.

We also show inverse external quantum efficiency versus cavity length for each type of laser in Fig. 5. The internal loss and quantum efficiencies are summarized in Table II. The internal losses were about 10 cm^{-1} with no noticeable difference among all structures. On the other hand, the compressively strained
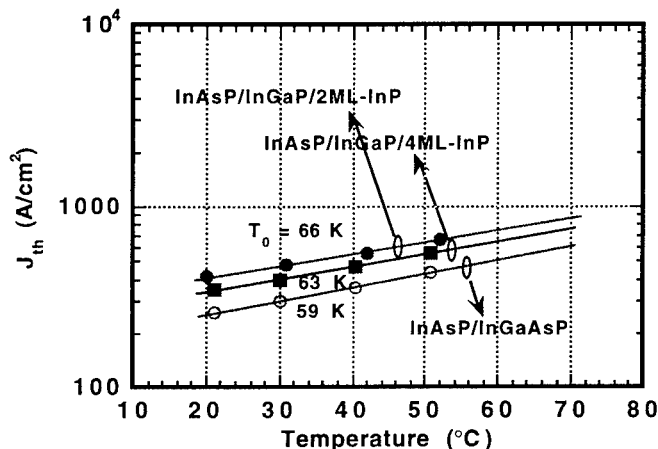
Fig. 6 Temperature characteristics of InAsP/InGaP strain-compensated and InAsP/InGaAsP compressively-strained lasers.

lasers exhibited both higher internal quantum efficiencies of 82% versus 40% to 50%. This was caused by the low carrier injection of electrons traveling in the SCH layer into the wells, as mentioned in Section III. An optimized and otherwise improved design may facilitate both the reduction in internal losses and increase in quantum efficiency of these strain-compensated lasers.

We measured the temperature characteristics for each laser, and the results are shown in Fig. 6. The characteristic temperature for strain-compensated (two-monolayer InP), strain-compensated (four-monolayer InP) and compressively-strained lasers were 66, 64 and 58 K, respectively. This slight difference in has been attributed to Ref.[6] in larger conduction band offsets,

VI. Conclusion

We have demonstrated for the first time strain-compensated InAsP/InGaP/InGaAsP/InP lasers grown by GSMBE. A record low threshold current density of 210 A/cm^2 for 2-mm long compressively-strained InAsP/InGaAsP/InP 1.3μm laser was obtained.

Acknowledgements

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High-temperature Characteristics of 1.3-μm InAsP/InAlGaAs MQW Lasers

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Introduction

Low-cost long-wavelength lasers operating at high temperatures without cooling systems are required for optical subscriber systems. InAsP multi-quantum-well (MQW) lasers have been attracting much interest because of their good high-temperature performance[1],[2]. This performance has been attributed to a large conduction band discontinuity (ΔE_c) preventing carrier leakage in the InAsP/InP system [3] compared with conventional InGaAsP/InP systems. However, our recent study revealed a relatively small ΔE_c in the InAsP/InP system. Based on this band line-up, it is possible to form a type-I band profile by using InAlGaAs as a barrier instead of InGaAsP. The InAsP/InAlGaAs QW system should have a large ΔE_c (>300 meV) sufficient to suppress the carrier leakage at a high temperature. In this paper, we present the band line-up study of this system and report on growth and characterization of this newly proposed strain-compensated InAsP/InAlGaAs MQW lasers for the first time. The lasers exhibited a threshold current density of 1.1 kA/cm^2 with a characteristic temperature as high as 116 K which is promising for realizing a cooling system free 1.3-μm laser.

I. InAsP/InAlGaAs band line-up

We have recently shown a relatively small ΔE_c ($=0.35\Delta E_g$) for an InAsP/InP heterostructure which is contrary to the reported value of $0.75\Delta E_g$[3]. Figure 1 shows the simplified band line-up of the strained InAs$_x$P$_{1-x}$ system and the In$_{0.53}$(Al$_y$Ga$_{1-y}$)$_{0.47}$As system lattice-matched to InP. In Fig. 1. the valence band edge in InP was defined as zero level. The conduction band discontinuity ratio ($Q_c=\Delta E_c/\Delta E_g$) between InGaAs and InP was assumed to be 0.4[4]. The band line-up of the InAlGaAs system was calculated assuming $Q_c=0.72$[5]. For the InAsP system, the solid line shows the band line-up for $Q_c=0.35$, where the dashed line is for $Q_c=0.75$. The suitable As composition, x, of an InAs$_x$P$_{1-x}$ QW for a 1.3-μm laser ranges from 0.4 to 0.6. Within this composition range, type-I band structure with a large ΔE_c can be formed with the InAsP/InAlGaAs QW system when Al composition, y, is larger than 0.6, while no type-I band structure can be formed assuming $Q_c=0.75$ as shown in Fig. 1.

To confirm this experimentally, we measured the photoluminescence (PL) and optical absorption spectra of the InAsP/InAlGaAs MQW. The PL samples include 5 periods of 8-nm-thick InAs$_{0.45}$P$_{0.55}$ layers and 45-nm-thick lattice-matched In$_{0.53}$(Al$_y$Ga$_{1-y}$)$_{0.47}$As layers with various Al compositions. From Fig. 1, the band structure of the MQWs can be classified into three types according to the Al compositions: (1) $0 \leq y \leq 0.2$, type-I structure with electrons and holes confined in the InAlGaAs layers, (2) $0.3 \leq y \leq 0.5$, type-II structure with electrons confined in the InAsP layers and holes in the InAlGaAs layers, and (3) $0.6 \leq y \leq 1$, type-I structure with electrons and holes confined in the InAsP layers.

Figure 2 shows the PL spectra obtained at 77 K. PL intensity decreases as Al composition increases from 0.0 to 0.5. That is because InAlGaAs layers, which have a large number of non-radiative recombination centers, are related to the radiation. In the range of $0.3 \leq y \leq 0.5$, PL peak energy was different from the optical absorption energy, indicating the type-II band structure. However, by increasing Al composition to more than 0.6, PL intensity increases and PL

linewidth becomes as narrow as 15 meV. The PL peak energy coincides with excitonic optical absorption peak energy, which also confirms the type-I band structure. Thus, we have experimentally confirmed the type-I band profile of the InAsP/InAlGaAs system having a large ΔE_c with Al composition larger than 0.6.

II. Device structure and fabrication

Figure 3 illustrates the schematic band-diagram of the active region of the strain-compensated InAsP/InAlGaAs MQW laser used in this study. The MQW consists of 7 periods of 6.7-nm-thick 1.43% compressively-strained $InAs_{0.45}P_{0.55}$ wells, 12.4-nm-thick 0.72% tensilly-strained $In_{0.42}(Al_{0.60}Ga_{0.40})_{0.58}As$ barriers. Five-monolayer-thick InP is inserted between every well and barrier to improve the optical properties. The MQW was sandwiched in a separate confinement heterostructure (SCH) including a 50-nm-thick lattice-matched $In_{0.53}(Al_{0.60}Ga_{0.40})_{0.47}As$ layer and a 50-nm-thick lattice-matched $In_{0.52}Al_{0.48}As$ layer. In this band structure the energy difference between the first electron quantum level in the InAsP well and the InAlAs layer was estimated to be 370 meV, which is sufficient to suppress the electron leakage at a high temperature.

Samples were grown on Sn-doped InP(100) substrates by gas-source molecular beam epitaxy (GSMBE). A relatively low growth temperature of 460°C was used to prevent heterointerface degradation during As, P switching. Figure 4 shows the measured and calculated double crystal X-ray diffraction spectrum of the MQW structure. Excellent agreement between the experimental spectra and the simulated one was obtained indicating high-quality structural growth of this material system.

However, the optical quality of as-grown sample is not so high because of the relatively low temperature growth of the InAlGaAs layer. Post-growth RTA (rapid thermal annealing) is known to be able to improve the performance of GaAs-based MQW lasers[6][7]. Thus, RTA was performed at 500-750°C for 10 s in flowing nitrogen gas ambient using an InP wafer as a cap to avoid phosphorus out-diffusion.

To optimize RTA condition PL measurements were performed. Figure 5 shows the room-temperature PL spectra from an as-grown sample and samples annealed at 650°C and 700°C. For the 650°C - annealed sample, the PL peak intensity was improved by more than ten times with little peak energy shift and little spectrum broadening (FWHM kept as narrow as 24 meV) after annealing indicating that there is little interdiffusion at QWs. This is also confirmed by the X-ray diffraction spectrum from the 650°C-annealed sample shown in Fig. 4(b), which is almost identical to the spectrum from the as-grown sample shown in Fig. 4(a). A further increase in annealing temperatures caused PL degradation such as peak energy shift and spectrum broadening as shown in Fig. 5(c) and saturated the improved intensities. This degradation can be attributed to an interdiffusion at the QW heterointerface.

Thus, the laser wafers were annealed at 650°C for 10 s after the growth, then processed into wide-stripe ridge waveguide lasers. The 2-μm-thick p-InP cladding layer was selectively wet-etched down to the SCH layer leaving a 20-μm-wide ridge stripe. After ridge formation, conventional passivation and metallization processes were performed.

III. Device Performance

First, the lasers were tested under pulsed-mode operation. Figure 6 shows the light-current characteristics of a 520-μm-long cavity laser with no facet coating, in the temperature range of from 25°C to 175°C. The threshold current density was 1.1 kA/cm^2 and the lasing wavelength was 1.31 μm at room temperature. The threshold current density for an infinite cavity length was estimated to be 0.6 kA/cm^2. The filled circles in Fig. 8 show the threshold current density as a function of the operating temperature for the pulsed-mode. The characteristic temperature of 116 K in the temperature range of 25°C-85°C and a maximum operating temperature of more than 175°C were obtained. The laser exhibited good temperature characteristics even with no facet coating. The differential quantum efficiency reduction was 1.4 dB from 25°C to 85°C.

CW light-current characteristics of the broad-stripe laser mounted on a Si heatsink as a p-side-up junction are shown in Fig. 7. Light power saturation was observed at temperatures greater than 100°C due to insufficient heat radiation. This power saturation might be improved by reducing the threshold current with a narrow stripe and with a highly reflective (HR) facet coating. The threshold current densities at variable temperatures under CW operation are shown in Fig. 8 by the open circles. The good characteristic temperature of 95 K and a differential quantum efficiency reduction of 2.2 dB were obtained in the range of 25°C-85°C for CW operations.

IV. Conclusion

InAsP/InAlGaAs strained MQW lasers with a large conduction band discontinuity (ΔE_c) have been proposed and demonstrated for the first time. An InAsP/InAlGaAs MQW with high structural and optical quality can be obtained by GSMBE growth combined with post-growth 650°C-RTA. A threshold current density of 1.1 kA/cm^2 was obtained for a broad stripe laser with 520-μm-long cavity length at room temperature. The lasers exhibited good temperature characteristics such as a characteristic temperature as high as 116 K under pulsed-mode operation and 95 K under CW-mode in the temperature range of 25°C -85°C .

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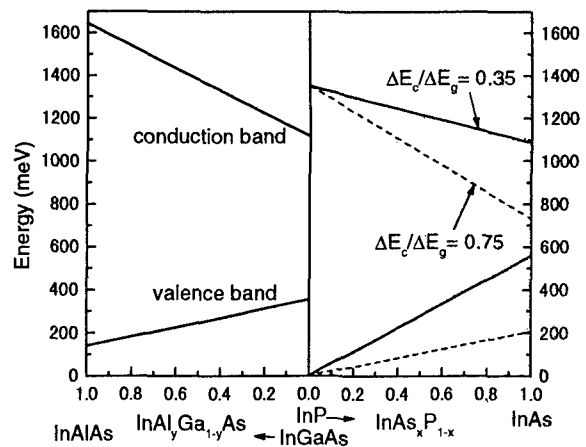
Fig. 1. Simplified band line-up of InAs$_x$P$_{1-x}$ on the right-hand side and lattice-matched In(Al$_y$Ga$_{1-y}$)As system on the left-hand side. On the right-hand side the solid line shows the band line-up for $\Delta E_c = 0.32\Delta E_g$ we found experimentally, and the dashed line is for the reported value of $\Delta E_c = 0.75\Delta E_g$.
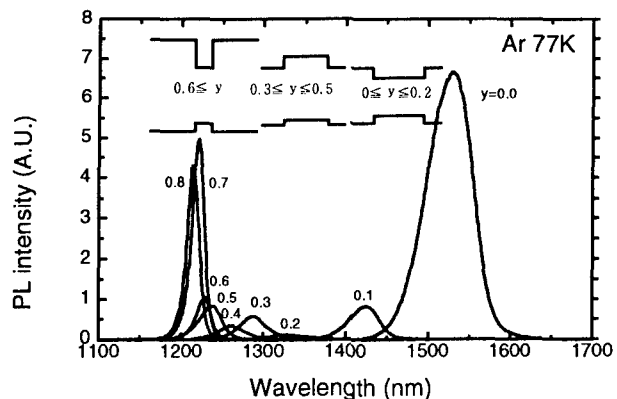
Fig. 2. The photoluminescence (PL) spectrum at 77 K from the InAsP/In(Al$_y$Ga$_{1-y}$)As MQWs with variable y (relative Al composition of barriers).

561
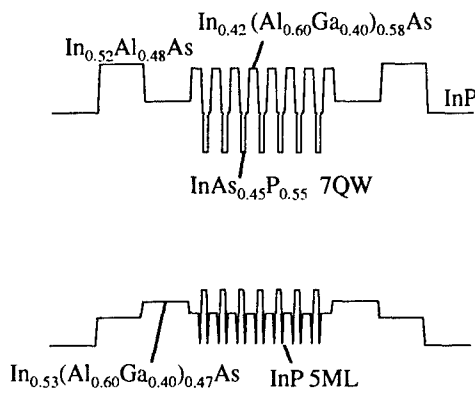
Fig. 3. Schematic band diagram of InAsP/InAlGaAs QWs. A large ΔE_c of 370 meV between InAsP quantum wells and InAlAs SCH layers was obtained.

Fig. 6. Light-current characteristics of a 520-µm-long as-cleaved laser at various operating temperatures under pulsed operation.

Fig. 4. Double crystal x-ray diffraction spectrum from (a) an as-grown sample, and (b) a 650°C-annealed sample, and (c) a simulated result.
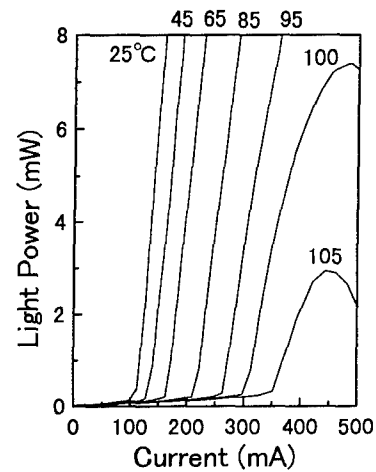
Fig. 7. Light-current characteristics of a 520-µm-long as-cleaved laser at various operating temperatures under CW-mode operation.

Fig. 5. Photoluminescence spectra from (a) an as-grown sample, at (b) a 650°C-annealed sample, and (c) a 700°C-annealed sample.
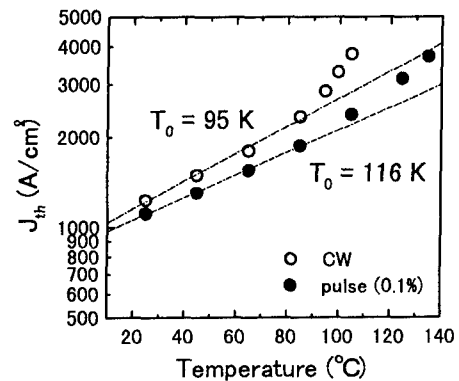
Fig. 8. The threshold current densities as a function of the operating temperature. Filled and open circles respectively denote pulsed-mode and CW-mode.

562

InAsP QUANTUM WELLS FOR LOW THRESHOLD AND HIGH EFFICIENCY MULTI-QUANTUM WELL LASER DIODES EMITTING AT 1.55 μm

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Introduction

We report the first successful use, to our knowledge, of InAsP quantum wells for 1.55 μm wavelength laser emission: 5 quantum well InAsP/InGaAsP horizontal cavity lasers showed 88% internal efficiency, 1.6 cm⁻¹ losses per well, and 33 A/cm² transparency current density per well, which equal or even surpass the best published characteristics for 1.55 μm wavelength lasers based on any material system. Strain relaxation issues do not severely limit the multi-quantum-well design since up to 17 quantum wells were integrated in a strain-balanced laser which showed equally good characteristics.

I. Background

InAsP quantum wells (QWs) were employed with success for a 1.3 μm wavelength laser emission [1-3] but there were doubts that this could be extended to a 1.55 μm wavelength emission. Indeed, a higher strain is necessary to adjust the band gap energy of InAsP and the possibility to grow a device-quality InAsP QW beyond the Matthews and Blakeslee's critical thickness [4] was questioned [2]. This issue was confirmed by Sugiura [3] who reported that double-QW InAsP/InGaAsP 1.55 μm lasers showed a high 1 kA cm⁻² threshold current density and that triple-QW structures did not yield any photoluminescence emission. In this work, we demonstrate that chemical beam epitaxy can overcome this problem, due to its low growth temperature capability.

II. MQW structure design

We chose the $InAs_yP_{1-y}$ QW thickness to be 10 nm and determined experimentally that the As content y should be 55% (i.e. 1.75% compressive strain) for a 1.53 μm photoluminescence (PL) emission, which is in good agreement with calculated values [2]. The InGaAsP barrier layers are 15 nm-thick and were grown using the same arsine and phosphine flows used for the growth of the InAsP QW layers, to achieve a constant y design [5]. This choice simplifies the growth interruption procedures and suppresses the well known As-P exchange that leads to the formation of uncontrolled composition layers at the heterointerfaces [6] between alloys with different y.

Thus the aimed barrier composition was $In_xGa_{1-x}As_{0.55}P_{0.45}$ with the indium content x chosen between 74% for a lattice-matched barrier and 57% for a tensile-strained barrier which compensates for the strain in the

QW [7]. Using this composition range, the emission wavelength of the barrier was in the 1.2 μm to 1.3 μm range.

III. Growth of MQW structure

All layers were grown at 1 μm/h with pure TMIn, TEGa, AsH₃ and PH₃ using an all-metal pressure-regulated gas manifold with no carrier gas. Because 3-dimensional growth can easily occur as a strain-relaxation driven process during the growth of such strained MQW layers [8, 9], the choice of the growth parameters must be done with care in order to avoid it. We have shown in a previous study that both the growth temperature Tg and the V/III ratio have a dramatic effect on the structural quality of strained InGaAs/InP bidimensional electron gas structures [10], and therefore we chose three sets of (Tg, V/III ratio) values that were found to be optimum in this latter study and grew 5 periods $InAs_{0.53}P_{0.47}/In_{0.65}Ga_{0.35}As_{0.53}P_{0.47}$ MQW test samples. Fig. 1 compares the X-ray rocking curves of these samples with a simulation obtained using the dynamical theory of X-ray diffraction [11]. No superlattice structure is present on the rocking curve of the sample grown at (Tg, V/III ratio) = (500°C, 8) which is an evidence for a serious degradation of the MQW layer interfaces. In contrast, the rocking curves of the samples grown with a (Tg, V/III ratio) of (480°C, 4) and (460°C, 2) are in very good agreement with the simulation. The superlattice satellite diffraction peaks have an intrinsic full width at half maximum (FWHM) and the thickness fringes between the satellites are resolved, which shows a high crystal quality. 300K PL measurements confirmed these differences in quality, as no emission was detected from the sample grown at 500°C while 460°C and 480°C samples emitted an intense 30 meV FWHM PL line.
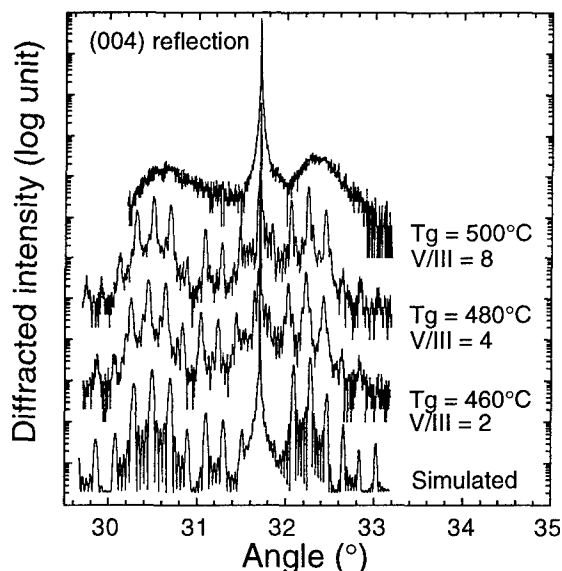
Fig. 1 X-ray diffraction rocking curves of 5-periods InAsP/InGaAsP test samples grown under different conditions

IV. Growth of laser samples

Six complete laser samples were grown with the optimized conditions. The structures are presented in Table 1 with their (Tg, V/III ratio) growth parameters, strain in QW and barrier layers deduced from X-ray diffraction analysis, the resulting average strain in the whole MQW and the lasing emission wavelength. The laser structures consist of an n-InP substrate, 200 nm-thick 10^{18} cm^{-3} Si-doped InP, the undoped MQW active layers, 1.5 µm-thick 4 10^{17} cm^{-3} Be-doped InP and a 10 nm-thick InGaAs contact layer. For samples A to D the active layers are 5-periods InAsP/InGaAsP MQWs sandwiched between two 150 nm-thick 1.1 µm wavelength InGaAsP optical confinement layers. Samples E and F have 17-periods InAsP/InGaAsP strain-compensated MQWs active layers and no additional optical confinement layers. Sketches of the 5-QW and 17-QW structures are presented on Fig. 2.

By comparing the 5-QW samples A and B, we check whether the 460°C and 480°C growth conditions are still equivalent when it comes to laser operation. With samples B, C and D we compare different degrees of strain compensation

Table 1 Growth parameters and structural characteristics of the laser samples

Sample		Tg (°C)	V/III ratio	InAsP strain %	Barrier strain %	Average strain %	laser λ (nm)
5 QW	A	460	2	1.65	-0.70	0.25	1520
	B	480	4	1.63	-0.60	0.30	1490
	C	480	4	1.77	-0.95	0.15	1560
	D	480	4	1.77	-0.20	0.55	1560
17 QW	E	480	4	1.80	-0.90	0.20	1590
	F	460	2	1.80	-0.90	0.20	1590
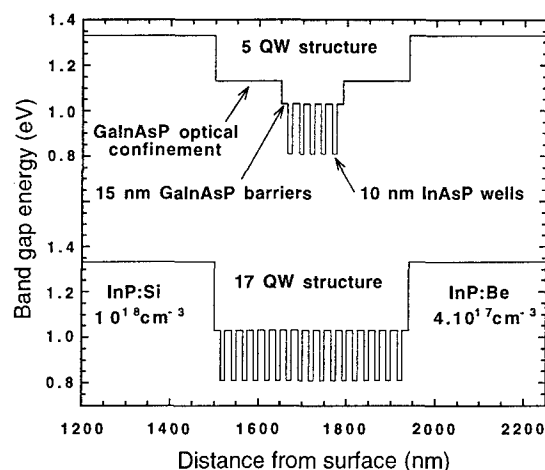
Fig. 2 Layer structures of the 5-QW and 17-QW laser diodes

in the MQW active layers. The strain-compensated 17-QW samples E and F were grown to test whether the strain-compensation technique would allow the realization of structures integrating many periods. Here again, both 460°C (sample #F) and 480°C (sample #E) growth conditions were tested.

All the samples were featureless when viewed under phase contrast optical microscope, except for 17-QW sample #E which exhibited a surface roughness distributed inhomogeneously over the sample. A degradation of the crystalline quality of sample #E as compared to sample #F is also visible on the X-ray diffraction rocking curves shown on Fig. 3 and is evidenced by broader satellites diffraction peaks. It appears that the optimum growth temperature window of the 17-periods MQW structure is reduced to lower temperature values, because the 17 QW layers are more sensitive to strain induced degradation than the 5 QW layers.
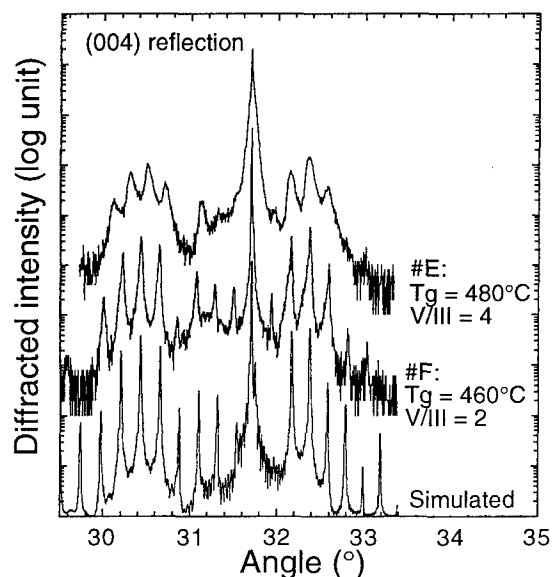
Fig. 3 X-ray diffraction rocking curves of 17-periods InAsP/InGaAsP laser samples #E and #F
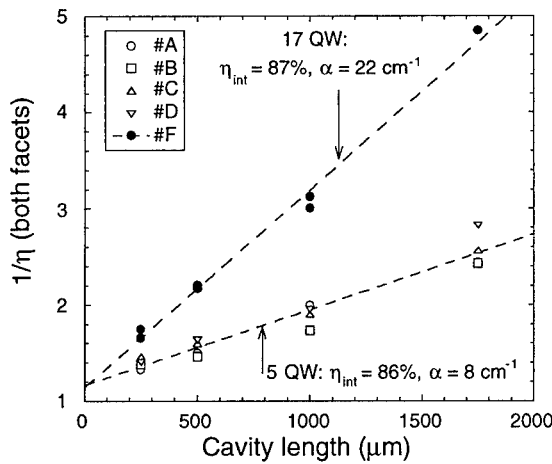
Fig. 4 Reciprocal external efficiency versus cavity length

Fig. 5 Threshold current density versus reciprocal cavity length

V. Laser characteristics

The samples were processed into 100 μm-wide mesa stripe lasers using standard etching and metallisation techniques and were cleaved to different lengths ranging from 250 μm to 1750 μm. The cleaved mirror facets were left uncoated. Laser operation was obtained at 25°C using pulsed current injection and the light-current curves were recorded up to 70 mW optical output power. The homogeneity of the laser emission on the facet was confirmed with an infrared camera. The internal efficiency η_{int} and the cavity losses α were extracted from the dependence of external efficiency η_{ext} with cavity length (Fig. 4), using

$$\frac{1}{\eta_{ext}} = \frac{1}{\eta_{int}}\left(1 + \frac{\alpha \cdot L}{\ln(1/R)}\right)$$

where L is the cavity length and R is the cleaved facets reflectivity (0.3).

A semi-logarithmic dependence of gain with current density [12] was assumed and a procedure similar to the one detailed in reference [13] was used to calculate the transparency current per well J_{tr} and the product of the optical confinement factor per well and the gain coefficient $\Gamma_w G_0$: J_{tr} and $\Gamma_w G_0$ were calculated by fitting the dependence of the threshold current densities J_{th} versus cavity length (Fig 5) with

$$J_{th} = \frac{N \cdot J_{tr}}{\eta_{int}} \cdot \exp\frac{1}{N \cdot \Gamma_W \cdot G_0}\left(\alpha + \frac{1}{L}\ln\frac{1}{R}\right)$$

N being the number of wells and using the previously determined values of η_{int} and α.

The values for η_{int}, α divided by the number of wells, J_{tr}, and $\Gamma_w G_0$ as measured for each sample are listed in table II. They are compared with the best published results obtained on strained GaInAsP/GaInAsP MQW samples grown by MOCVD [13-15]. For comparison with other published results, the minimum threshold current density J_{th}min,

measured on the longest (1750 μm) cavity lasers, is also reported on Table 2.

From Fig. 5, Fig. 6 and Table 2 it is clear that all the 5 QW lasers have very similar characteristics. The differences between these samples can be attributed to statistical data scattering. Thus, for 5 QW structures, both the 460°C and 480°C growth condition parameters appear equally good, and no clear influence of the tensile strain in the barrier is observed in the [-0.2%...-1%] range. The very high quality of all the 5 QW laser samples is indisputable: they demonstrate simultaneously state of the art values for η_{int}, α/well, J_{tr}, and $\Gamma_w G_0$ (the average values for the 4 samples are respectively 86%, 1.6 cm^{-1}, 36 A/cm^2 and 8.5 cm^{-1}) and a record transparency current density of 33 A cm^{-2} was obtained with sample #B.

The characteristics measured on sample #F is evidence that there is no degradation of the QWs quality when the number of periods in the strain-compensated MQW layers is increased up to 17. The internal efficiency remains high at η_{int}=87%. The cavity losses increase linearly with the number of wells (1.3 cm^{-1}/well) which simply shows that the losses mainly occur in the QW region, possibly free carriers absorption. A lower $\Gamma_w G_0$ value for the 17 QW laser compared to the 5 QW

Table 2 Lasers characteristics and comparison with best published values

sample	η_{int}	α/well cm^{-1}	J_{th} min A/cm^2	J_{tr}/well A/cm^2	$\Gamma_w G_0$ cm^{-1}
5 QW A	0.87	1.6	282	36	8.4
5 QW B	0.88	1.5	282	33	7.4
5 QW C	0.81	1.4	297	38	9.0
5 QW D	0.88	2.0	306	39	9.5
17 QW F	0.87	1.3	666	24	5.0
4 QW Osinski [13]	0.88	2.6	268	40	9.2
4 QW Osinski [13]	0.63	1.4	324	36	9.0
2 QW Mathur [15]	0.80	2.3	-	36	8.4
5 QW Ougazzaden [14]	0.77	1.5	328	39	9.3

ones was expected due to the lower average optical confinement coefficient of the 17 MQW structure. The impressively low 24 A/cm^2 value of the transparency current should be considered with care, as carrier injection non-uniformity is probable and makes the determination of J_{tr} and $\Gamma_w G_0$ somewhat inaccurate.

VI. Conclusion

We have presented 5-periods InAsP/InGaAsP MQW horizontal cavity lasers whose characteristics equal or even surpass the best published ones for 1.55 μm wavelength lasers. Furthermore, up to 17 periods have been integrated in a strain-balanced MQW structure without showing any degradation of the laser characteristics. It must also be noted that all the laser samples that were grown with the optimal conditions, seven at this date, on a four months time scale, gave very similar results: the characteristic values reported here are typical ones. InAsP is thus definitively a good choice for low threshold and high efficiency MQW lasers emitting at 1.55μm.

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Fabrication of a 1.3-μm-wavelength multiple-quantum-well laser on a (211)A InP substrate

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Abstract

We demonstrate crystal growth and fabrication of a long-wavelength laser on a (211)A InP substrate, with the expectation of reducing threshold current density by applying substrates of (n11) surface orientation. We examined samples InGaAs(P) SQWs of various thickness. We found that InGaAsP SQWs could be fabricated with good optical properties provided the SQW layers were not made too thin. However, the properties of the InGaAs SQWs tended to be degraded probably due to the difficulty of exchanging group-V gases at the heterointerfaces. A laser that had an unstrained InGaAsP/InGaAsP MQW active layer emitting at 1.3-μm was fabricated on a (211)A substrate. Its threshold current density was 900 A/cm^2, which is comparable to the value for the same type of laser on a (100) substrate. These results suggest that long-wavelength lasers with satisfactory quality can be fabricated on a (211)A substrate.

I. Introduction

Properties of semiconductor lasers have been remarkably improved by applying a strained multiple-quantum-well (MQW) layer to their active region. Further improvement is required especially in terms of lowering threshold current density (J_{th}) and obtaining stable operation at high temperature. However, the improvement that is possible with the strained MQW approach now seems to be in its final stage. Hence, new techniques to better laser properties are needed.

Fabricating lasers on non-(100)-oriented substrates is a technique that may be suitable for such a purpose. Ten years ago, it was reported that an AlGaAs laser fabricated on a (111)A GaAs substrate had a lower J_{th} than that of a laser on a (100) GaAs substrate[1]. Since then, research has been widely performed on crystal growth and device fabrication on non-(100)-oriented substrates, especially on substrates with (n11)-expressed orientation. This research has been aimed not only at reducing J_{th} of the laser, but also at producing other effects such as second harmonic generation[2,3]. However, most of the research has been on GaAs and short-wavelength devices, and the research on InP has been very limited: fabrication of lasers on (011) and (311)B InP substrate has been reported, although the superiority in applying the (n11) orientation was not clarified[4,5]. On the other hand, the dependence of a long-wavelength laser's properties on its substrate surface orientation has been investigated for (n11)-expressed orientation by simulation[6]. The results implied that the

orientation near (211) was the most effective in reducing J_{th}.

In this paper, we report on crystal growth and laser fabrication on a (211)A InP substrate, to examine the possibility of improving laser properties by applying this orientation. InP-based layers were grown on (211)A InP substrates by metalorganic vapor-phase epitaxy (MOVPE), and a 1.3-μm-wavelength laser that had an unstrained MQW active layer was fabricated using the resulting crystal.

II. Crystal Growth conditions and evaluation of SQWs

MOVPE growth on a (211)A InP substrate was carried out in a vertical reactor. The background pressure in the reactor during the growth was 55 torr, and the growth temperature was 620°C. Trimethylindium (TMI), triethylgallium (TEG), PH$_3$, and AsH$_3$ were used as source materials, and Si$_2$H$_6$ and dimethylzinc (DMZn) were used as n-type and p-type dopant gases respectively. We began by observing the dependence of the surface morphology on the V/III ratio. The surface was milky when the ratio was lower than 100. Within the ratio of 200 to 750, the grown surfaces appeared smooth and there was no clear dependence on the ratio. We set the ratio at 450 throughout this work, choosing a high value to be safe.

First, we grew and examined a structure that comprised InGaAs(P) single quantum wells (SQWs) with various thicknesses. Figure 1 shows the layer structure and schematic lattice order around a 0.5-nm-thick SQW. Figure 2(a) shows a cross-sectional image taken with a transmission electron microscope (TEM) of a structure comprising InGaAs SQWs, and a high-resolution TEM
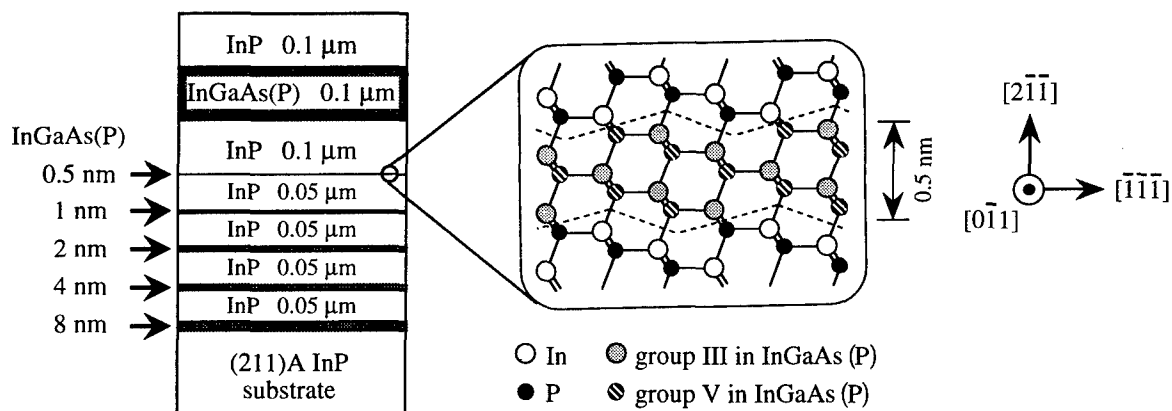
Figure 1 Schematic diagram of the layer structure which comprises InGaAs(P) SQWs with various thicknesses, and the lattice order around the 0.5-nm-thick SQW.
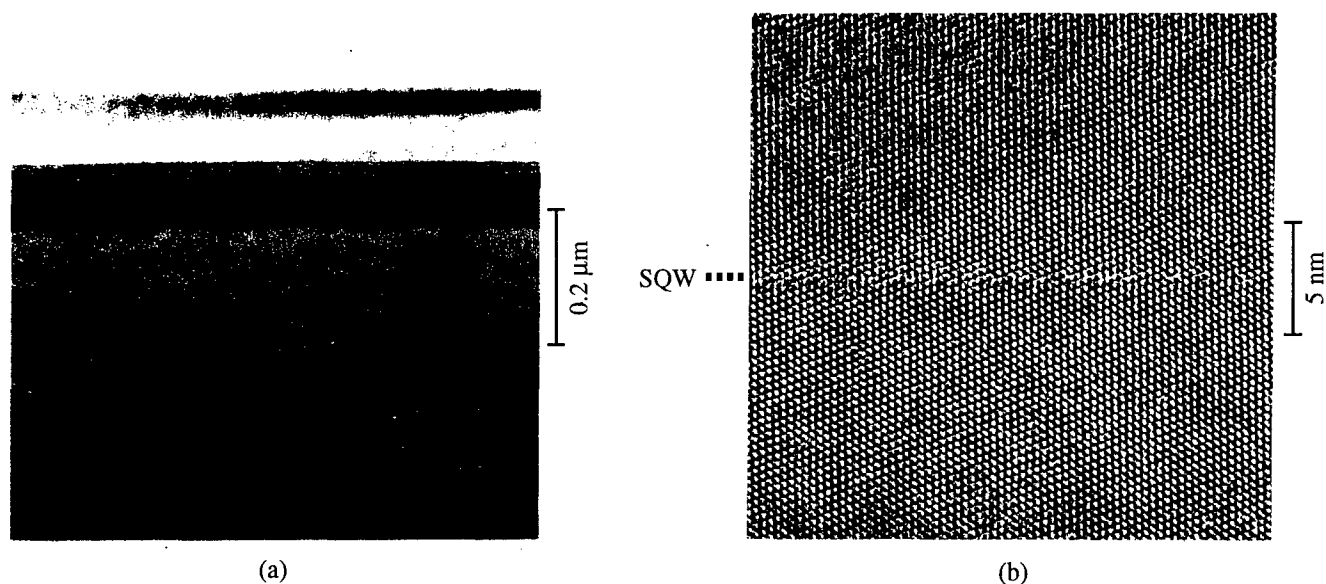
Figure 2 (a) Cross-sectional TEM image of a structure comprising InGaAs SQWs and (b) high-resolution TEM image of the area near the 0.5-nm-thick SQW.

image of the area near the 0.5-nm-thick SQW is shown in Fig. 2(b). As shown in these TEM pictures, there is no sign of dislocations in this structure, and all InP/InGaAs and InGaAs/InP heterointerfaces are flat even at the interfaces of the thin 0.5-nm-thick SQW. However, we can see some undulation in the lattice order at the interface in the high-resolution picture, as indicated by the broken lines in the schematic lattice order in Fig. 1.

The photoluminescence (PL) was measured for samples with the structure shown in Fig. 1, but without the 0.1-μm-thick InP and InGaAs top layers. Figure 3 shows 77-K PL spectra from samples of (a) InGaAs SQWs on (211)A and on (100), and (b) InGaAsP (λg=1.4 μm) SQWs on (211)A and on (100). Growth on the (100) InP substrate was done at the same time as the growth on (211)A. Comparing the spectra from the InGaAsP SQWs

in (b), we see that the intensity and the half-width of the peaks on the (211)A substrate are equivalent to those on the (100) substrate, except for the 0.5-nm-thick SQW. The peak of the 0.5-nm-thick SQW appears to have been degraded due to the effect of undulation in the lattice order at the interface, as shown in Fig. 2(b). On the other hand, comparing the spectra in (a), degradation is observed on all SQWs, not only on the 0.5-nm-thick SQW. This suggests that the InP/InGaAs and InGaAs/InP interfaces were not optically flat enough, probably because the group-V-gas exchange is difficult between PH_3 and single AsH_3. Nevertheless, the results indicate that InGaAsP SQWs could be fabricated with good optical quality, as far as the layer thickness was not too thin to be affected by lattice undulation.

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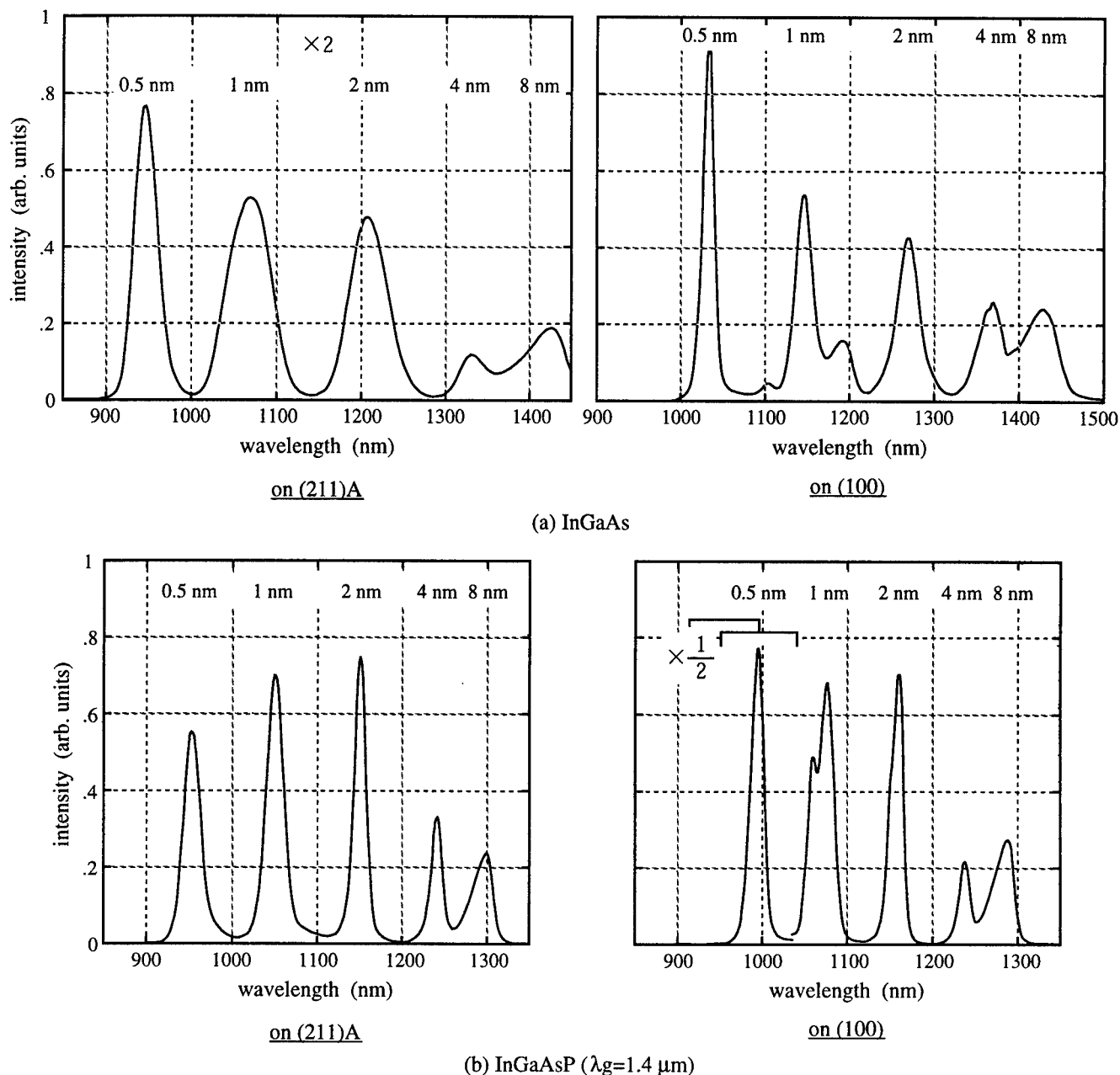
Figure 3 77-K PL spectra from samples which comprise (a) InGaAs SQWs and (b) InGaAsP SQWs
on (211)A and (100) InP substrates

III. Laser Fabrication

Next, we fabricated a long-wavelength laser on a (211)A InP substrate. This laser had a broad-area mesa-stripe structure. Its active region was an unstrained MQW layer that consisted of five 5-nm-thick InGaAsP wells separated by six 10-nm-thick InGaAsP ($\lambda g=1.15$ μm) barriers. The quaternary composition of the wells was the same as that of the SQWs examined above. Figure 4 shows the PL spectrum of the MQW on a (211)A substrate at room temperature, together with that of an MQW simultaneously grown on a (100) substrate. The shapes of these two spectra are very similar in that they both have a

half-width of 47 meV and similar intensities, which shows the good quality of the MQW on (211)A. Figure 5 shows the current-light (I-L) and current-voltage (I-V) characteristics of the laser on a (211)A InP substrate under CW operation at room temperature. The mesa width of this laser was 20 μm and the cavity length was 400 μm. The characteristics shown in Fig. 5 are equivalent to those of a similar laser fabricated on a (100) InP substrate. The threshold current was 74 mA, and Jth was calculated to be 900 A/cm^2, which is equivalent to or lower than the value of similar lasers on (100). The characteristics temperature (T$_0$) of this laser was 50 K between 20 and 50^{0}C.

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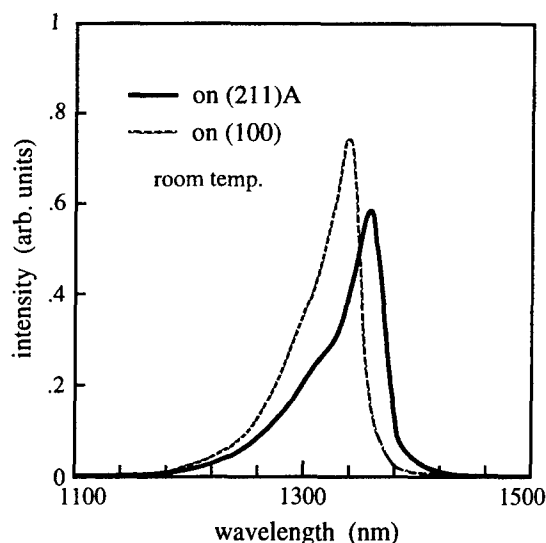
Figure 4   Room-temperature PL spectra of 1.3-μm -wavelength InGaAsP/InGaAsP MQWs grown on (211)A and (100) InP substrates.
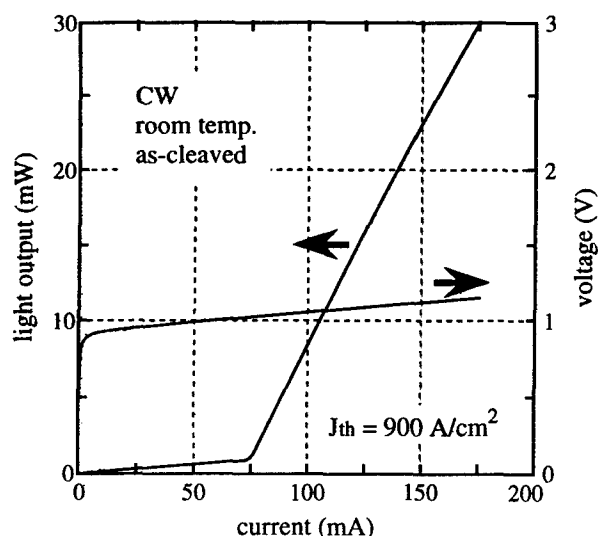
Figure 5   I-L and I-V curves of a 1.3-μm-wavelength MQW laser fabricated on a (211)A substrate under CW operation at room temperature.

We simultaneously fabricated a laser on a (100) InP substrate, but this laser showed very poor characteristics. This is because the p-type doping conditions were not appropriate for growth on (100). The doping characteristics on (211) A are very different from those on (100)[7]: in our case, the p-type concentration increased by more than one order on (211)A compared to the concentration on (100) under the same growth conditions, and, in contrast, the n-type concentration fell to about half

of the concentration on (100). Thus, layers have to be grown separately on (211)A and (100) to obtain good laser characteristics on both substrates.

IV. Conclusion

We have investigated MOVPE growth and fabrication of an unstrained MQW laser on a (211)A InP substrate, to see whether it is possible to reduce Jth by using this surface orientation. We first examined structures with InGaAs(P) SQWs of various thickness. The interfaces of the InGaAs SQWs appeared flat in the TEM images, but they were not flat enough optically. On the other hand, optical properties of the InGaAsP SQWs were as good as the properties of SQWs on a (100) substrate, except for the 0.5-nm-thick SQW which might have been thin enough to be affected by undulation in the lattice order at the interface. We fabricated a 1.3-μm-wavelength laser which had an unstrained InGaAsP/InGaAsP MQW active layer. This laser had a low Jth value of 900 A/cm², comparable to what can be obtained from the same type of laser on a (100) substrate. These results suggest that long-wavelength lasers with satisfactory quality can be fabricated on (211)A substrates.

Whether laser properties can be improved by applying the (n11) orientation has not been clearly demonstrated yet, but our results did not fall short of our expectations. Our prediction, based on a simulation, is that the expected effect of reducing Jth will become apparent when a strained MQW is applied to the active region[6]. Examination on strained MQW lasers will give us the answer to the question.

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15 May 1997

Optoelectronic Hybrid Technologies

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SUMMARY NOT AVAILABLE

UNIFORM FORMATION OF A QUARTER-MICRON PERIOD DIFFRACTION GRATING ON A 2-INCH InP WAFER USING REACTIVE BEAM ETCHING

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ABSTRACT

Uniform formation of a 250-nm period diffraction grating on a 2-inch InP wafer was demonstrated using a Br2-N2 mixed gas reactive beam etching method. The electrically isolated configuration of the wafer on an etching holder is essential for obtaining rectangular shaped groove gratings. Distribution of secondary electrons generated on the holder is considered to be the dominating cause of the etching efficiency. By using a cover plate in front of the wafer, uniform distribution of the secondary electrons and uniform etching are achieved. The use of low gas pressure conditions was shown to be effective in the formation of gratings deeper than 1 μm.

I Introduction

Cost reduction of semiconductor optical devices is indispensable for the development of all optical networks. A full wafer process has been shown to be very effective for device fabrication, [1] while the uniform formation of a quarter-micron period diffraction grating on a 2-inch InP wafer is a subject that remains to be investigated. Dry etching techniques have been tested[2,3] because of their reproducibility instead of conventionally used wet etching techniques. Since the shapes of dry etched grooves for diffraction gratings are not restricted by the chemical properties of InP, the gratings will produce many useful optical characteristics. A blazed grating with high diffraction efficiency[4] can be made by using anisotropic dry etching. Grooves more than 1-μm deep formed on a waveguide can act as a clad-grating reflector and can be used to make one-step growth DFB and DBR lasers. [5] To apply these gratings to InP devices, detailed studies of dry etching for InP submicron structures are required. In this paper, essential etching factors for the uniform formation of the gratings on a 2-inch wafer are studied by using the beam etching method previously reported by the authors.[6] Quarter-micron size grooves whose depth is over 1 μm are fabricated. A waveguide Bragg filter made using the dry etching process and regrowth process is demonstrated as an example of an application for the grating device.

II Experiment
(A) Beam etching system

The etching system used in this experiment is shown in Fig. 1.[6] A 6-inch-diameter plasma chamber and an 11-inch-diameter etching chamber were evacuated by a turbomolecular pump and operated at a base pressure of 2×10^{-8} Torr. An electron cyclotron resonance (ECR) plasma produced by a 2.45-GHz microwave input was used as an ion source. The input power is 40 W
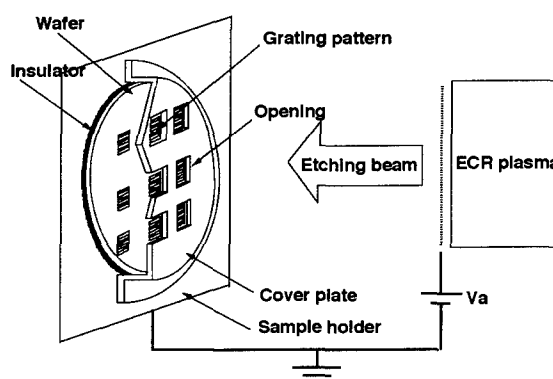
Figure 1. Schematic diagrams of the etching system. Va is voltage extracting a beam from the ECR plasma.
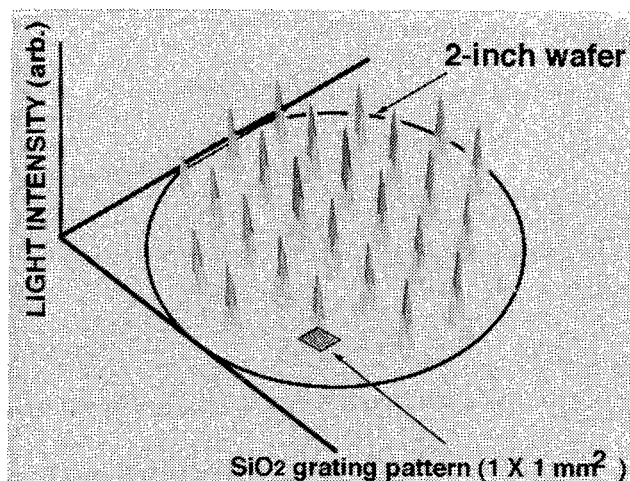
Figure 2. Mapping of diffracted light intensity.

for all experiments. The etching beam was extracted by applying a voltage Va to the ion source. The Br2 and N2 etching gases were supplied into the plasma chamber through a mass flow controller. Gas pressure was measured with a diaphragm pressure gauge. The etching samples were placed on the molybdenum holder and heated to 100 °C with a buried heater. The temperature was measured with a radiation pyrometer from the outside of the etching chamber through a sapphire view port.

(B)   Patterning of a quarter-micron period grating and it's diffraction mapping evaluation

The etching samples were Sn doped n-type InP (001) wafers. After depositing a 0.2-μm-

thick SiO2 layer on the wafer, a line and space pattern of ZEP resist whose period was 250 nm was formed by electron beam lithography. The patterns have a 1 mm×1 mm area and positioned with a space of 8 mm on a 2-inch wafer. Then, the patterns were transferred to the SiO2 film by C2F6-RIE and was used as an etching mask.

At each step of these patterning processes, uniformity of the resist pattern and the SiO2 mask pattern was evaluated by measuring optical diffraction characteristics.[7] The 2-inch wafer was placed on the step moving stage and was irradiated by He-Cd laser light whose beam diameter was about 0.2 mm. The laser light intensity diffracted by the patterns on the wafer were monitored and mapped out corresponding to the moving steps. The mapping result of the SiO2 mask pattern is shown in Fig. 2. The intensity of the diffracted light from each pattern over the whole wafer shows the same value. This indicates that the SiO2 mask patterns are made with a good uniformity.

IV   Etching results and discussions
(A) Etching of rectangular grooves
The etching of rectangular grooves is essential for making various types of gratings such as a saw-tooth-shaped blazed grating and a clad-grating. Typical etched shape was found to depend on the electrical configuration of the sample on the holder. When the samples were directly placed on the holder, the etched grooves showed wedge-
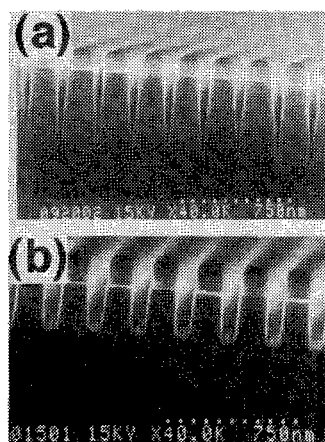
Figure 3. Dependence of the etched shapes on the configuration of the sample. (a) is observed when the sample was directly placed on the holder and (b) is obtained when the insulator was used (see Fig. 1).
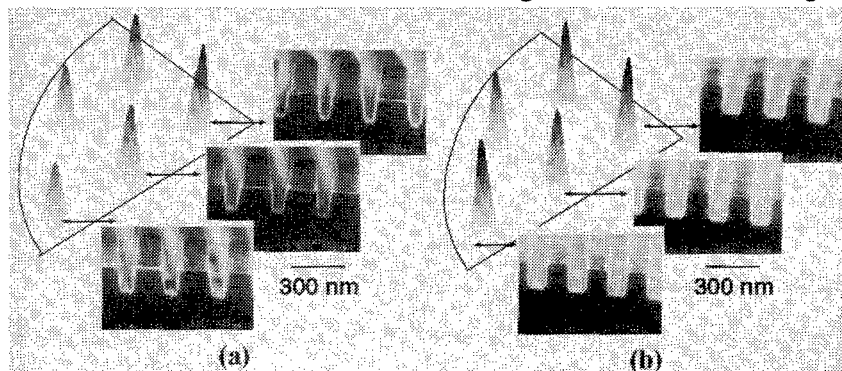
Figure 4. Diffraction mappings and cross-sectional SEM photographs of the shallow grating. These evaluations were carried out for a quarter of a 2-inch wafer. (a) is the grating etched without the cover plate and (b) is with the cover plate.

575
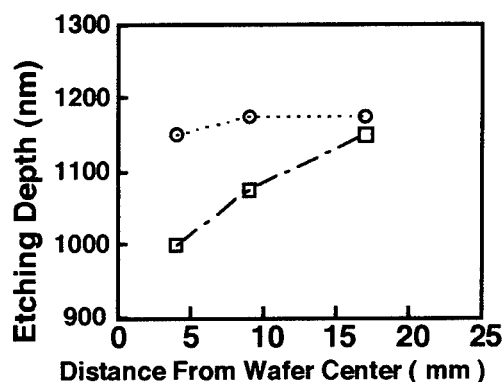
Figure 5. Dependence of etching depth on the distance from the wafer centers. $\bigcirc$ and $\square$ are the groove depth etched with and without the cover plate.

Figure 6. Dependence of the groove shape on the gas pressure. The gas conditions are (a) Br2 (0.05 mTorr) + N2 (0.35 mTorr) and (b) Br2 (0.05 mTorr) + N2 (0.08 mTorr).

shapes regardless of the etching parameters such as gas pressure, input microwave power, and beam acceleration voltage, as shown in Fig. 3(a). Due to the extremely narrow point of the grooves, the regrowth process for a cladding layer over these grooves is confronted with difficulties. On the other hand, when the samples are mounted on the holder sandwiching the insulator as shown in Fig. 1, the wedge-shaped free grooves were formed, as shown in Fig. 3(b).

In order to etch the rectangular grooves consisting of vertical side walls and a flat bottom surfaces without the side etching phenomenon, the etching condition of low Br2 gas pressure (i.e., Type I in Ref. 6) was used. Etching under Type I conditions is induced by the ambient Br2 gas species and the electrically neutral N2 beam, where the neutral beam is produced by the secondary electron generated by the N2 ion incident into the sample holder. When the sample wafer is mounted on the holder using the insulator, the secondary electron is generated only from the holder surface surrounding the wafer and not from the wafer surface. Due to the ununiform generation, the amount of the neutral N2 beam assisting the etching decreases at the center of the wafer compared with the periphery. The unbalanced distribution of the N2 beam is solved in this experiment by using a conductive cover plate in front of the wafer, as shown in Fig. 1. The cover plate has openings at the region corresponding to the etching pattern on the wafer and is electrically connected to the holder. Thus, the secondary electrons are generated from the

whole surface through the plate.

Etching was carried out under the conditions of Va=350 volt, 100℃ sample temperature, and etching time of 3 min. The etched gratings were evaluated from the diffraction mapping measurements and the SEM observation of their cross section. The results for one quarter part of the 2-inch wafer are shown in Figs. 4. The V-shaped grating at the wafer center changes into a U-shape at the wafer periphery when a cover plate is not used (Fig. 4 (a)). Diffracted light intensity change was also observed. The origin of the change is considered to be the unbalanced distribution of the N2 beam. When the cover plate was used, uniform gratings with rectangular shapes were obtained regardless of their positions (Fig. 4(b)). Uniform diffracted light intensity was also observed.

(B) Deep groove etching

An etching of grooves more than 1-mm deep is necessary for clad-grating devices. As a result of investigating the etching using various parameters, two significant features were observed. One is the distribution of the groove depth on the wafer as shown in Fig. 5. When the cover plate is not used, the grooves positioned at the periphery of the wafer are deeper than those at the wafer center. The uniformity of the depth is improved by using the cover plate. The results indicate that the distribution of the amount of secondary electrons and that of the incident neutral N2 beam are made uniform by the cover plate. The

576

other feature is the shape of the grooves. The typical shapes obtained here are shown in Fig. 6. The groove width increases at the middle part of the depth for the N2 gas pressure of 0.23 mTorr. This shape can be eliminated by lowering the N2 gas pressure to 0.08 mTorr.

V Application to waveguide Bragg filter

As an example of device application for the dry-etched grating, waveguide Bragg filters were fabricated on the 2-inch wafer. After a 0.1-μm depth first order grating was etched into a 0.3-μm-thick core layer ($\lambda g = 1.3$ μm), the cladding layer was re-grown. The rectangular grating was successfully buried as shown in the cross-sectional SEM photograph of Fig. 7. Then, 2-μm-wide high-mesa type waveguides were formed on the 100-mm-length grating region. The measured transmission spectrum of the Bragg filter is shown in Fig. 8. Owing to a large coupling coefficient obtained using the 0.1-μm deep grating which is deeper than that widely used wet etching gratings, a wide-band spectrum could be achieved.

VI Summary

The uniform formation of a quarter-micron period diffraction grating on a 2-inch wafer was demonstrated using a cover plate placed in front of the wafer. The plate is considered to make the distribution of secondary electrons uniform. The use of low gas pressure conditions was shown to be effective in the formation of gratings deeper than 1 μm which can be used for clad grating.
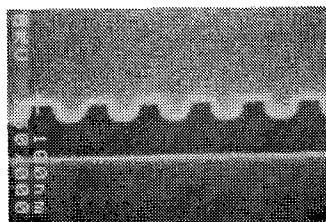
Figure 7. Cross-sectional SEM photograph of the buried grating.
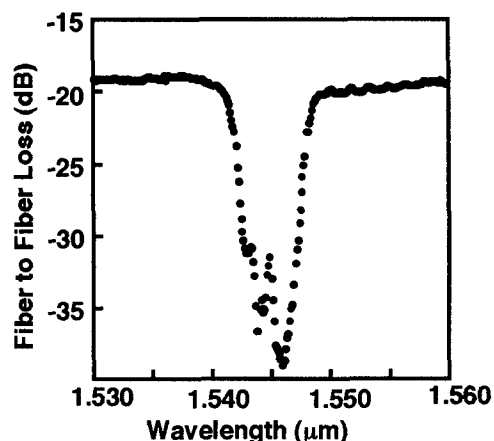
Figure 8. Transmission spectrum of the fabricated waveguide Bragg filter.

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Low Damage Reactive Ion Etching Process for Fabrication of Ridge Waveguide Lasers

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Introduction

The damage produced during CH_4/H_2 reactive ion etching (RIE) processes has been measured using low temperature photoluminescence. The damage depth profile was estimated and a low level damage RIE process has been developed. The process has been used to fabricate InGaAs/InGaAsP ridge waveguide lasers containing 5 quantum wells with threshold currents, 43-45 mA for 500 μm lasers, that are indistinguishable from those of wet-etched devices.

I. Background

Dry etching is a widely used process in the fabrication of waveguide optoelectronic devices, due to its highly anisotropic etch profile which produces vertical sidewall and good dimensional control. Dry etching processes involve particle bombardment which, unfortunately, causes damage to be imparted to the material being etched leading to the degradation of the optical and electrical properties of the material[1,2,3,4]. It is therefore of great importance to understand and assess the damage, and investigate possible low damage processes for the fabrication of optoelectronic devices.. When used in the fabrication of lasers this damage can have a detrimental effect on the performance of the devices, varying from increasing the threshold current to killing lasing action entirely. It is therefore of great importance to understand and assess the damage, and develop low damage process for the fabrication of optoelectronics devices.

Currently, reactive ion etching (RIE) based on CH_4/H_2 is the most widely used dry etching technique for structures containing In, because it can give excellent surface morphology and anisotropy [5,6] compared to RIE using Cl and Br containing compounds [7] However the damage introduced during the RIE CH_4/H_2 process can have detremental effects on the characteristics of optoelectronic devices (e.g. ridge waveguide lasers), and, in some cases, dry etched devices fail to operate at all.

The damage caused by RIE of an InGaAs/InP quantum well structure using CH_4/H_2 was

investigated. The RIE damage was assessed by measuring the damage depth profile using a low temperature (5 K) photoluminescence (PL) technique, with specially designed multiquantum well (MQW) material. Post dry etching annealing was also carried out to investigate its impact on the removal of dry etch damage. Finally, 3μm wide ridge waveguide InGaAs/InGaAsP MQW lasers were fabricated by RIE dry etching followed by a post-annealing procedure and were compared with those from lasers fabricated using wet chemical etching.

II. Experimental

The structure used to study the dasmage caused by CH_4/H_2 RIE contained 5 wells of widths (from the surface downwards) 20 Å, 40 Å, 60 Å, 80 Å and 120 Å, the top 4 wells being separated by 200 Å of InGaAsP ($\lambda_g = 1.26$μm) barriers. The bottom well was placed at a depth of 4100 Å from the surface, deeper than any damage induced by the RIE, and was used to provide a reference signal for normalising the photoluminescence (PL) signals. On top of the uppermost well, 200 Å of the quaternary and a 100 Å cap of InP were grown.

The RIE was performed in a conventional 13.56 MHz parallel plate system at a chamber pressure of 14 mTorr with the cathode held at a temperature of 30 °C by circulating cooling fluid. The gas flow rates were 7.2 sccm for the CH_4 and 52 sccm for the H_2. The etching power was varied from 20 W to 100 W.

To measure the etching rates, samples patterned with a SiO$_2$ mask were etched for periods from 15 mins to 30 mins at different plasma power levels, then measured using a depth profile meter. In order to determine the damage caused by the etching process samples were etched by the CH$_4$/H$_2$ plasma for 12 s at plasma powers of 20 W, 50 W and 100 W. After etching, annealing was performed at 500 °C for 60 s using a rapid thermal annealer (RTA) to remove the damage. PL was measured at 5 K before etching, after etching and after annealing.

3 μm wide ridge waveguide lasers were fabricated by both wet chemical etch and RIE dry etch. The damage can estimated indirectly by comparing the performance of the lasers. The laser material which contained 5 InGaAs/InGaAsP QWs in the active region which was 1.5 μm below the surface, was grown by MOVPE and was similar to that used by McKee et al (8). A plasma power of 50 W was used to etch the ridge waveguide. This etching power was chosen because it has a relatively high etch rate and causes relatively little damage. The ridge height was about 1.2 μm. After etching, the sample was annealed at 500 °C for 60 s. A 200 nm thick SiO$_2$ passivation layer was deposited and contact windows were opened on top of the ridges. The samples were then thinned and metal contacts were evaporated, Ti/Au for the p-type and Au/Ge/Au/Ni/Au for the n-type, which were annealed at 400° C for 60 s in the RTA. The samples were then cleaved to a length of 500 μm.

III. Results and Discussion

The measured etch rates for the CH$_4$/H$_2$ RIE were 28 nm/min for a plasma power of 20 W, 72 nm/min for 50 W and 96 nm/min for 100 W. The surface morphology of these samples was examined using a scanning electron microscope, it was found that the samples etched at 100 W showed visible surface roughness, whereas, the morphology of the surface etched at 20 W plasma power was smooth.

The results of the PL measurements are shown in Fig. 1. It can be seen that there is a significant reduction in the intensity of the PL signal of the two uppermost wells for all the etching powers, indicating that there is a significant amount of damage occurring to a depth of at least 300 Å, even at the lowest etching power investigated.

For all but the deepest well, there is significant broadening of the PL signal indicating that some damage is propagating at least 900 Å into the structure. This broadening increases with increasing power (Fig. 2), so the peaks merge together
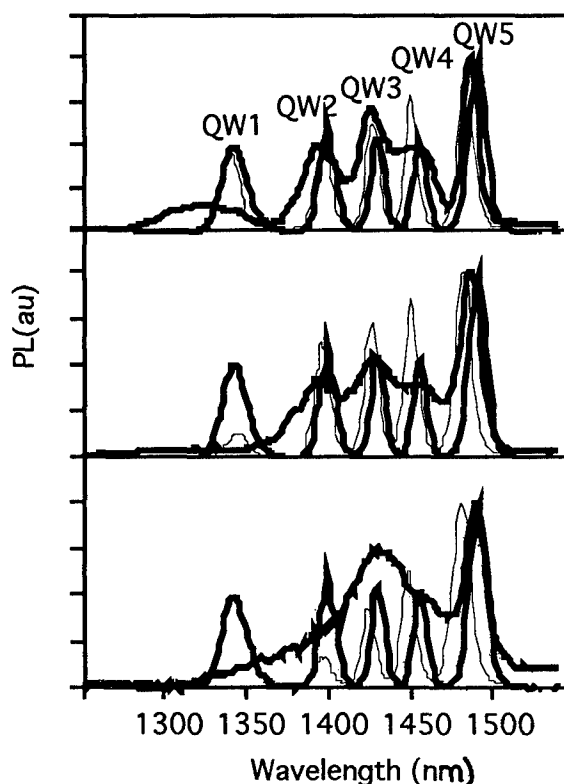
Fig.1 The low temperature PL intensity as a function of wavelength. The plasma powers are 20W, 50W, 100W respectively from the top to the bottom. ▪▪▪▪ as-grown, ▬▬▬ after etching and ──── after annealing.
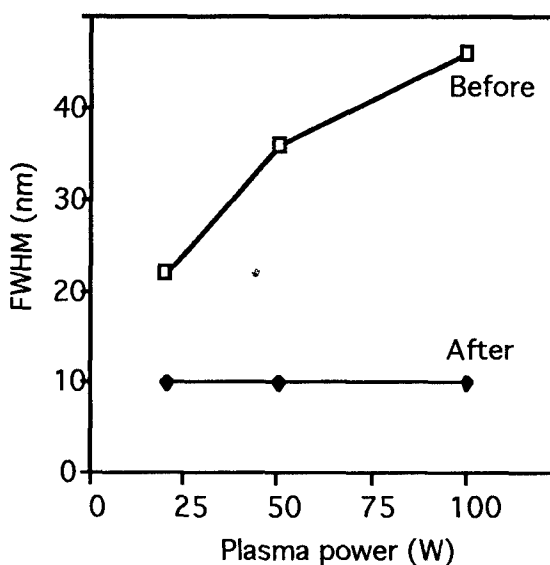
Fig. 2 The full width half maximum of the PL peak from quatum well 3 before and after annealing as a function of the plasma power.

579

at 100 W etching power.

The effect of post etch annealing is to recover the PL signal from all the wells for the sample etched with a power of 20 W. At an etching power of 50 W, the PL signal of the top well does not completely recover and, at 100 W, the PL signal from the uppermost well is completely missing and that from the second top well shows a reduced intensity. Under these etching conditions only about 190 Å of the top layer was removed, consequently the first well is far from being removed, it is still more than 100 Å below the surface. The failure to recover the PL signal suggests that extended defects have been formed in the sample which are not eliminated by annealing. The width of the photoluminescence of the peaks reduces on annealing. There is also evidence of a blue shift in the PL signal, particularly at the highest etch power. This indicates that the point defects generated during the etching are propagating through the samples during the annealing stage, and causing intermixing of the wells and barriers. As expected the point defects are highly mobile and propagate deep into the structure; consequently there is a significant blue shift even in the deepest well for the sample etched at 100 W.

The depth of the residual damage after annealing as a function of plasma power is plotted in Fig. 3; it can be seen that for the lower powers the damage is confined to a region close to the surface, the depth of the damage is estimated to be 300 Å or less, indicating that these plasma powers followed by the anneal should be a good process for device fabrication.
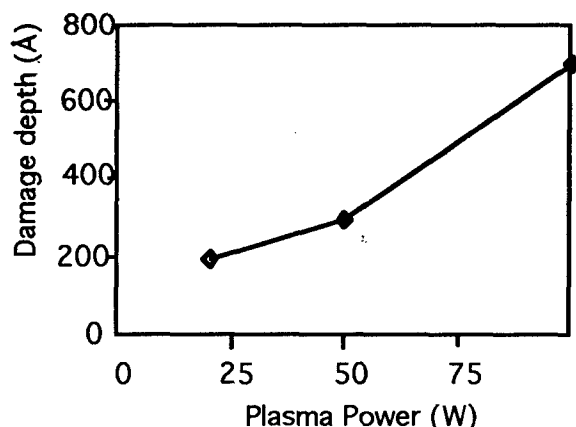
Fig.3 The damage depth as function of the plasma power.

Fig. 4 shows the light-current characteristics for lasers etched by the RIE process using 50 W plasma power then annealed at 500 °C for 60 s. The

annealing will also remove any hydrogen which may have diffused into the structure during the etching (2,3), hydrogen is known to passivate acceptors therefore it is desirable to remove it from electrically active devices. Also shown are the characteristics for lasers which have been fabricated using wet etching. It can be seen that both lasers have very similar threshold currents, 43 mA for the wet etched lasers and 45 mA for the dry etched lasers, and similar differential quantum efficiencies, which suggest that the residual damage left after dry etching and annealing is sufficiently low that it does not affect the laser performance. Lasers which have been etched with a plasma power of 100 W and not annealed did not lase.
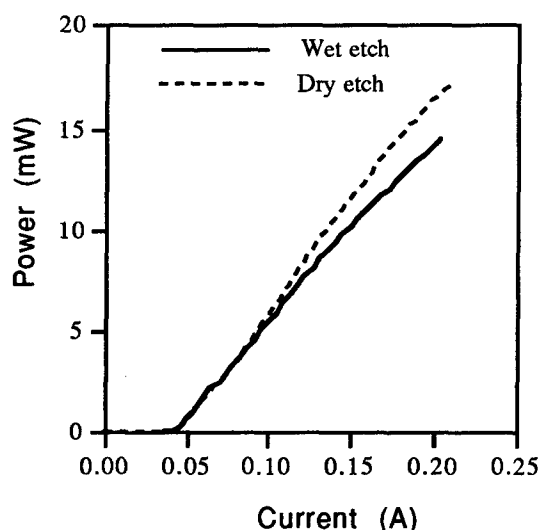
Fig. 4 The light current characteristics of wet etched and dry etched lasers.

IV. Conclusions

The depth of the damage introduced by CH_4/H_2 reactive ion etching as a function of plasma power was measured. It was found to lie in the range 300 Å to 700 Å when the etching power was varied from 20 W to 100 W. A post etch anneal at 500 °C for 60 s removed most of the damage, during this process point defects propagated into the epilayer causing quantum well intermixing in the deeper wells. Comparison of the characteristics of InGaAs/InGaAsP multi-quantum well lasers fabricated by the RIE process with lasers fabricated using wet etching showed that the damage does not significantly affect the laser qualities provided a

580

relatively low power etch process and post-dry-etch annealing are used.

V. Acknowledgements

VI. References

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Surface Damage in GaInAsP/InP Wire Structures
by Cl₂/H₂-ECR Dry Etching

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Abstract   We investigated photoluminescence (PL) intensity dependence on the width of GaInAsP/InP wire structures, which were fabricated by an electron cyclotron resonance dry etching (ECR-dry etching) using a mixture of Cl₂/H₂ (small amount of H₂ gas is mixed with Cl₂ gas) as the etching gases. As the result, a reduction of surface damage in GaInAsP/InP wire structures was observed. The S•τ product, where S is sidewall recombination velocity and τ is the carrier lifetime of the wire structures fabricated using Cl₂/H₂-dry etching and Cl₂-dry etching were estimated to be 92nm and 130nm, respectively, under an excitation power of approximately 100W/cm² (YAG laser, λ=1.06mm) at 296K.

1. Introduction

Low-dimensional quantum-well structures such as Quantum-Wire (Q-Wire) and Quantum-Box (Q-Box) structures have been studied for their high performance and their applications to photonic and optoelectronic devices[1-3].

Until now, a lot of works have been performed to fabricate Q-Wire and Q-Box structures using dry etching process[4-7]. Low-damage dry etching is one of the key technology to realize multiple-Q-Wire (MQ-Wire) and multiple-Q-Box (MQ-Box) laser structures. An electron cyclotron resonance reactive ion beam etching using Cl₂ gas (Cl₂-ECR-RIBE) is considered to be one of the most effective method to fabricate high density and high uniformity MQ-Wire and MQ-Box structures[8].

In our previous study, low-damage and vertical dry etching was achieved using Cl₂ gas for low ion extraction voltage and at low pressure condition[7].

Recently, G. A. Vawter and C. I. H. Ashby have realized smooth InP etching using Cl₂+H₂ gas mixture, when compared with the pure Cl₂ gas[9].

In this work, we estimated the sidewall recombination velocity of GaInAsP/InP wire structures fabricated by Cl₂/H₂-, Cl₂-ECR-dry etching and wet chemical etching. The S•τ product, where S is sidewall recombination velocity and τ is the carrier lifetime of the wire structures fabricated using Cl₂/H₂-dry etching and Cl₂-dry etching were 92nm and 140nm, respectively, under an excitation

power of approximately 100W/cm² (YAG laser, λ=1.06mm) at 296K.

2. Etching Condition

Figure 1 shows the schematic diagram of ultra-high vacuum ECR-dry etching system used in this work. This dry etching system consists of a load lock section, an etching section and a plasma section. The ion extraction voltage V_{ex}, the substrate voltage V_s and sample temperature T_{sub} can be controlled up to 500V, ±500V and 600°C, respectively. We used Cl₂ and H₂ gas as an etching gases.

In our previous study, we obtained good results for V_{ex} = 0V and V_s = 0∼-50V using pure Cl₂ gas(1.0sccm)[6,7]. In order to achieve low-damage dry etching, it is necessary to decrease the ion extraction voltage as well as substrate voltage. In addition, the
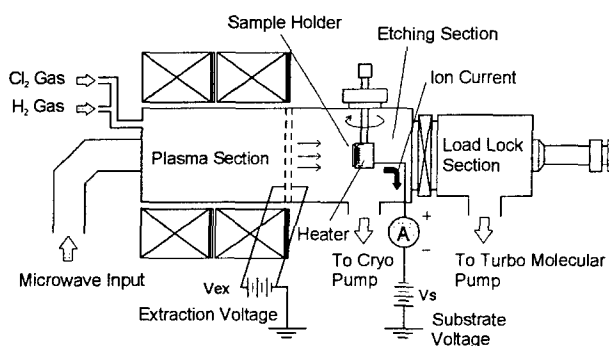
Fig. 1 ECR-dry etching system.

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background pressure should be around $5 \sim 8 \times 10^{-6}$ Torr to increase the mean-free path of ions and radicals to achieve vertical etching. The sample temperature was 300°C.

In this work, we used the mixture of Cl_2/H_2 (a mixture of $Cl_2:H_2=1.0:0.4$sccm) as etching gases and etching conditions are shown in Table.1.

Table 1 Cl_2/H_2-dry etching conditions

Etching Gas	Cl_2/H_2
Micro Wave Power	300W
Gas Flow Rate	1.0/0.4sccm
Pressure	8×10^{-6}Torr
Ion Extraction Voltage	0V
Substrate Voltage	-50V
Sample Temperature	300°C

3. Fabrication Process

Figure 2 shows an outline of the fabrication process. First, we prepared single-quantum-film (SQ-Film) wafers. The wafer consisted of p-InP buffer layer (1μm thick), i-GaInAsP step-index optical confinement layer (OCL) (200nm thick, $\lambda_g=1.2$μm), lattice-matched i-GaInAsP SQ-Film layer (10nm thick, $\lambda_g=1.48$μm), i-GaInAsP barrier layer (10nm thick, $\lambda_g=1.2$μm), and a thin i-InP top layer (5nm thick) were successively grown on the (100) p-InP substrate by low-pressure organometallic vapor phase epitaxy (LP-OMVPE). Then a 20nm thick SiO_2 layer was deposited by thermal chemical vapor deposition (CVD) and stripe masks for various wire widths pattern were formed along the $\langle 01\bar{1}\rangle$ direction on the same wafer using electron beam lithography (ZEP520 resist) followed by CF_4 reactive ion etching (RIE). A periodic SiO_2 stripe mask pattern with a certain width was formed within an 44μm×4mm and formed with separation of 300μm. After removing ZEP520 resist using an OMR resist remover 502A at 200°C for 3min and three samples were cleaved from the same wafer as shown in Fig.2. One of the sample was subjected to Cl_2-ECR-dry etching, where etching conditions were similar to previously reported (1.0sccm Cl_2 gas, V_s= -50V, T_{sub}= 300°C, 2min)[7], and etching depth was about 80nm. The second sample was subjected to Cl_2/H_2-ECR-dry etching (a mixture of $Cl_2:H_2=1.0:0.4$sccm, 2min), where etching conditions where shown in Table 1, and etching depth was about 80nm. For comparison, the other sample was subjected to wet chemical etching using

1) 1st OMVPE

2) EB Lithography and CF_4-RIE

3) Dry Etching and Wet Etching
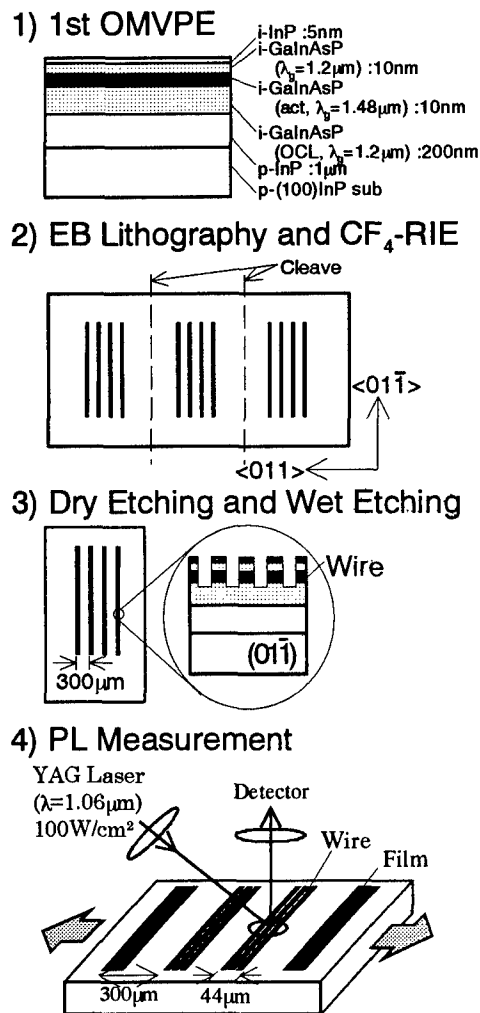
4) PL Measurement

Fig. 2 Fabrication process of wire structures.

a) Dry etched wire structute.

b) Wet etched wire structute.
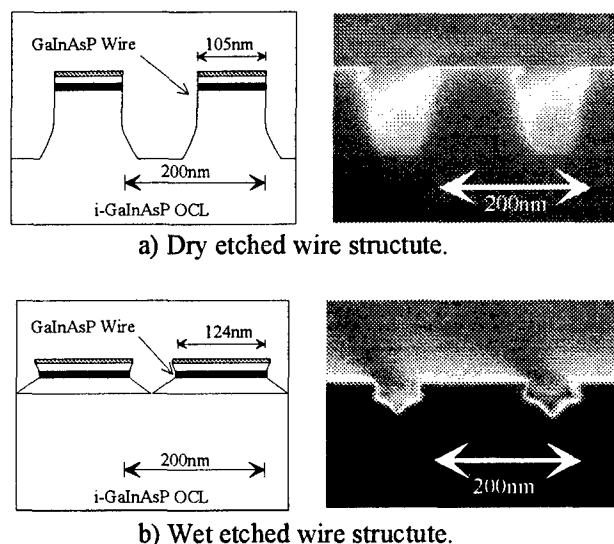
Fig.3 SEM views of the 200nm period wire structures fabricated by dry etching and wet etching.

583

Br-methanol and H_2SO_4-based etchant[3]. After removing the SiO_2 mask using 7%-BHF, the PL measurement were carried out. Figure 3 shows the cross sectional SEM views of 200nm period wire structures fabricated by the dry etching and the wet etching process.

4. PL Measurement

The PL measurement for three samples were carried out. In case of dry etched samples, the PL measurements were carried for two times, before cleaning and after cleaning process. The cleaning process was done using extremely slow rate wet chemical etchant $H_2SO_4:H_2O_2:H_2O$ =1:1:40 at $0°C$ for 20secs (etched depth 2nm)[7]. The PL measurement was performed under an excitation power of $100W/cm^2$ (YAG laser, $\lambda=1.06\mu m$) at 296K. Figure 4 shows the PL spectra for the 200nm period wire structures fabricated by the dry etching and the wet etching process. Figure 5 shows the wire width dependence on the PL intensity normalized by the space filling factor. As can be seen in Fig.5, the PL intensity of the samples fabricated by Cl_2/H_2-dry etching were higher than those fabricated by Cl_2-dry etching.

From the measured normalized PL intensity, we estimated the $S \cdot \tau$ product and W_d using the eq.(1) by least square fitting method[4].

$$\frac{I_{wire}}{I_{film}} = \frac{1}{1 + \dfrac{2 \cdot S \cdot \tau}{W - 2W_d}} \qquad (1)$$

where I_{wire}, I_{film}, W, and W_d denotes the PL intensity of Wire structure, the original Q-Film structure, the geometrical wire width and the width of the dead layer, respectively.

The estimated $S \cdot \tau$ product for the wire structures fabricated using Cl_2/H_2-dry etching, Cl_2-dry etching and wet etching were 130nm, 200nm, and 62nm at 296K, respectively. We found the value of $S \cdot \tau$ product of dry etched sample was reduced due to mixing of small amount of H_2 gas with Cl_2 gas. The estimated W_d for Cl_2-dry etching and wet etching were 0nm and 2nm, respectively. As can be seen, the dead layer thickness of Cl_2-dry etching was estimated to be lesser than 5nm.

Figure 6 shows the wire width dependence on the PL intensity after cleaning the samples using extremely slow rate wet chemical etchant $H_2SO_4:H_2O_2:H_2O$ =1:1:40 at $0°C$ for 20secs (etched depth 2nm). The estimated $S \cdot \tau$ product for the wire
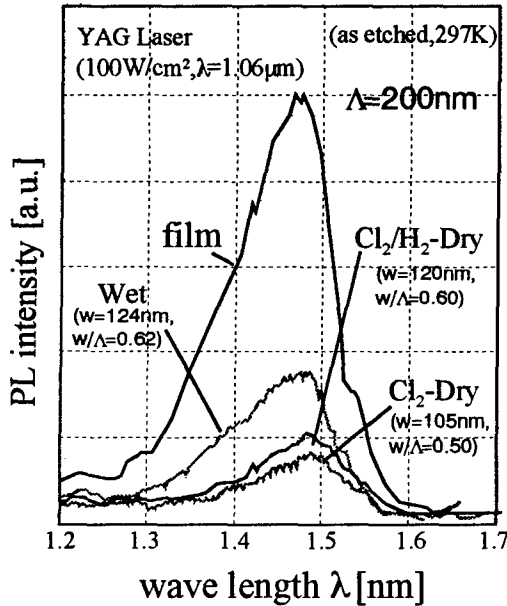
Fig.4 PL spectra for the 200nm period wire structures fabricated by dry etching and wet etching.
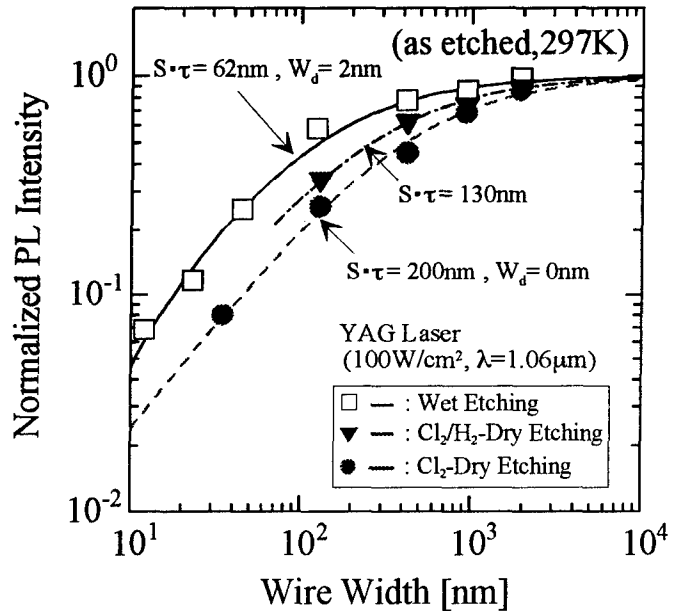
Fig.5 Normalized PL intensity of wire structures as a function of wire width (as etched samples).

584

structures fabricated using Cl_2/H_2-dry etching and Cl_2-dry etching were 92nm and 140nm at 296K, respectively.
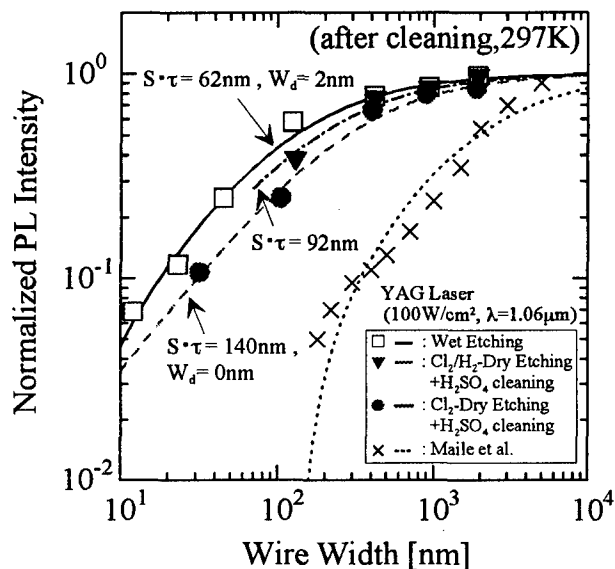
Fig.6 Normalized PL intensity of wire structures as a function of wire width (after cleaning).

Conclusion

We investigated PL intensity dependence on the width of GaInAsP/InP wire structures, which were fabricated using the Cl_2/H_2-ECR-dry etching (a mixture of $Cl_2:H_2=1.0:0.4sccm$) and the Cl_2-ECR-dry etching (1.0sccm Cl_2 gas) process and compared them. The estimated S • τ product for the wire structures fabricated using Cl_2/H_2-dry etching and Cl_2-dry etching were 92nm and 140nm at 296K (after cleaning the samples), respectively. The estimated dead layer thickness W_d, in case of Cl_2-dry etching was lesser than 5nm.

We found the value of S • τ product of dry etched sample was reduced due to mixing of small amount of H_2 gas with Cl_2 gas.

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WET THERMAL OXIDATION OF AlInAs AND AlAsSb ALLOYS LATTICE-MATCHED TO InP

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Abstract

The wet thermal oxidation of AlAsSb and AlInAs lattice-matched to InP is investigated. The oxidation kinetics is determined as a function of temperature and oxidation duration for both materials. The Al content in the material is found to modify the kinetics : the higher it is, the lower the oxidation temperature can be used. Both oxides are characterised by optical and electronic microscopy, by SIMS and by X-Rays diffraction. High oxidation selectivity towards the other materials is obtained with AlAsSb. However, an interfacial layer, composed of pure Sb and As and textured on InP, is forming during the oxidation process. On the opposite, during the AlInAs oxidation, such interfacial layer do not form but the oxidation selectivity is not so good. Finally, the electrical characteristics of the AlAsSb oxide are determined.

I. Introduction

The wet thermal oxidation of $Al_xGa_{1-x}As$ alloys has successfully been employed in Vertical Cavity Surface Emitting Light (VCSEL) technology for lowering the threshold current and applied voltage. This method, issued from Dallessasse et al. work [1], consists in partially oxidizing an $Al_xGa_{1-x}As$ layer with a high Al content, located between the active layers and the upper Bragg mirror. The oxidation of these materials is now well controlled and several labs are currently using this technique [2,3]. However, it deals only with materials lattice-matched to GaAs whereas today, much attention is given to VCSEL grown on InP substrates. Thus, it looks interesting to transfer this technology to materials lattice-matched to InP. AlInAs and AlAsSb alloys, containing respectively 48% and 100% of Al as element III species are good candidates for oxidation. In this paper, we investigate the wet thermal oxidation of these two materials. Temperature and time dependence of the oxidation rate are established for both materials. Oxide characteristics are also determined and we conclude on the opportunity to use AlInAs or AlAsSb oxide as confinement layers for VCSEL applications.

II. Experimental procedure

The AlAsSb samples are grown by molecular beam epitaxy (MBE). They are composed of a GaAsSb / AlAsSb / GaAsSb double heterostructure grown on InP substrate. Two AlAsSb thicknesses have been tested (500 Å and 15000 Å).Mesas are defined by square area (330x330 μm²) Si_3N_4 mask aligned along both [110] and [1 $\bar{1}$ 0] directions, with a H_2SO_4 : H_2O_2 : H_2O based solution in order to expose the lateral part of the AlAsSb layer to the oxidizing flow. The AlInAs samples (5000 Å thick) are grown by Organo Metallic Vapour Phase Epitaxy (EPVOM) on InP wafers. Square areas of Si_3N_4 mask are deposited. Some of the samples are introduced in the furnace such as (technology B). The other samples are processed with a H_3PO_4 : H_2O_2 : H_2O based solution for mesas etching (technology A) (See Fig.2). The oxidation is carried out in an horizontal quartz tube placed in a furnace. The furnace, heated in the range 300 - 600 °C is supplied with N_2 bubbled water held at 80°C. The line between the bubbler and the furnace is heated at 60 °C and an N_2 flow can be added to prevent condensation. The N_2 flow is regulated by a mass flow controller which is fixed at 0.8 l/mn during all the experiments. We investigate the oxidation kinetics through the oxidation time (t) and the furnace temperature (T).

After oxidation, the samples are characterised by optical and electronic microscopy, by X-Rays diffraction and by Secondary Ion Mass Spectrometry (SIMS). SIMS measurements are carried out under 6.5 kV Cs^+ bombardment and the secondary detected ions are positive and associated with Cs. For simplification, the radical Cs^+ does not appear in the text and the figures.

III. Temperature dependence of the lateral oxidation

Figure 1 reports the temperature dependence of AlInAs and AlAsSb lateral oxidation depth which is determined with optical or electronic microscopy. It is compared to AlAs data from ref [4]. The oxidation duration was 20 mn for AlAsSb. In the case of AlInAs and AlAs, the data were extrapolated to 20 mn using a linear law. This is justified for AlAs in that temperature range in ref [4] and for AlInAs as shown next.
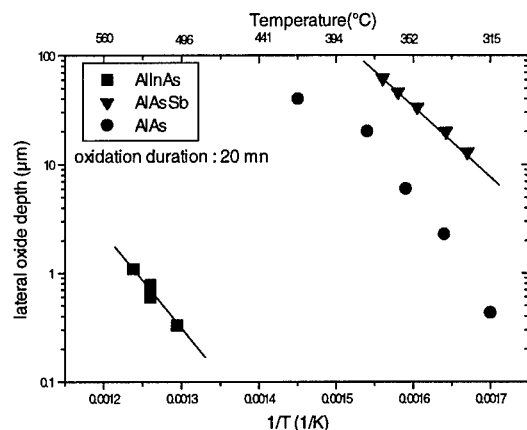
Fig.1 : Temperature dependence of AlInAs and AlAsSb oxidation. Data from ref. 4 are reported for comparison with AlAs oxidation.

An Arrhenius dependence is found for both materials. The AlAsSb oxidation rate is very high (depth of about 30 μm for 20 mn at 350°C). There is quite no influence of the initial thickness layer on the oxidation rate. The AlAs oxidation rate is slower than that of AlAsSb despite the same Al concentration in both materials. Concerning the AlInAs oxidation rate, it is low even at high oxidation temperatures (around 2 μm/h at 520°C). This lower value (compared to AlAsSb) is related to the lower Al amount in AlInAs and the selectivity of the oxidation towards Al composition. As is reported by Nickel [5] for $Al_xGa_{1-x}As$ oxidation with $0.48 < x < 0.8$, we notice an increase of the activation energy for the lower Al content alloy (1.8 eV for AlInAs oxidation) as compared to the higher Al content alloy (1.2 eV for AlAsSb oxidation). Although it is relatively slow, the oxidation rate of AlInAs looks compatible with VCSEL applications. Indeed, Takenouchi et al. have used this material to obtain an oxide/InP Bragg Mirror [6] from AlInAs/InP stacks. However, oxidation temperature higher than 500°C may induce thermal degradation of the material. To work this out, we tested two different technologies as depicted in figure 2 (technology A - technology B) and we examined, with scanning electron microscopy (SEM), the effects of an oxidation performed at 520 °C.

In case A, mesas are defined by etching. Thus, lateral AlInAs surface and InP wafer surface are exposed to the oxidizing flow. After oxidation, a dense dendritic front appears at the border of the mesas (Fig 2.a). The analysis of these dendrites by Transmission Electron Microscopy (TEM) reveals that In and P atoms from the wafer react with O to form $In(PO_4)$ polycristal. Thus, approach B is preferable since the InP substrate is not exposed to the oxidizing flow and no thermal degradation is observed after oxidation (Fig. 2b).
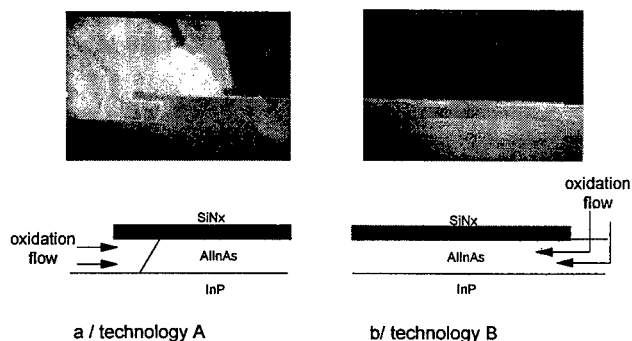
Fig. 2 : Comparison of the thermal degradation induced by AlInAs oxidation at 520°C for two different technologies.

In both approaches, the oxidation rate is quite similar and the oxide penetration is homogeneous and isotrope along [011] and [0$\overline{1}$1].

IV. Time dependence of the lateral oxidation

We now examine the time dependence of oxidation of AlInAs and AlAsSb, performed respectively at 520°C and 350°C (Figure 3).
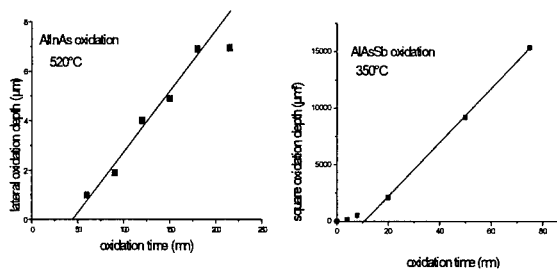
Fig.3 : Time dependence of the oxidation depth for both AlInAs and AlAsSb alloys.

For oxidation time higher than 10 mn, a square root variation is found for AlAsSb oxidation while it is linear for AlInAs. An accurate law has been established for AlAsSb oxidation which allows to calculate the lateral oxidation depth at any temperature and oxidation time[7]. We notice that an initialisation time is necessary before the lateral AlInAs oxidation starts. This time is a little bit higher than for AlInAs surface oxidation. Indeed, a preliminary surface oxidation of the exposed AlInAs layer occurs before the lateral oxidation starts.

587

IV. Oxide characterisation

IV.A Structural characteristics

Both oxides are stable and the oxidation front is abrupt. The non oxidized part of the AlInAs layer preserves its initial crystalline structure.

Concerning the AlAsSb oxidation, an interfacial crystallised (Sb,As) layer , textured on (100) is forming either above or below the oxide (Figure 4). This induces a swelling of the structure of about 15 % which also induces strains. SIMS profile at the interface reveals that this additional layer is composed mostly of Sb plus some As. The SIMS analysis also reveals that the Sb and As levels into the oxide are very low. At temperature around 350°C, the oxidation occurs only in AlAsSb material whereas GaAsSb keeps its initial characteristics. This confirms the high selectivity of the oxidation towards Al content. The accumulation of Sb is due to the low vapour pressure of this metal and its oxides at the oxidation temperature[8, 7].

a

b
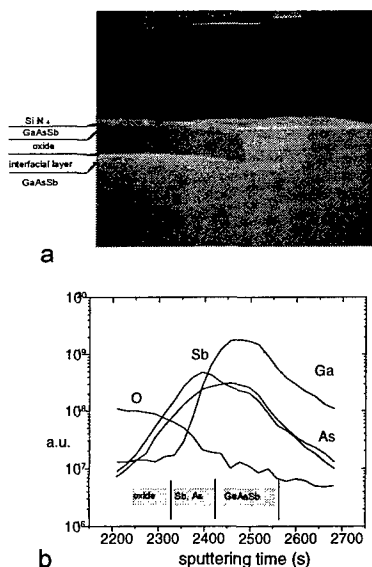
Fig. 4 : SEM (a) and SIMS (b) characterisation of the interfacial layer which is formed during AlAsSb oxidation

On the opposite, concerning AlInAs lateral oxidation, TEM analysis reveals that the oxide is essentially composed of amorphous Al oxide and polycrystalline In oxide. There is essentially no residual As in the oxidized part and no interfacial layer has been formed during oxidation. In that case, as in the case of AlGaAs, pure As as well as its oxides have high vapour pressures at the oxidation temperature and may out diffused efficiently $(P_{As2O3}$ (520°C) > 1 bar). As a result, we do not observe a swelling after the oxidation but a small contraction. It is interesting to note that the contraction is lower for lateral oxidation (10%) than for surface oxidation (30%). In the first case, Al and In oxides are homogeneously mixed while in the second case, the two

phases are separated. Finally, TEM observations reveal that the O diffusion for lateral oxidation occurs at the interface with the substrate (the upper part of the layer is less oxidized than the lower part) and that, even with the technology B, the InP wafer is oxidized at the interface into $InPO_4$. This layer is inhomogeneous and its thickness reaches several thousand Angstroms.

IV.B Electrical characteristics

The electrical characteristics of the AlAsSb oxide have been determined. A Metal Oxide Semiconductor structure has been tested with a 600 Å oxide thickness. The contact surface was 350x350 μm^2. The I-V curve is reported on Fig. 5.
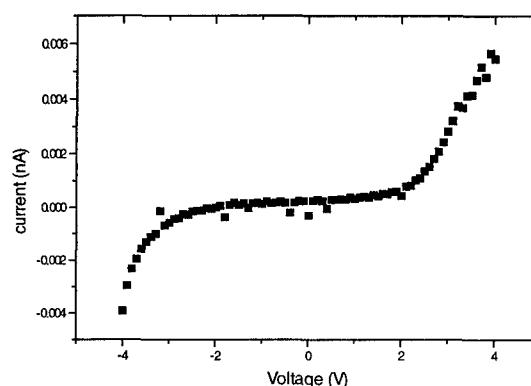
Fig.5 : I-V characteristic of the AlAsSb oxide

From that plot, we calculate an oxide resistivity of $1.4 \ 10^{15}$ $\Omega.cm^2$. This value is quite similar to that of alumine which confirms that the oxide phase is close to Al_2O_3. The critical field at 1 nA/cm² is 450 kV/cm and is sufficient for VCSEL applications.

Conclusion

We have investigated the wet thermal oxidation of both AlInAs and AlAsSb materials and the oxides have been characterised. Under 520°C, the oxidation rate of AlInAs is too low to be usable for VCSEL applications. However, at this temperature, InP also oxidizes and we demonstrated that the InP degradation could be minimised by using a specific technology. On the opposite, AlAsSb is oxidizing at low temperature with high rates. The oxidation selectivity towards the other III-V materials is high and compatible with VCSEL applications. Moreover, we demonstrated that the oxide is highly resistive and owns properties for an efficient electrical confinement. However, the negative effects of the interfacial layer on the confinement remain unknown.

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SILICON SHADOW-MASKED MOVPE FOR InP-BASED THICKNESS-TAPERED GUIDED-WAVE DEVICES

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Introduction

A new fabrication method of high-quality thickness-tapered semiconductor waveguides is proposed based on controlling in-plane thickness during MOVPE by using a comb-shaped silicon shadow mask. Combining a thickness-tapered InGaAsP strained multiple-quantum-well and a flared ridge-waveguide structure resulted in high power (>20 mW) and narrow beam (< 13°) operation over a wide-temperature-range up to 85°C in an InGaAsP/InP 1.3-μm diode laser, which makes this technique attractive for future use in fabricating lightsources for subscriber fiber communications.

I. Background

In-plane thickness-control epitaxy has become a key to achieve semiconductor photonic integrated devices. The techniques so far reported are based on selective-area growth (SAG) on dielectric masked substrates [1-3], shadow-mask growth with epitaxial shadow masks (Epi-SMG) [4], or selective-area etching [5]. This paper reports a new, simple method for growing high-quality thickness-tapered waveguides by shadow-mask growth during MOVPE using a comb-shaped silicon shadow mask (Si-SMG) [6,7]. The technique is useful for fabricating mode-size converter-integrated devices, which will be essential for low-cost optical component assemblies [8,9].

II. Experiment

Figure 1 shows a photograph and a conceptional view showing how the in-plane thickness is controlled in the Si-SMG technique. Prior to the growth, a comb-shaped shadow mask was fabricated from a 200-μm-thick (100) silicon (Si) substrate using standard Si-LSI technology combined with wet etching of the Si to form a through hole. The entire surface of

the shadow mask was then coated with a silicon-dioxide (SiO2) film by thermal oxidization. As shown in the figure, the cross-section of the comb portion had a reversed-trapezoid shape with (111) facet sidewalls. By controlling the top widths of the shadow masks, we can design the thickness tapering. Here, the top and bottom widths were 280 and 20 μm, respectively. The pitch of the comb strips was 1600 μm. After putting this shadow mask on a 2-inch (100) n-type InP substrate, we performed low-pressure MOVPE under our standard growth conditions (600℃, 40 Torr) to form a partly-thickness-tapered 1.3-μm-wavelength strained InGaAsP-MQW structure. The direction of the comb stripes was adjusted to [01-1] of the InP substrate by using a specially designed wafer holder. The gap width between the bottom of the shadow mask and the surface of the InP substrate was typically 20 μm. The layer structure consists of an n-InP buffer layer, the MQW layer, and a thin p-InP cladding layer. The MQW layer had five 1.4% compressively-strained InGaAsP wells and 100-nm-thick separate confinement heterostructure (SCH) layers, which was optimized for low-threshold operation under elevated temperatures [10]. After the Si-SMG, the in-plane distributions in the layer thickness and the room-temperature photoluminescence (PL) were evaluated by a surface profiler (DEKTAK III) and a by microscopic PL, respectively.

After the Si-SMG, no polycrystalline nucleation was observed on the shadow masks. Figure 2 shows an SEM view of the tapered MQW crystal. Good surface morphologies in both the flat and tapered sections were observed. The distribution of the total thickness of the

MQW layer (Fig. 3) measured along the [011] direction (perpendicular to the comb stripes) shows that there are smooth thickness transition regions that have an approximately 300-μm-long taper. The taper length seemed to be determined by the diffusion length of the grown species diffused under the shadow masks. A slight thickness enhancement of less than 5% was seen in the regions below the edge of the shadow masks. This enhancement is caused by the SAG mode produced by the SiO2-coated shadow masks. A minimum total thickness of 0.08 μm was obtained under the center portion of the shadow mask, which resulted in a thickness reduction ratio Rg of 6.2. The results of microscopic PL measurements were also shown in Fig. 3. The results confirmed that this thickness reduction was translated into the blue-shift of the PL peak wavelength from 1310 down to 1200 nm. In the flat sections, sufficient PL emission intensities were obtained which were comparable to those of normal growth. This is one of the main advantages of the Si-SMG technique compared to the SAG technique in which crystal deterioration tends to be caused by the associated composition changes when Rg is greater than 2 to 3. In the tapered regions, a slight reduction in the peak-intensities was observed; this slight drop is due to the reduction in the total thickness of the MQW layer.

III. Device applications

The tapered MQW layer was applied in a 1.3-μm-wavelength laser diode with an integrated intra-laser-cavity beam expander (BEX) waveguide (Fig. 4). After removing the shadow mask, the wafer was entirely regrown

by a p-InP cladding layer and a p+-InGaAs contact layer. Then, it was built into a reversed-mesa flared-ridge-waveguide (RM-RWG) structure with buried polyimide to flatten the RWG. The combination of the thickness taper and a flared RWG offers smooth mode field expansion in both vertical and horizontal directions. The flared RWG had a constant lateral neck width of 2 μm in its 400-μm-long uniform section and was tapered up to 7 μm at the output facet. It also had a 300-μm-long constant-thickness MQW monolithically integrated with a 300-μm-long thickness-tapered MQW. The devices were cleaved to a total length of about 600 μm, and the back facet was coated with a high-reflection film. After that, the device was mounted on a SiC heat sink in a junction-up configuration.

Typical temperature dependences (at 25, 70 and 85°C) of the light-current characteristics for our BEX-laser are shown in Fig. 5. The high-quality tapered-MQW active region clearly leads to high lasing performance. The threshold currents of 12 mA at 25°C and 26 mA at 85°C correspond to a very high characteristic temperature of 78 K. Furthermore, the forward current and voltage required for a 10-mW output were only 56 mA and 1.14 V. Figure 6 shows typical far-field patterns (FFPs) at various chip outputs. Gaussian-shaped FFPs were observed with full width at half maximums (FWHM) of 11° and 13° degs. in the lateral and vertical directions, respectively. This narrow beam drastically improved the lens-less fiber coupling. As shown in Fig. 5, a coupling loss of only 1 dB was attained between this BEX-laser and an 8-μm-diameter flat-end dispersion-shifted fiber (DSF) with a 5-μm-gap between the laser and the DSF. A large alignment tolerance of about 2 μm was also confirmed in both directions when the gap was 20 μm.

IV. Conclusion

We have demonstrated a silicon shadow-mask-growth technique that allows high-quality thickness-tapered semiconductor waveguides to be made very easily. Combining a thickness-tapered InGaAsP strained multiple-quantum-well and a flared ridge-waveguide structure resulted in high power (>20 mW) and narrow beam (< 13°) operation, which makes this technique attractive for future use in fabricating lightsources for subscriber fiber communications.

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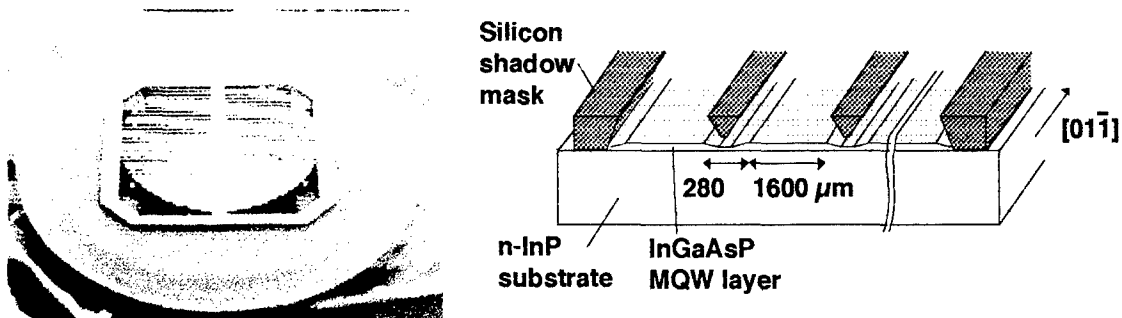
Fig. 1 Photograph and conceptional view of the in-plane thickness-control by the Si-SMG technique
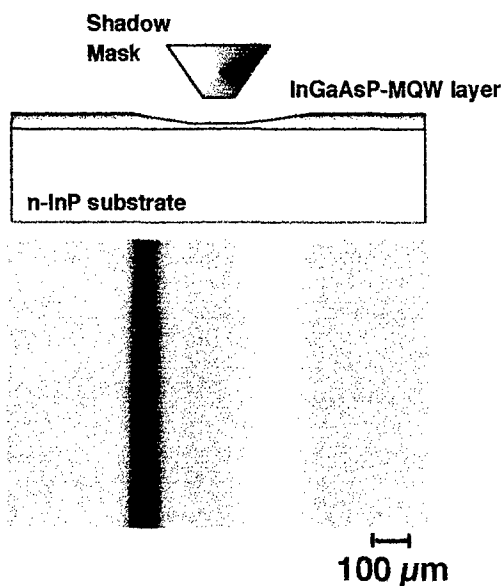
Fig. 2 Surface morphology of the shadow-mask-grown MQW layer adjacent to the masked region
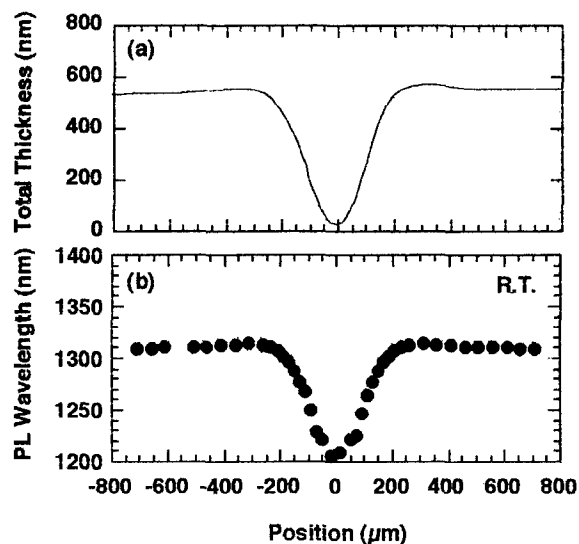
Fig. 3 Distribution of total thickness and PL peak wavelength of MQW layer
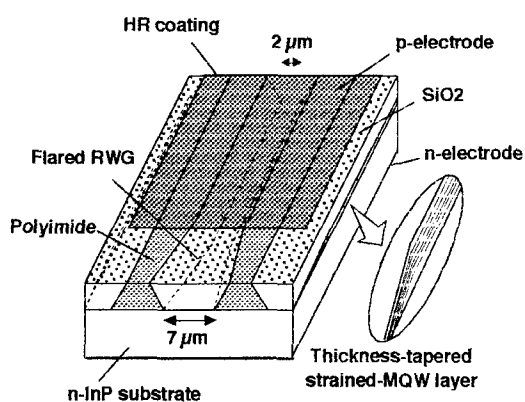
(a) Device structure
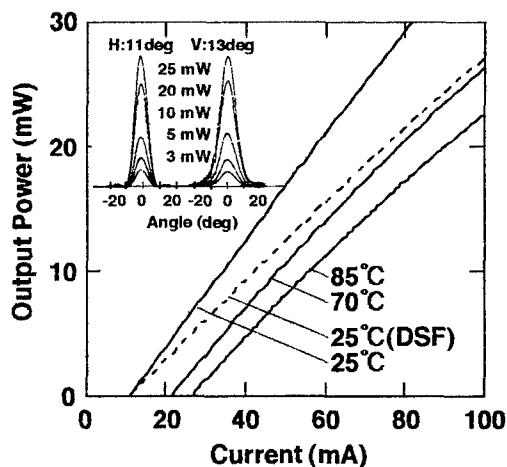
(b) Light-current curves at 25, 70, and 85°C

Fig. 4 Application to a beam expander-integrated laser

STRIPE DIRECTION DEPENDENCE IN SELECTIVE AREA GROWTH OF InGaAsP USING TBP AND TBA

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I. Background

Selective area growth (SAG) of InP and InGaAsP is a promising technology for the realization of photonic integration in which the energy gap and waveguide characteristics are varied along the path of the light. Also, when such structures are grown selectively in narrow (~2 μm) openings between masking materials such as SiN_x or SiO_2, buried heterostructures (BH) can be formed by removing the masking material and overgrowing it with a higher bandgap material. This method has been realized exclusively only on structures oriented along [110] stripe direction.[1,2] The [1$\bar{1}$0] direction has generally been avoided because of the growth of materials over the edge of the masking material, which is believed to deteriorate the structure quality. However, for [110] oriented stripes, low V/III ratios as well as the reduced growth rates are required to minimize the edge growth enhancement caused by the species that have migrated from the adjacent masking material. These conditions are often not the optimum conditions for device quality material and require a significant modification of a growth system optimized for the non-selective epitaxy. In addition, if it can be controlled, the overhang caused by InP growth on the side wall can be used to advantage to protect the InGaAs(P) active region during the device processing after SAG.

In this work, we employ tertiarybutyl-phosphine (TBP) and tertiarybutylarsine (TBA) as phosphorous and arsenic sources, respectively, for SAG of InP and InGaAsP. These sources enable us to maintain a relatively low V/III ratio of ~20 even under reduced pressure (76 Torr) MOCVD growth at 640 °C. With the growth rates which are not extremely low compared to the conventional growth, the growth surface profile by SAG using [110]-stripe is studied and their ultimate limit is presented. Also, the alternative [1$\bar{1}$0] direction is investigated and the control of the growth over the SiN_x adjacent to the selectively opened area is presented. Also, based on the experimental observations, the mechanism leading to the differences in these directions are presented.

II. Growth rate enhancement in InP SAG

The perfect prevention of the growth on SiN_x area causes lateral vapor phase diffusion of sources as well as the surface migration of the source elements decomposed on the masked area. The growth rate enhancement cause by this additional source supply is one of the important characteristics of SAG. Especially, when the opening between SiN_x is as narrow as 1~2 μm, the top surface area decreases as the growth proceeds, and this causes the growth rate change. Figure 1 shows a typical cross sectional scanning electron microscope (SEM) image of InP by SAG with [110]-aligned stripes. Very thin InGaAsP marker layers were inserted between InP layers. For the study of the growth surface evolution, we used 2~2.5 μm opening with 11 μm wide SiN_x masks on either side. The source supply during the growth of this sample corresponds to a growth rate of 2.5 μm/h in normal growth without masked region. We observed that growth rates higher than 4 μm/h at normal condition cause significant amount of edge growth enhancement but, at the reduced growth rate of 2.5 μm/h, the edge growth is prevented completely even at V/III ratios as high as 200. Also, in the [110] direction, there is no growth on {111}B plane until the top surface disappears. After the top surface disappears, the absence of any allowed growth plane causes growth on {111}B plane and even on the SiN_x area.
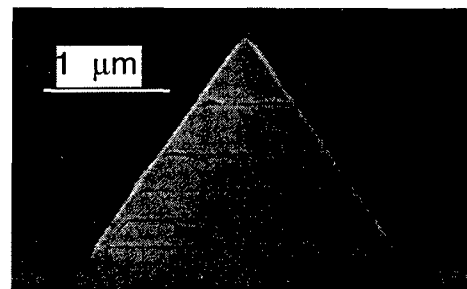
Figure 1. Cross-sectional SEM image for SAG-InP grown with V/III of 30 with normal growth rate of 2.5 μm/h.

In the SAG of InP on openings wider than 5 μm, it was observed that the enhanced growth rate increases linearly with the stripe width until the deposition starts on SiN_x. For narrow openings cases, the growth rate variation during the SAG makes this conclusion meaningless. However, by measuring the thickness of the first InP layer in Fig. 1, the growth rate at the first stage of SAG can be compared. In this measurement, the growth rate is observed to increase as V/III ratio decreases. Figure 2 shows the growth rate enhancements of each layer as functions of V/III ratio. For normal growth, we could not observe the growth rate variation in this range of V/III ratio. This growth rate difference is believed to come from the enhancement of the lateral vapor phase diffusion by reduced amount of TBP. The drastic change in the second

layer growth rate at lower V/III is the result of the decreased top surface area after the first layer growth.
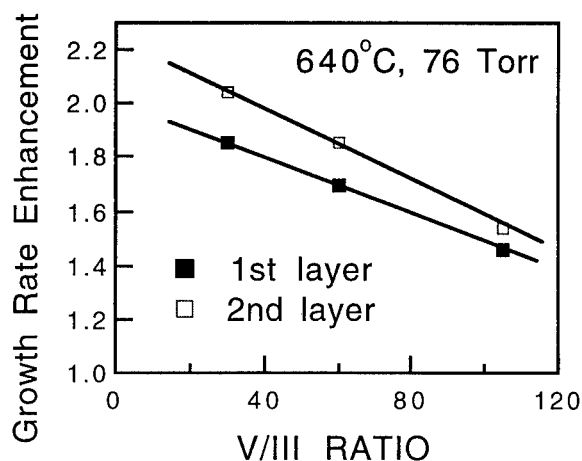
Figure 2. V/III ratio dependence of the InP growth rate enhancement with stripe along [110].

For the [1$\bar{1}$0] direction, we found the growth on {111}A plane causes overhang around the edge of the selectively grown area in the sample prepared simultaneously with the one shown in Figure 1. Also, the growth rate of the second layer is almost the same as the first layer. However, from various growths performed with different thicknesses for the first layer before the InGaAsP marker growth, it was found that this overhang growth starts only after the InGaAs(P) growth. This means that, on the {111}A plane covered with InGaAsP, the non-growth property disappears. Once InP starts to grow on {111}A, its growth rate on this plane becomes comparable to that on {001} plane. Even though InGaAsP slightly covers {111}B plane in [110] direction counterpart too, the non-growth property on {111}B is still preserved. The most significant problem of the overhang growth is the possible covering of SiN$_x$ mask area by overgrown InP, which causes process difficulty in the regrowth for BH formation.

III. Surface flatness in InGaAs(P) growth

For SAG of InGaAsP in a narrow opening, it was observed that the edge growth enhancement due to the surface migrated species is very hard to eliminate. Figure 3 shows the surface profile of InGaAsP layers grown with a normal growth rate of 1.5 µm/h and V/III of 200. The composition of this quaternary under normal growth generates InP-lattice-matched epilayer with photoluminescence (PL) emission wavelength (λ) at 1.2 µm. This composition of InGaAsP is important for the waveguide and quantum well barrier materials for 1.55 µm wavelength light emitting devices. The surface flatness and the material quality of λ=1.2 µm InGaAsP can limit the possible growth conditions for the SAG for optical communication applications. At the relatively high V/III ratio of 200, both [110] and [1$\bar{1}$0]

directions give very nonplanar surface of quaternary layers. In order to minimize the edge growth enhancement, the migration of growth source species on the top of the surface has to be enhanced, and lower growth rate and lower V/III ratio are known to be effective for this.
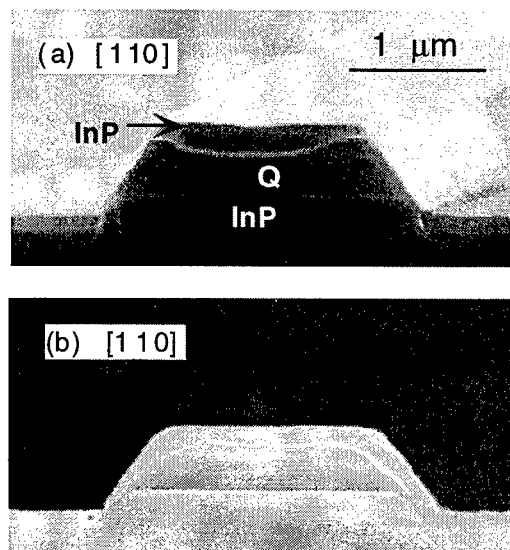
Figure 3. SEM cross-section image for (a) [110] and (b) [1$\bar{1}$0] direction samples grown on 2.5 µm opening between 11 µm masking stripes. For the quaternary growth, V/III = 200 and the growth rate is 1.5 µm/h at normal growth.

An easy way to check the surface migration of the source materials on the growth surface is to observe the growth pattern around the opposite edge of the SiN$_x$ to the narrow opening. Figure 4 shows the SEM image of the samples under various conditions taken at the edge of the 11 µm wide masking SiN$_x$ stripe along [110] direction, and Fig. 4 (c) is the counterpart of Fig. 3 (a). The growth rate and the V/III ratio for the buffer and capping InP layers in each sample are similar to its quaternary growth condition. For the structure grown on narrow opening shown in Fig. 3 (a), it can be seen that the surface of the capping InP layer has a small dip at the center, and this feature can be explained by Fig. 4 (c) which shows that the surface migration during the capping InP layer can make the surface flat only to 0.7 µm. Thus, the flat regions from both sides cannot merge completely at the center of the narrow opening structure in Fig. 3 (a). From these SEM images, it is observed that reductions of the growth rate and the V/III ratio lead to flatter surfaces in SAG. It is very easy to get flat InP surface in this narrow opening of ~2 µm, but the surface migration during the quaternary growth is not fast enough. Instead of trying to reduce the quaternary growth rate further, which would require replacing the mass flow controllers in our MOCVD system optimized for the normal growth of optical device structures,[3] we emphasized reduction of the V/III ratio that was aided by the high decomposition efficiencies of TBP and TBA.[4]

(a) 3 μm/h, V/III = 70

(b) 1.5 μm/h, V/III=70   (c) 1.5 μm/h, V/III=200
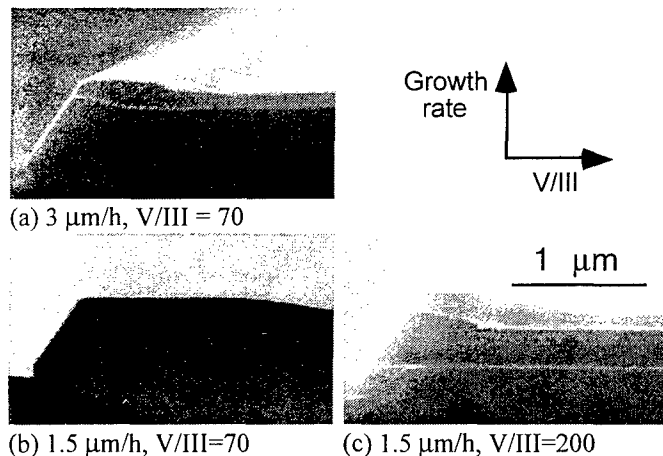
Figure 4. Evolution of surface flatness of InP and InGaAsP (λ=1.2 μm) in terms of normal growth rate and V/III ratio.

In attempts to grow InGaAsP quaternaries under low V/III ratios, several problems were observed. First, the relative incorporation efficiency of As and P changes, so the ratio of TBA/TBP to get 1.2 μm emission has to be changed by more than a factor of two as the V/III ratio is reduced from 200 to 20. Also, if the whole InP/InGaAsP structure is grown at a low V/III ratio of ~20, the surface of InGaAsP becomes rough even on a very flat InP buffer layer. Figure 5 compares the surface of the InGaAsP layers prepared on different buffer InP layers. This result demonstrates that the InP buffer has to be grown at relatively high V/III larger than 50 in order to remove the surface fluctuation of overgrown InGaAsP. This restriction does not cause any problem since the source migration during InP growth is good enough at this V/III ratio. The layers in Fig. 5 were grown by SAG with stripe along [1$\bar{1}$0], but this conclusion is applicable to all the cases including the normal growth.

InP @ V/III = 15	InP @ V/III = 15
Q @ V/III = 20	Q @ V/III = 20
InP @ V/III = 15	InP @ V/III = 70
(a)	(b)
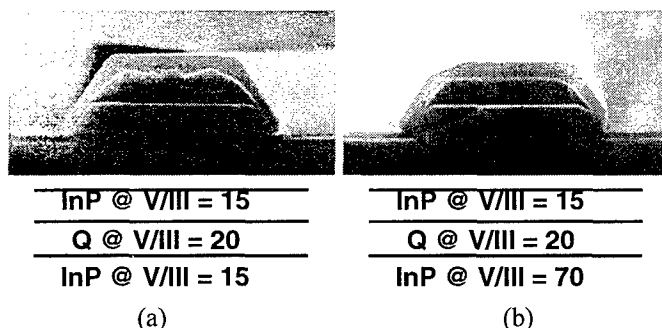
Figure 5. Surface fluctuation of quaternary layers depending on the InP buffer growth

Figure 5 (b) shows a typical cross-sectional view of samples prepared by [1$\bar{1}$0] SAG, which is characterized by the very flat top surface of InGaAsP and the InP coverage over the side walls. For the [1$\bar{1}$0] direction, the surface flatness is no longer a problem if the InGaAsP is grown with V/III less than 100. Also, in Fig. 5 (b), the InP which covers the side wall does not cover the SiN$_X$ mask, which is in sharp

contrast to the features of high V/III=100 InP cap in Fig. 3 (b). We found that the InP cap grown with V/III below 50 does not cover the SiN$_X$ mask.

The capping InP also has to be grown carefully to prevent the As carry-over after the quaternary growth.[5] In order to get rid of the InAsP interfacial layer which can reduce the carrier injection into the active region of the device, an intense TBP purge has to be done during the growth interruption between the quaternary and the capping InP. Figure 6 shows how the elongation of TBP purge time can reduce the lower energy shoulder corresponding InAsP interfacial layer and also improves the luminescence efficiency. The net TBP flow of 10 sccm for 2 seconds is sufficient for the InP cap after the growth of ~0.3 μm thickness of waveguiding InGaAsP with λ=1.2 μm.
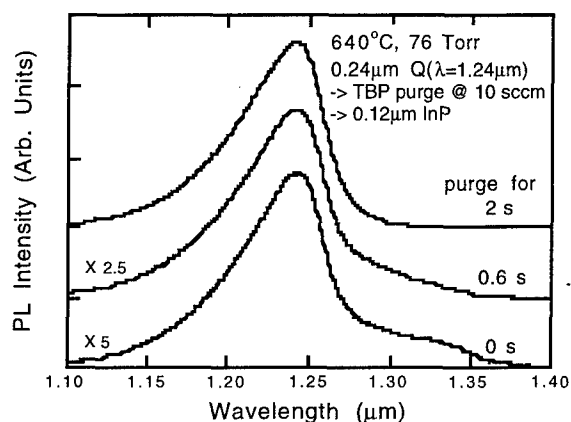
Figure 6. Photoluminescence spectra of InGaAsP layers grown with different TBP purge

High quality InGaAsP with l=1.2 μm cannot be grown with V/III below 20 using TBP and TBA. Figure 7 shows the surface of the InGaAsP layer grown with V/III=15 on optimized InP buffer. The PL spectra from this sample has a very broad peak centered at 1.2 μm. The cross-sectional SEM picture of this sample shows 3 dimensional island growth occurred after ~0.05 μm InGaAsP had been grown. Actually, even though the V/III ratio is 15, the relative amount of TBA compared to the total amount of group III sources is almost one in this case. Thus, the ultimate limit of the lowest V/III for the growth of λ=1.2 μm InGaAsP is turned out to be 20.
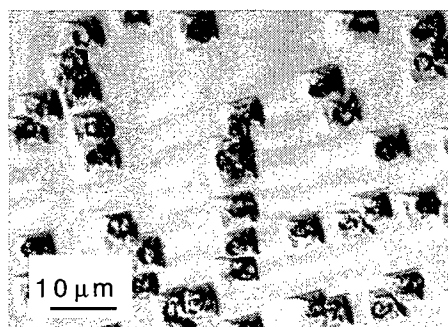
Figure 7. Surface of InGaAsP (λ=1.2 μm) grown with the growth rate of 1.5 μm and V/III=15.

596

Even at this extremely low V/III, the waveguiding InGaAsP layer cannot be grown perfectly flat. Figure 8 (a) shows the best surface flatness that we achieved with a normal growth rate of 1.5 μm/h. For this sample grown at V/III=20, the PL intensity from the normally grown area is only 20 % of that out of the sample grown at V/III=200. We tried another composition of InGaAsP with λ=1.5 μm, and, in this case, V/III can be reduced down to 10. However, it was impossible to get a very flat surface at this composition with the normal growth rate of 1.5 μm/h. Meanwhile, for the growth of InGaAs lattice matched to InP, the surface flatness is much better than even InP. Figure 8 (b) shows the cross-section of the sample grown with V/III=50. From the fact that only InGaAsP gives a strong edge growth enhancement, it is concluded that the strong Ga-P interaction is the major cause of the reduced migration on the top surface in SAG. Therefore, it is concluded that, without reducing the growth rate of InGaAsP substantially, it is very hard to control the surface flatness of InGaAsP-containing structure for [110] SAG.
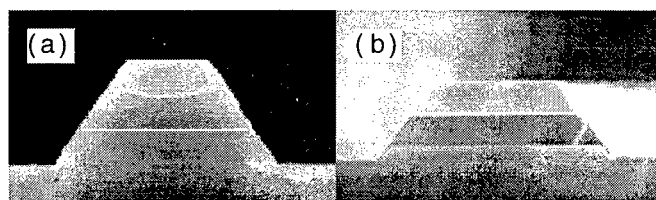
(a) InGaAsP (V/III=20)   (b) InGaAs (V/III=50)

Figure 8. Surface flatness of (a) InGaAsP (λ=1.2 μm) and (b) InGaAs grown by [110] direction SAG.

IV. Stripe direction dependence

It was observed that the growth rate of InGaAsP in [1$\bar{1}$0]-stripe SAG is always less than that of [110] counterpart. The additional growth enhancement in [110] SAG compared to [1$\bar{1}$0] originates from more effective incorporation of the surface-migrated species in the top surface. In the case of [1$\bar{1}$0] SAG, the chemical characteristics of {111}A side wall are believed to prohibit the species originating from the mask area from migrating to the top surface of the structure. This reduced incorporation of surface-migrated species is also a major cause for flat surfaces in [1$\bar{1}$0] SAG.

It is noticeable the growth pattern of InP SAG is significantly changed after InGaAsP growth. Usually, if [110] and [1$\bar{1}$0] stripes with the fixed opening and masking widths are used at the same time in SAG, the height and the shape of buffer InP layers are the same in both directions. Also, from the cross-sectional images of both samples with thick InGaAsP layers, we could observe that a very thin layer of InGaAsP covers the side wall of the buffer InP. This means the non-growth property of {111} plane starts to be disturbed by InGaAs(P) growth. So, after the waveguide layer growth, the side wall of complete SAG structure is covered by InGaAs(P) in both directions. But, the difference in the InP growth on InGaAs(P) side wall causes the major difference in the InP overhang behavior. The non-growth property on

{111}B plane is much better than {111}A. For the buffer layer growth, if the side wall is made of InP itself, both planes give perfect non-growth property. However, once that plane contains As atoms, In-As bonding which has the lowest energy among all possible interactions can cause capture of indium-containing species on the side wall, which triggers the InP growth on the plane. This process is more probable on {111}A plane. This effect leads to the side wall growth in [1$\bar{1}$0] SAG. Once this side wall growth starts, even after the side wall is covered completely by InP, the migration of the species coming from the masked area is disturbed at the boundary between SiN$_X$ and InP by the side wall overhang itself, and this can cause further growth of InP on the side wall. In the case where side wall growth happens, if we reduce the V/III, this enhances the selectivity between SiN$_X$ and InP surface, so the coverage of SiN$_X$ can be avoided. This side wall growth property can be used to protect the active region during the post-growth processing, which makes it much easier to fabricate BH structures.

V. Conclusion

The SAG of InP and InGaAsP by MOCVD using TBP and TBA is investigated, especially by comparing the differences between the structures with the SiN$_X$ stripe aligned along [110] and [1$\bar{1}$0] directions. The way to control the surface flatness of InGaAsP by reduced V/III ratio is studied and the ultimate limitation in [110] SAG with a reasonable growth rate is shown. From [110] and [1$\bar{1}$0] SAG, differences in InGaAsP growth rate on the top surface and InP coverage on the side wall are observed and explained by a model based on the different chemical properties of {111}B and {111}A planes. Based on these results, the advantage of [1$\bar{1}$0] direction is discussed from the view point of device processing.

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DESIGNING THE RELATIVE IMPACT OF THICKNESS/COMPOSITION CHANGES IN SELECTIVE AREA ORGANOMETALLIC EPITAXY FOR MONOLITHIC INTEGRATION APPLICATIONS

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Introduction :

Selective area growth (SAG) study has been performed with atmospheric pressure MOVPE. We have studied growth rate enhancement and composition variation as a function of the mask and opening widths. Two distinct behaviours, depending on the opening width, have been identified. For the opening regions larger than 5 μm an overgrowth occurs near the edge of the mask and the relative variation of III elements in the centre is small and independent of the mask width. On the other hand for the narrow opening regions (<3μm) the growth has a triangular shape with smooth [111] facets. In that case the relative variation of III elements in the centre increases linearly with the mask width. Moreover we have grown a multiquantum well structure laser in a 2 μm opening region. Good material quality and lasers characteristics have been obtained.

Selective area growth (SAG) is a promising approach for monolithic integration technology. These last few years much effort is focused on this approach and various integrations have been successfully realised such as DBR laser [1], laser-modulator [2]. In this technique two parallel ~ 1 mm long dielectric masks are shaped on the substrate prior to the growth. The presence of this dielectric mask changes locally the active concentration in the gas phase, leading to a lateral variation of growth rate and composition. For bulk layers the wavelength shift is only due to the composition variation. In the quantum wells, further to the composition, the growth rate variation introduces an additional wavelength shift. The amount of the both wavelength shifts depends on geometric parameters, namely the mask and the opening width.
The control of wavelength shift either by composition variation or by thickness enhancement is favourable for different applications. For example in the case of laser-taper integration a wavelength shift together with high thickness ratio between laser and tapered regions is required. On the other hand, for laser-guide integration, to ensure sufficient optical confinement and low optical losses in the guide region, only a large wavelength shift is recommended.
For this purpose an experimental study of the growth behaviour in selective area epitaxy has been realised as a function of mask and opening widths (W_m and W_o respectively). This study was supported by computer modelling [3]. The growth was performed by atmospheric pressure MOVPE. We used trimethylindium (TMIn) and trimethylgallium (TMGa) as element III sources, arsine (AsH3) and phosphine (PH3) as element V sources. For the dielectric masks, we used Si_xN_y with typically 120 nm thickness deposited on InP substrates by chemical vapour deposition (CVD). Then, stripe patterns were defined in the dielectric mask by conventional photolithography and reactive ion etching (RIE). The stripes were formed in the [110] direction. For all the samples, the growth rate was kept relatively low (< 1 μm/h) in order to obtain a flat surface and good crystal quality in the opening regions.
The layer thicknesses in the openings $t_{(in)}$ were investigated by SEM and compared with those measured far from the mask $t_{(out)}$. Figure 1 shows the

growth rate enhancement R=t$_{(in)}$/ t$_{(out)}$ in the centre of different opening regions as function of W$_m$/W$_o$.
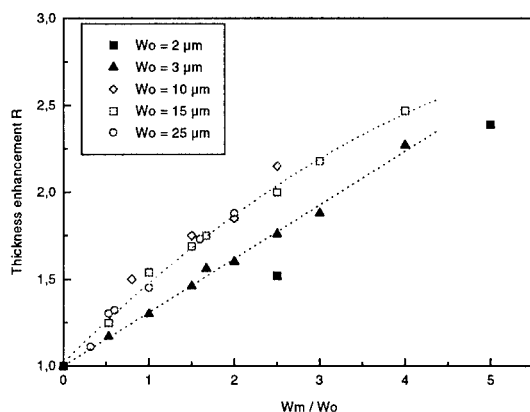
Fig. 1 : Thickness enhancement R=t$_{(in)}$/t$_{(out)}$ in the centre of different opening regions as a function of W$_m$/W$_o$.

At constant W$_m$/W$_o$, the ratio R is nearly the same for openings beyond 5 µm, whereas R decreases for the openings lower than 3 µm. Likewise for the growth shape, the influence of the mask edge is different for narrow and wide openings. For the large gaps a "bowl like" shape is obtained due to the overgrowth near the mask edge. This shape is perfectly simulated with our computer modelling (Figure 2).
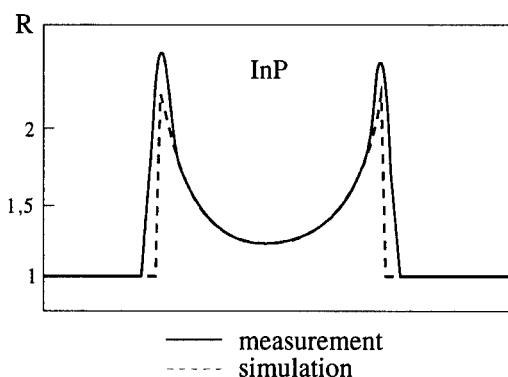
Fig. 2 : Measured and simulated growth shapes for a large gap (W$_o$=40 µm and W$_m$=40 µm).

As shown in this figure the edge effect is very pronounced up to 2or 3 µm from the mask. Consequently, for the multiquantum well structures, the transition band energy near the edges is lower than in the centre. This effect leads to a large loss of the photoluminescence intensity in the centre. To obtain the real value of PL intensity and wavelength a 3 µm mesa has to be etched in the centre of the opening region. In the case of the narrow openings (<3µm), this lateral variation of thickness is negligible. Also, in this

case, the developement of [111] facets dominates the overall mesa shape (Fig. 3).
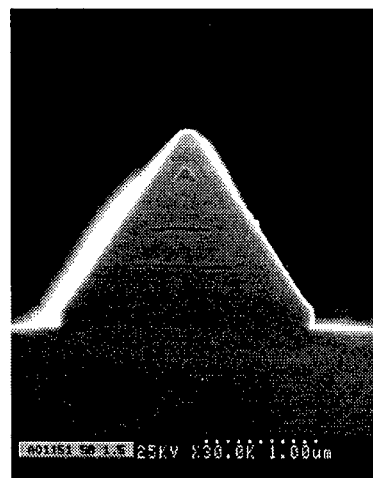
Fig. 3 : Selective growth in a 1.5 µm wide opening (W$_m$=50 µm).

The disadvantage of this triangular form is that the growth rate changes in the growth direction leading to a broad luminescence spectrum in the case of multiquantum well structures. To overcome this problem the active layer should be grown near the mask level where the growth is not affected by facets.

The composition variation in the opening region was investigated quantitatively by energy dispersion X-ray (EDX) microanalysis in TEM spectrocorrected for X-ray absorption.
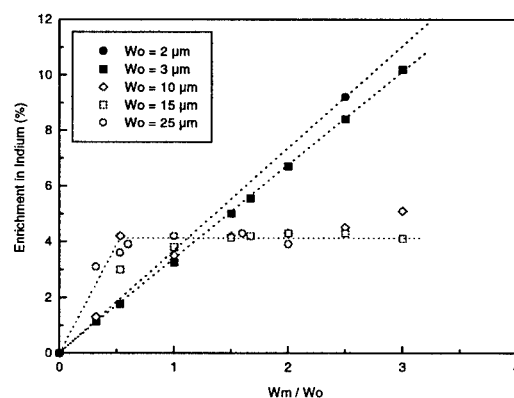
Fig. 4 : Indium enrichment in the centre of the opening region as a function of W$_m$/W$_o$, for different opening widths.

The probe size is between 2 and 5 nm which allowed us to study the composition variation even for openings narrower than 2 µm. The accuracy is of 0.01 and 0.015 for III and V elements respectively.

599

For the openings larger than 5 µm indium enrichment near the mask is observed. This enrichment introduces an additional strain near the mask edge. This effect added to the overgrowth cited above often leads to the apparition of misfit dislocations. In the centre the relative variation of indium compared to the outside far from the mask is independent of the mask width (Fig. 4). On the other hand for openings smaller than 3 µm the composition is uniform over the opening region for different mask widths (Fig. 5) and in the centre the relative variation of composition increases with the mask width (Fig. 4).
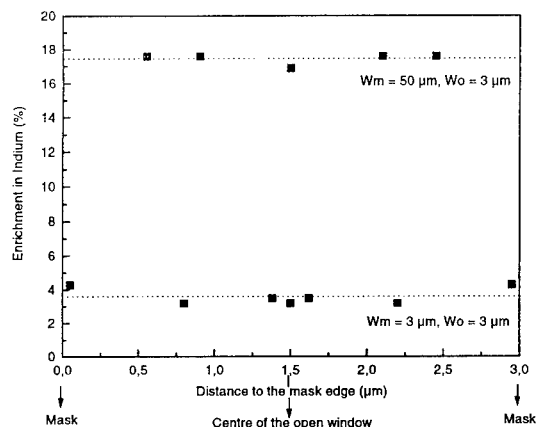
Fig. 5 : Enrichment in Indium across a 3µm wide opening region, for W_m=3 and 50µm.

This difference of behaviour between large and narrow gaps can be attributed to the diffusion lengths of III elements. Indeed, the diffusion length for TMGa (~ 12 µm) is four times higher than that of TMIn (~ 3 µm) [3]. This difference is underlined by the difference of growth rate ratio between InP and GaAs for the narrow gaps (Fig. 6).
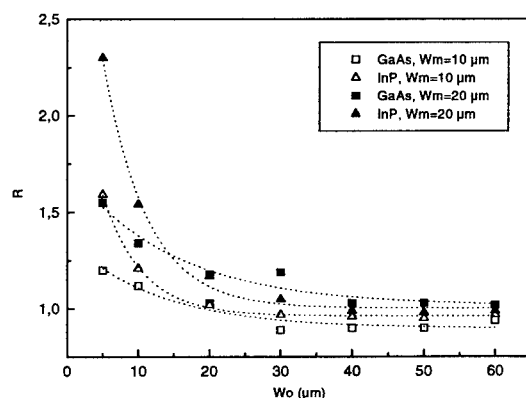
Fig. 6 : InP and GaAs thickness enhancement R in the centre of the opening region as a function of opening width Wo for two mask widths (10 and 20 µm).

To investigate the materials quality and explore the device performance potential with the narrow design, we have grown a structure with 6 lattice matched InGaAsP wells and barriers at 1.55 µm and 1.2 µm respectively. The mask and opening region are 20 and 2 µm wide respectively.
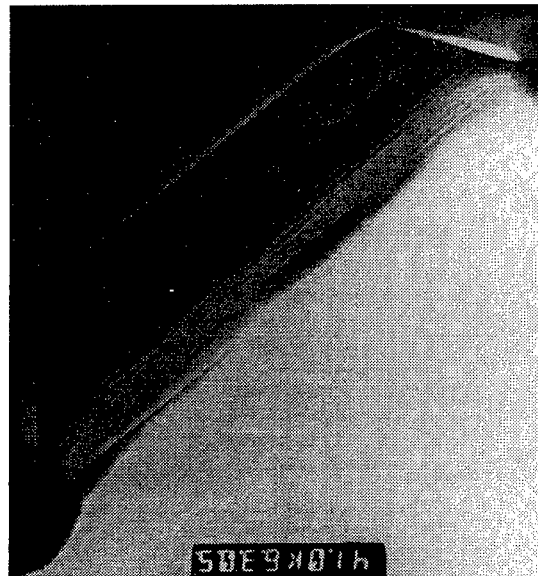
Fig. 7 : X-TEM micrograph of the InGaAsP MQW structure selectively grown in a 2 µm wide opening, with 20 µm wide masks.

The structural quality was examined by cross-sectional transmission electron microscopy (X-TEM). In the limit of resolution of TEM, the thickness layer is identical for all wells. In addition the lateral thickness variation is negligible (fig.7).

A wavelength shift over 200 nm is obtained with a thickness enhancement of only 2.5 times. A large part of shift is attributed to the relative composition variation.
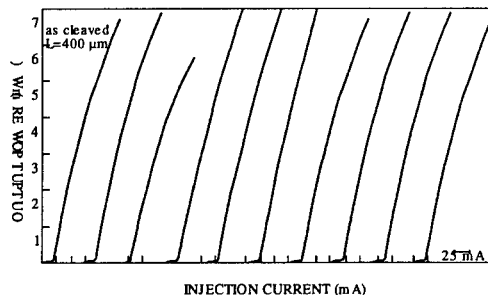
Fig. 8: P(I) characteristics for 10 consecutive lasers grown by SAG with W_o=2 µm and W_m=20 µm.

We fabricated a buried heterostructure laser with no semiconductor etching process as reported by Y. Sakata

600

et al [4]. The masks were removed and 2 µm p InP and 0.3 µm p+ InGaAs have been regrown on the 2 µm wide mesa formed by selective area growth. Figure 8 shows the output power versus injection current characteristics for 10 adjacent lasers. The characteristics are very uniform with an average threshold current of about 14 mA for as cleaved lasers with 400 µm cavity length.

In summary a study of thickness and composition variation in SAG has been realised by atmospheric pressure MOVPE. We established that the relative variation of III elements is different for narrow (<3µm) and large (>5µm) opening regions. This difference of behaviour may be explored for many applications. It also has been demonstrated that the growth in narrow openings, as low as 2 µm, yields excellent quality material and good laser characteristics.

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Migration Effect from a Masked Region for InGaAsP-Selective MOVPE

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Introduction

Selective MOVPE growth [1] is widely used for fabricating integrated waveguide devices such as DFB-LD integrated EA modulators [2-4] or laser diodes equipped with a spot size converter [5]. This technique makes it easy to achieve in-plane bandgap control and thickness control, simply by changing the dielectric mask's geometry [1]. Lateral vapor phase diffusion from the masked region to the growth region has generally been assumed to be the principal mechanism for growth rate enhancement and composition change for selective MOVPE [1][6], and surface migration from the masked region[7-8] has been thought to be a minor mechanism. The effect of surface migration, however, plays a particularly important role for selective MOVPE growth in narrow stripe regions (i.e. 0.5-2.0 µm widths) [1-2, 4, 9-10] but this has not yet been closely investigated.

In this paper, we discuss the effect of surface migration from a dielectric-masked region for InGaAsP-selective MOVPE growth. This paper proposes a novel method for identifying the effective surface migration length in a dielectric-masked region by introducing the concept of obtaining the threshold mask width for the vapor phase diffusion effect. We have found that the surface migration effect and vapor phase diffusion effect have different mask width dependences for the growth rate and composition change.

1. Experimental

MOVPE growth was performed at a temperature of 650 °C and pressures of 25, 75 and 150 Torr. Trimethylindium (TMIn) and triethylgallium (TEGa) were used as the group-III source materials. Arsine (AsH$_3$) and phospine (PH$_3$) were used as the group-V source materials. A schematic structure of selectively grown layers is shown in Fig. 1.

Typically, a 100-nm thick SiO$_2$ film is deposited on a (100) just oriented n-InP substrate by an atmospheric CVD method. Then, a pair of SiO$_2$ mask stripes are patterned by a conventional photolithography technique and wet etching with buffered HF solutions. The mask stripe width W$_m$ is varied from 1 to 50µm while keeping the open stripe width at 1.5µm. These stripes are formed in the [011] direction. Next, ridge-type InP (50nm) /InGaAsP (40nm) /InP (100nm) double hetero structures are grown in the open stripe regions. The typical growth rates are 0.75 µm/h for InP and 0.60 µm/h for InGaAsP, and the V/III ratio is around

200. Note that the above mentioned growth conditions are for an unmasked region (W$_m$=0µm). The selectively grown layers are surrounded by quite smooth (100) and (111)B crystal planes[1] and this structure has already been used for many advanced optical waveguide devices[2, 4, 10-13].

SEM observations were made to evaluate the thickness of selectively grown layers. Micro-area photoluminescence (µ-PL) measurements at room
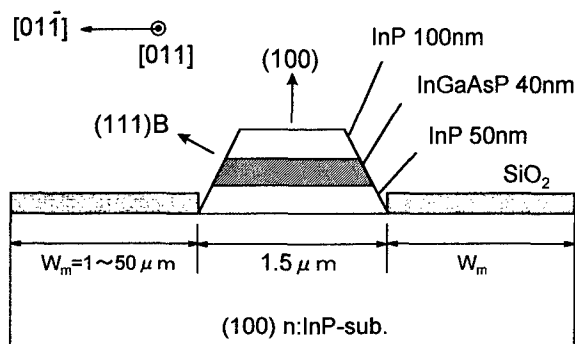
Fig. 1 Schematic structure of selectively grown layers.

temperature were used for estimating the bandgap wavelength of the selectively grown layers, where an Ar^+ laser beam was focused to a 1μm spot diameter with an excition light power density of $30kW/cm^2$.

The crystal compositions of selectively grown InGaAsP layers were calculated from the layer thickness and PL wavelength including both the quantum effect and strain effect. In these calculations, the variations of group-V for the different mask widths were ignored[1].

2. Results and discussions

Figure 2 shows the mask width dependence of the normalized growth rate for selectively grown InGaAsP (Q1.13, Q1.29 and Q1.55) and InP layers. The growth pressure (P_g) was 75 Torr. In the figure, there are two different gradient slopes giving the inflection points around W_m=7 μm. The first one (W_m<7μm) shows the effect of surface migration from a masked region, and the second one (W_m>7μm) shows the effect of lateral vapor phase diffusion. We defined the intercepts as the threshold mask widths (W_{th}) where the vapor phase diffusion effect started to occur (Fig. 1).

In regions where surface migration is dominant (e.g. W_m<5μm), source materials reaching the SiO_2 mask will migrate to the open stripe area and incorporate into the selectively grown layer. In other words, source species are substantially consumed in the masked region. Therefore, there is no gradient for the source concentration in the lateral vapor phase and no lateral vapor phase diffusion is occurs. Therefore, we can define the effective migration length (L_m) in the masked region to be equal to $W_{th}/2$.

The dashed lines in Fig. 2 show results calculated using L_m (=$W_{th}/2$), measured as the diffusion length with the diffusion coefficient as the adjusting parameter. They agree well with the experimental data and support the validity of the proposed model. In other words, we can identify L_m by ascertaining W_{th}. Using this model, L_m at P_g= 75 Torr was estimated to be 3.5-4.0 μm for several compositions. We also found that the effective migration length (L_m) was strongly dependent on the growth pressure.
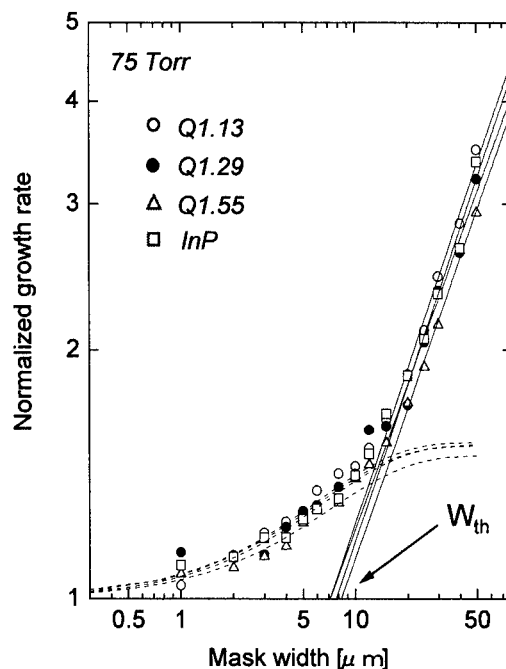
Fig. 2 Mask width dependence of the normalized growth rate for Q1.13, Q1.29, Q1.55 and InP. The dashed lines show results calculated using the measured L_m. Q means InGaAsP (quaternary) and the suffix indicates the band gap wavelength.
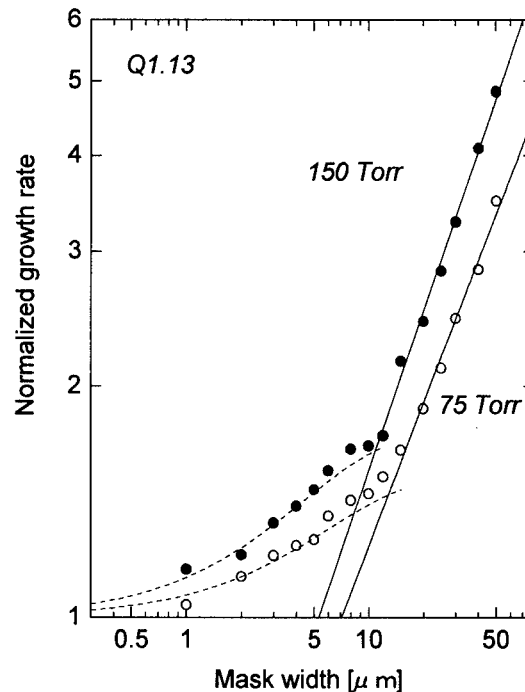
Fig. 3 Mask width dependence of the normalized growth rate for Q1.13 at different growth pressures. The dashed lines show results calculated using the measured L_m.

Figure 3 shows the mask width dependence of the normalized growth rate for Q1.13 (InGaAsP, λg=1.13µm) at P_g=75 Torr and 150 Torr. In the case of P_g=150 Torr, L_m was decreased and estimated to be 2.5µm. The relationship between L_m and P_g for Q1.13, Q1.29, Q1.55 and InP are shown in Fig. 4. L_m was decreased as the growth pressure was increased for all compositions. This was because the higher growth pressure (i.e., slower flow velocity) resulted in well-decomposed group-III source materials (e.g., DMIn→MMIn→In, DEGa→MEGa→Ga). These materials have several dangling bonds and are reactive to the SiO$_2$ mask, resulting in shorter migration lengths.
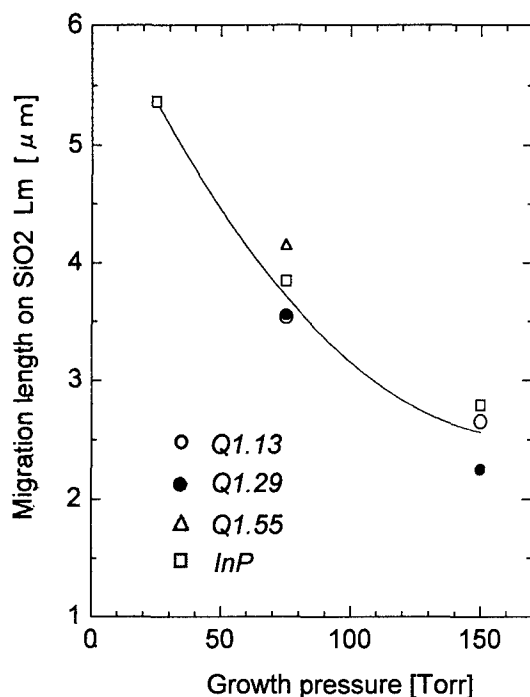
Fig. 4   Growth pressure dependence of the effective migration length L_m.

Next, we discuss composition changes for InGaAsP layers. Figure 5 shows the mask width dependence of the composition change (increase in indium content) for Q1.13 at P_g=75 Torr and 150 Torr. There are also two different gradient slopes around W_m=5-7µm (almost equal to W_{th}). The data can be interpreted to mean that L_m or the sticking factor difference between the In source and Ga

source due to the migration effect is larger than the difference due to the vapor phase diffusion effect.
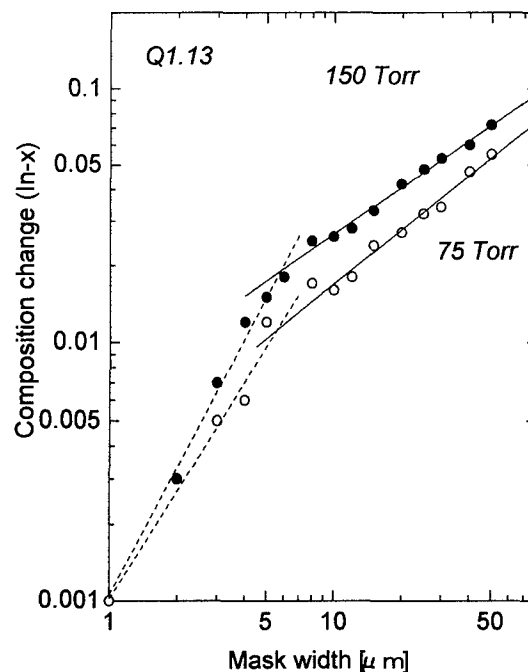
Fig. 4   Mask width dependence of the composition change (increase in indium content) at different growth pressures.

3. Conclusion

We propose the concept of using the threshold mask width (W_{th}) for the vapor phase diffusion effect as a way to identify the surface migration length (L_m) on the surface of a SiO$_2$ mask. We found that L_m strongly depends on the growth pressure.

L_m was decreased as the growth pressure was increased. This was because the higher growth pressure resulted in well-decomposed group-III source materials which have several dangling bonds and are reactive to the SiO$_2$ mask.

We also showed that the mask width dependences of both the growth rate and composition clearly change around W_m=W_{th}. This result means that the surface migration effect and vapor phase diffusion effect have different tendencies concerning mask width variations.

4. Acknowledgments

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Formation of InAsP layer on corrugated InP substrate by MOVPE for buried grating of DFB lasers

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Introduction

Characteristics of the InAsP layer formed on corrugated InP substrate by mass-transport mechanism have been investigated for use as the buried grating of distributed feed-back (DFB) lasers. The size of the InAsP layer can be controlled by the height of the corrugation, and the arsenic composition in the InAsP layer can be controlled by the AsH_3 partial pressure. Fabricated 1.3 µm DFB lasers which have InAsP layer as absorptive grating have shown low threshold current and high slope efficiency from -40 ~ +85°C, and high reliability have been demonstrated.

I. Background

The InGaAsP distributed feed-back (DFB) laser is the most promising light source for high-speed optical communications. Recently, the use of InAsP layer as the buried grating has been reported, which is formed by annealing the corrugated InP substrate in the mixed atmosphere of arsine (AsH_3) and phosphine (PH_3) during the MOVPE (metalorganic vapor phase epitaxy) growth by mass-transport mechanism.[1-3] We have previously reported that the InAsP layer can be utilized as absorptive grating for the gain-coupled (GC) DFB lasers[1] and demonstrated high performance of the fabricated GC-DFB lasers.[4][5] However, the detail characteristics of the InAsP layer and the influence on the reliability of the lasers have yet to be clarified. To realize DFB lasers with high performance, precise control of the coupling coefficient is an important issue. From this point of view, we investigated the controllability of the size and the composition of the InAsP layer by changing the corrugation height fabricated on the InP substrate and the AsH_3 partial pressure in the annealing process. Furthermore, we investigated the influence of the compressively strained InAsP layer on the property of the multiquantum well (MQW) as an active layer and on the reliability of the lasers.

Fig. 1 Fabrication process of samples

II. Experimental procedure

Figure 1 shows the fabrication process of the studied samples. The triangular corrugation (pitch: 203 nm, height: 30 ~ 90 nm) in the <Ī10> direction was formed on Sn-doped InP substrate which is just-oriented (001) as shown in Fig. 1(a) using the conventional holographic photolithography and chemical etching. In the next step, the corrugated substrate was heated up to 600°C within 15 min in a mixed atmosphere of AsH_3 and PH_3 as shown

in Fig. 1(b). During the heating, the AsH_3 partial pressure (P_{AsH_3}) was 1.3 ~ 6.8×10^{-3} Torr and the PH_3 partial pressure (P_{PH_3}) was 2.7×10^{-1} Torr. During this process, in the troughs of the corrugation, the InAsP layer was selectively formed from AsH_3, PH_3 and transported indium from the convex region of the corrugated substrate. Then undoped or Si-doped InP layer (50 ~ 200 nm thickness) or undoped InGaAsP layer (λ_g = 1.05 µm, 50 nm thickness) was grown on the substrate by low pressure (60 Torr) MOVPE

as shown in Fig. 1(c). For some of samples, then undoped InGaAsP guide layer (λ_g = 1.05 μm, 50 nm thickness), strained-layer MQW (SL-MQW), undoped InGaAsP guide layer (λ_g = 1.05 μm, 30 nm thickness) and undoped InP layer (200 nm thickness) were grown as shown in Fig. 1(d). The SL-MQW is composed of 10 pairs of 6-nm-thick compressively strained InGaAsP ($\Delta a/a$ = 0.6%) well layer and 10-nm-thick InGaAsP (λ_g = 1.05 μm) barrier layer. The composition of strained well layers was adjusted for the PL (photo-luminescence) peak wavelength of SL-MQW to be 1.3 μm at RT. The structures of the grown samples were evaluated by transmission electron microscopy (TEM). The composition of the InAsP layers was evaluated by energy dispersive spectroscopy (EDS) using a focused electron beam in the TEM. The optical characteristics were evaluated by PL spectrum at the measurement temperature of RT and 77K. The excitation wavelength in the PL measurements was 514.5 nm.

III. Experimental results and discussions

A. TEM image

Figures 2 (a), (b) show the TEM micrographs of the ($\bar{1}$10) cross-sectional image for the grown samples. The samples of (a) and (b) were formed on the 60-nm-height and 30-nm-height corrugated InP substrates under the condition of P_{AsH3} = 2.7×10^{-3} Torr and 4.1×10^{-3} Torr, respectively. Both have undoped InP layers (200 nm thickness) on the InAsP layers. It is clearly shown that the triangular shaped InAsP layer is successfully formed in the trough of the corrugated InP substrate for the each case. It has been previously reported that slip-line dislocations generate along {111} planes in the structure in which the InGaAsP layer is directly grown on the corrugated InP substrate after the heating in the mixed atmosphere of AsH₃ and PH₃.[6] However, in these graphs, there are no dislocations around the InAsP. The height of the layers is about 35 nm and 9 nm for (a) and (b), respectively. This result show that the size of the InAsP layer can be controlled by the height of the corrugation.

(a)

(b)

Fig. 2　TEM images of the grown samples

(a) P_{AsH3} : 2.7×10^{-3} Torr, corrugation height : 60 nm

(b) P_{AsH3} : 4.1×10^{-3} Torr, corrugation height : 30 nm
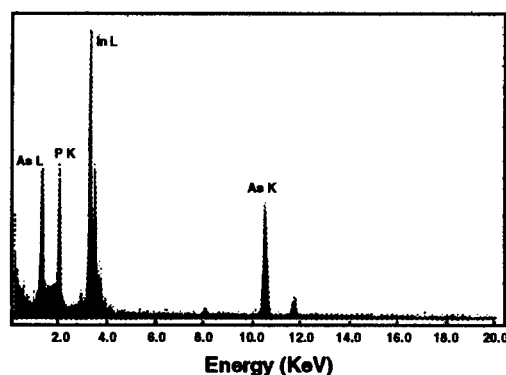
Fig. 3　EDS spectrum of grown sample
(P_{AsH3} = 4.1×10^{-3} Torr)
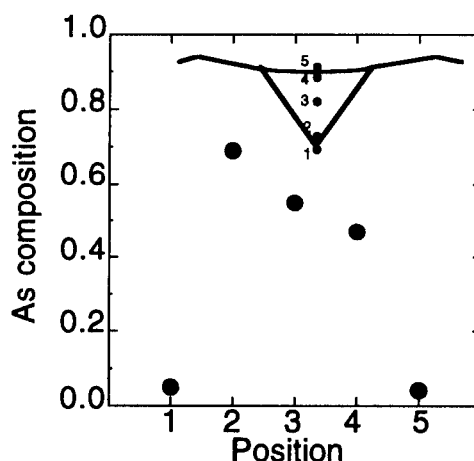
Fig. 4　Position dependence of As composition in the InAsP layer (P_{AsH3} = 4.1×10^{-3} Torr)

607

B. EDS measurement

Figure 3 shows the EDS spectrum of the grown sample. The measurement was carried out at the center of the InAsP layer. The sample was formed on the 90-nm-height corrugated InP substrate under the condition of P_{AsH3} = 4.1×10^{-3} Torr and has Si-doped InP layer (200 nm thickness). In this spectrum, the peak of Ga is not observed and the layer formed by annealing is confirmed to be InAsP. The peak at about 12 KeV originates from Cu in the sample holder. Figure 4 shows the position dependence of the arsenic composition in the InAsP layer. The inserted figure shows the measured positions. At the nearest position to the substrate, arsenic composition of InAsP is 0.69, which means a compressive strain of 2.2%. This arsenic composition is much larger than the maximum value (~ 0.3) [2] in the structure which has the InGaAsP layer directly grown on the InAsP layer. Arsenic composition decreases as the distance from the substrate increases. During the heating, the change in decomposition efficiency of PH_3 is larger than that of AsH_3, which results in the change of arsenic composition.

C. PL measurement

Figure 5 shows the PL spectra from the grown samples taking P_{AsH3} as the parameter at RT. The samples were formed on the 90-nm-height corrugated InP substrates and have Si-doped InP layer (200 nm thickness). The emission from InAsP layer that has a peak at 1.21 μm is shown in the PL spectrum from the sample (P_{AsH3} = 2.7×10^{-3} Torr). The peak wavelength increases with an increase of P_{AsH3}. This result means that the arsenic composition in the InAsP can be easily controlled by P_{AsH3} during the heating.

Fig. 6 shows FWHM (full-width at half maximum) of PL spectra from the SL-MQWs above InAsP layers grown on substrates with the different corrugation height. The corrugation height of 0 nm means the plane substrate. The measurements were carried out at 77 K. All samples were formed under the condition of P_{AsH3} = 2.7×10^{-3} Torr and 50-nm-thick buffer layer between the InAsP layer and the InGaAsP guide layer.
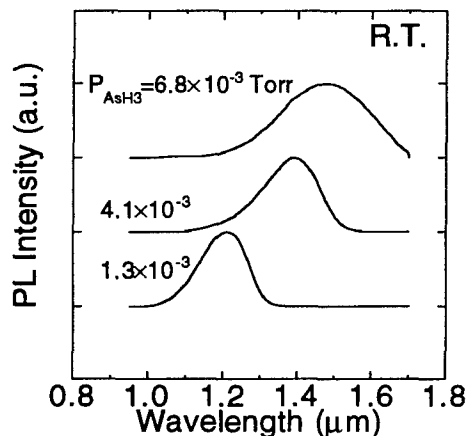
The closed circles and open circles show samples with undoped-InP buffer layers and undoped-InGaAsP buffer layers, respectively. In the case of InP buffer layer, FWHM value scarcely depends on the corrugation height. On the other hand, in the case of InGaAsP, FWHM broadens with increasing the corrugation height. The results of TEM, EDS and PL show that InP is suitable as the buffer layer between InAsP layer and MQW. In the case of InGaAsP, the broadening of PL spectrum is thought to be resulted from the fluctuation of the well width due to undulation of the surface of the InGaAsP buffer layer.

D. Device results

We fabricated 1.3 μm SL-MQW-GC-DFB lasers which have InAsP layer as absorptive grating.[7] The InAsP layer was formed on the 90-nm-height corrugated InP substrate under the condition of P_{AsH3} = 2.7×10^{-3} Torr for the grating to realize suitable coupling coefficient. These lasers has buried heterostructure and the cavity of 300 μm. Figure 7 shows the typical CW light-injection current characteristics of an AR/HR (5%/80%) coated laser taking the heat-sink temperature as the parameter. At 25 °C , the threshold current and the slope efficiency are 8.9 mA and 0.60 mW/mA, respectively. Even at 85°C, the threshold current and the slope efficiency are 30.6 mA and 0.41 mW/mA, respectively. This slope efficiency at 85°C is the highest reported value as far as we know. The side-mode suppression ratio of more than 40 dB is maintained in the measured temperature range.

Figure 8 shows the life test data. The measured lasers have the threshold currents of 10 ~ 15 mA and the slope efficiency of 0.5 ~ 0.6 mW/mA. The power was held constant (16mW) at 70°C. For more than five thousand hours, no degradation is observed. This result shows that DFB lasers with InAsP grating have high reliability for use in optical communication systems in spite of large compressive strain in InAsP.

Fig. 5 PL spectra from the grown samples taking P_{AsH3} as the parameter
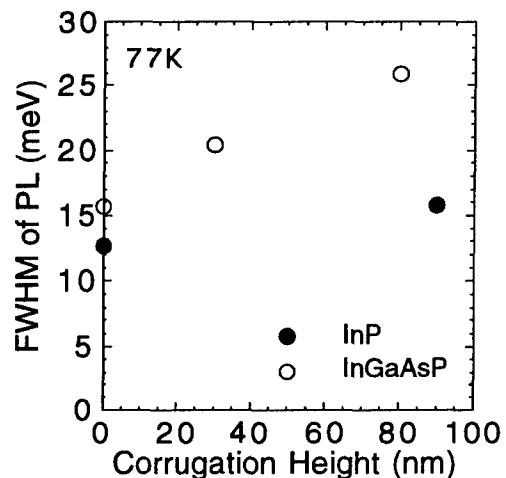
Fig. 6 FWHM of PL spectra from the strained-layer MQWs above InAsP layers grown on substrates with different corrugation height taking kind of the buffer layer as the parameter
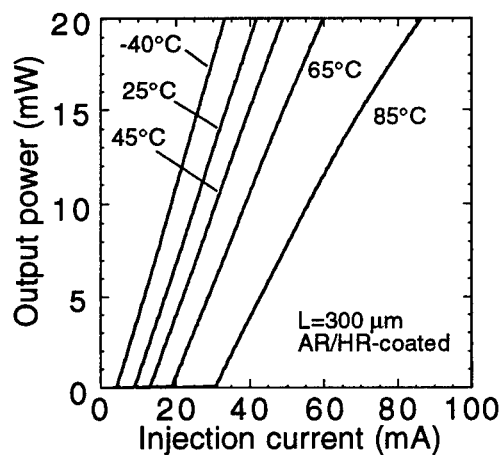
Fig. 7 CW light-injection current characteristics of an AR/HR (5%/80%) coated laser taking the the heat-sink temperature as the parameter

Fig. 8 Life test data of fabricated lasers under the condition of 16 mW APC at 70°C

IV. Conclusions

We have investigated the characteristics of the InAsP layer which is formed by annealing the corrugated InP substrate in the mixed atmosphere of AsH_3 and PH_3 during the MOVPE growth. The size of the InAsP layer can be controlled by the height of the corrugation fabricated on the InP substrate, and the arsenic composition in the InAsP can be easily controlled by the AsH_3 partial pressure. The results of TEM, EDS and PL show that InP is suitable as the buffer layer between InAsP layer and MQW active layer. Furthermore, fabricated 1.3 μm SL-MQW-GC-DFB lasers which have InAsP layer as absorptive grating have shown low threshold current ($\leq$ 30.6 mA) and high slope efficiency ($\geq$ 0.41 mW/mA) from -40 ~ +85°C, and high reliability have been demonstrated.

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MOVPE-BASED LOCALIZED EPITAXIAL GROWTH TECHNIQUES AND ITS APPLICATIONS

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Introduction

As the functionality of InP-based photonic integrated circuits (PICs) is increasing rapidly and a wider range of components are integrated on a single chip, there is a need for advanced epitaxial techniques which enable the formation of regions with different bandgap energy simultaneously in a single epitaxial growth step. In this paper two MOVPE-based technologies which have the potential to meet those requirements are reviewed: selective area growth (SAG) and shadow masked growth (SMG).

I. Selective area growth (SAG)

During selective area growth (SAG), the substrate is partially covered with a mask, usually SiN_x or SiO_x (see Fig. 1) [1,2]. Selectivity is obtained because of the different surface properties of dielectric mask and semiconductor surface [3]. On the semiconductor surface, the decomposition of precursors, and hence growth, is facilitated by surface catalytic reactions; this effect does not occur on dielectric films. It is therefore important to choose the growth conditions such that surface catalytic reactions are decisive for growth. This implies that reaction of species in the gas phase must be avoided, i.e. the number of collisions between reacting species in the hot zone should be low. Growth on the dielectric mask can be prevented by lowering the reactor pressure, lowering the reagent partial pressure, shortening the transit time in the reactor, increasing the growth temperature and decreasing the mask dimensions.
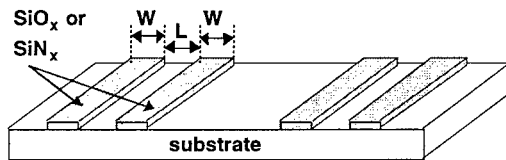
FIG. 1: Principle of selective area growth

During SAG, the growth rate and the growth behaviour is changed. The growth rate in the unmasked region (e.g. between two oxide stripes) is enhanced because molecules or atoms impinging on the mask desorb, the desorbed molecules collides with molecules in the gas phase and are redirected towards the sample surface, where they desorb again if they strike the mask, but stick if they strike the openings in the mask [1]. The deposition of material exclusively in the mask openings results in a lateral concentration gradient in addition to the gradient normal to the surface that is present in diffusion

controlled growth. This means that by increasing the mask surface, the growth rate in the unmasked areas will increase. This is illustrated in Fig. 2 for a mask with constant mask opening ($L = 8\mu m$) and variable oxide stripe width for two reactor pressures [2]. The relative thickness (or growth rate enhancement) is defined as the ratio of the layer thickness in the centre of the mask opening to the nominal layer thickness on an unmasked substrate.
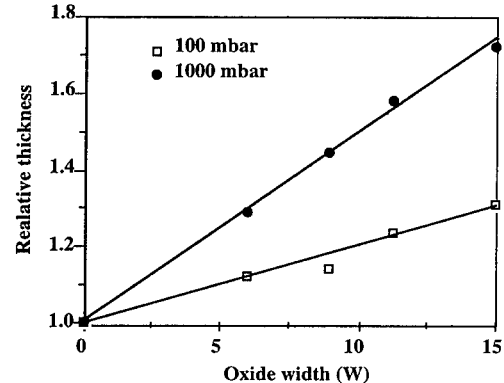
FIG. 2: Relative thickness of selectively deposited InGaAs layers on InP substrates in a 8 μm mask opening between two oxide stripes of variable width for reactor pressures of 100 mbar and 1000 mbar

In Fig. 2 a much higher growth rate enhancement is observed for growth at atmospheric pressure. The growth rate enhancement also seems to be dependent on the material composition. It has been demonstrated that growth rate enhancements (R) for binaries follow the sequence $R(InAs) > R(InP) > R(GaAs) > R(GaP)$ when using TMG, TMI, AsH_3 and PH_3 as precursors [1,4]. The dependence of the growth rate enhancement on reactor pressure and composition cannot simply be explained by a diffusion limited growth process.

Because of the successive impinging and desorbing onto and from the mask during SAG, group III molecules spend a longer time near the substrate and can decompose more in the gas phase [5, 6]. The growth rate during SAG is therefore no longer determined by just the input group III concentration, but also by the amount of vapour-decomposed intermediate species. A methyl-gallium bond is indeed stronger than a methyl-indium bond, which explains the larger InP (InAs) growth rate enhancement with respect to GaP (GaAs). The different growth rate enhancement of the binaries is correlated to the decomposition temperatures of the source molecules, which are in the order: TMI < TMG < AsH3 < PH3. The main effect is the decomposition of the group-III molecules. A secondary effect is the decomposition of the group V molecules and its influence on the decomposition of the group III molecules, as it is assumed that the decomposition of group V molecules is catalyzed by the decomposition of group III molecules and vice versa [7].

From the above considerations it can also be understood why SAG at atmospheric pressure leads to higher growth rate enhancements than at low pressure. At atmospheric pressure the residence time of the growth species in the reactor is larger and therefore the group III molecules spend a longer time above the hot substrate, leading to more decomposed group III molecules in the gas phase compared to low pressure growth.

The composition dependence of the growth rate enhancement for binaries will result in compositional changes when ternary and quaternary alloys are selectively deposited. Many researchers have indeed reported the In enrichment of such alloys [1,4,6,8,9]. Again this can be explained by the enhanced decomposition of the group III molecules in the vapour phase during SAG. The diffusion coefficient, which is mainly dependent on the collision diameter, and hence the size, of the molecule, is larger for decomposed group III species than for non-decomposed molecules. As the decomposition temperature of TMI is lower than that of TMG, more TMI will be decomposed and the In species will have a larger diffusion coefficient and hence a larger gas phase diffusion rate compared to Ga species, which explains why the selectively deposited alloys are In-rich. Next to this, most researchers also observed the highest In enrichment close to the mask edge. Since the In species are more decomposed and hence more reactive, they are more readily incorporated in the crystal than the less decomposed Ga species. When taking into account the lateral gas phase diffusion from the masked area to the semiconductor growth surface during SAG, it becomes obvious that the In enrichment is the highest at the mask edge.

In contrast to the In/Ga ratio, no change in As/P-ratio is observed in selectively deposited InGaAsP. This is probably related to the high V/III ratio used during MOVPE: since only a small amount of group V species is consumed compared to the quantity supplied, the different behaviour between the As and P species is insignificant [9].

So far only adsorption/desorption from the mask and gas phase diffusion has been considered as the mechanism responsible for selectivity. Another proposition is surface diffusion from the dielectric mask and from side facets near the mask edge. The latter mechanism, however, becomes only dominant when the distance between the oxide stripes is very small (smaller than a few μm), at high reactor pressures and high growth rates.

II. Shadow masked growth (SMG)

SMG uses a mask that is mechanically held at a certain distance above the substrate as shown in Fig. 3. [10,11]. During epitaxial growth, deposition on the substrate will take place through the window in the shadow mask. Since MOVPE is a diffusion limited growth process, growth through a shadow mask window will result in a reduced growth rate with respect to the growth rate on a planar substrate, because the concentration gradient is locally decreased at the substrate surface in the mask window. By changing the distance between the mask and the substrate (D) or the width of the window (W), it is possible to control the thickness reduction in the middle of the window. The higher the distance (D) and the smaller the width (W), the higher the growth rate reduction. With a constant mask-substrate spacing, it is possible to control the thickness of a layer over the substrate by simply changing the channel widths.
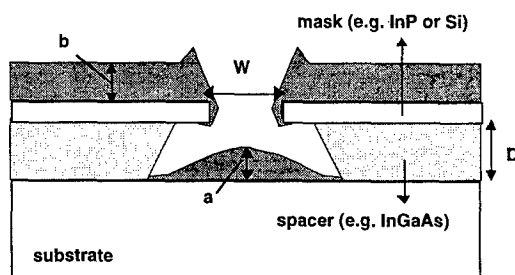
FIG. 3: Principle of shadow masked growth

There exist several methods to implement SMG. A first method uses a monocrystalline mask (e.g. InP) on top of a spacer layer (e.g. InGaAs). First the windows in the mask layer are etched. Then the spacer layer is selectively etched through until a reasonable undercutting is achieved (typically 10 to 20 μm). Fig. 4 shows the relative growth rate or growth rate reduction ($= a / b$) as a function of the mask width W and the reactor pressure.

Theoretical calculations based on a simple gas phase diffusion model agree well with experimental results obtained at atmospheric pressure and have shown that only the ratio W/D (width/spacing) determines the relative growth rate [12]. A more accurate model, including the release of radicals from physisorbed group-III species and recombination of these radicals with other physisorbed species followed by lateral gas phase diffusion and incorporation, gives a better fitting of the shape of the profile in the growth window [13]. The latter model assumes that the radicals have a longer residence time under the mask than on a normal growth surface, as their only

611

escape route is diffusing through the open window. None of these models, however, can explain why the growth rate reduction is higher at higher reactor pressures, as observed in Fig. 4. Perhaps the smaller growth rate reduction at low pressures could be explained by the increased group III diffusion rates.
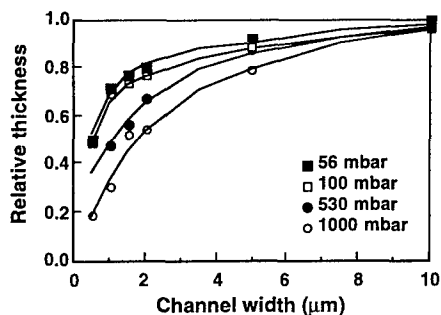
FIG. 4: Relative thickness of InP layers deposited on a InP substrate through a mask window of variable width for reactor pressures between 56 and 1000 mbar

During SMG, there are also compositional changes: unlike SAG, InGaAs(P) layers deposited in a small mask window become clearly Ga-rich. This can be attributed to the different diffusion rates of TMG and TMI: TMG diffuses faster than TMI and therefore more TMG is incorporated in the growth window. The changes in In/Ga ratio are more pronounced at low reactor pressures.

A second SMG method does not use a monocrystalline mask, but a pure mechanical mask. The mask consists of a comb-shaped silicon shadow mask placed just above the substrate as illustrated in Fig. 5 [14]. In this case there is no spacer layer, but just a gap between substrate and mask, which is established by using a special substrate holder. The silicon mask is coated with SiO_2 in order to prevent nucleation on the mask. The growth mechanism is rather complex as it is composed of a depletion of species under the mask and an excess of growth species on the dielectric mask. Nevertheless very smooth layers and large thickness reductions were obtained. InGaAsP-layers under and in the neighbourhood of the mask are believed to be Ga or P rich. Taking into account the high V/III-ratio during MOVPE-growth, the layers become most probably Ga-rich, which is consistent with SMG using monocrystalline masks.
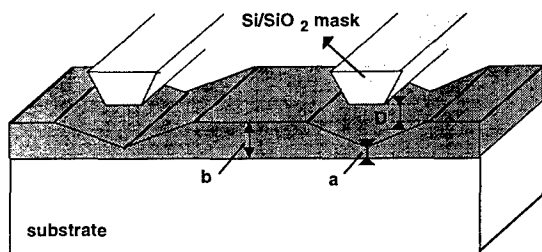
FIG. 5: Principle of SMG using a Si/SiO_2 shadow mask

III. Comparison of SAG and SMG

The SAG and SMG exhibit a lot of similarities on one hand, and a lot of contrasts on the other hand. Both the SAG and SMG technique are able to achieve lateral thickness variations over a (partially) masked substrate. Both techniques translate horizontal dimensions (window width) into vertical dimensions (layer thickness). During SAG the growth rate increases, while during SMG the growth rate decreases in the masked areas. By introducing quantum well structures, lateral thickness variations can be converted into lateral bandgap energy variations. Both SAG and SMG show not only thickness variations, but also compositional variations. In both cases, there is a co-operation between thickness reduction and compositional variations with respect to bandgap variations, which means that bandgap shifts caused by thickness variations and compositional variations do not oppose each other. Bandgap energy shifts exceeding 350 meV have been demonstrated for SAG [15] and 85 meV for SMG [11].

A drawback of the SMG-technique using a monocrystalline mask is the additional growth step of the shadow mask and an additional processing step to remove the shadow mask before processing of the device. However this drawback is eliminated by using a mechanical mask instead of a monocrystalline mask. A drawback of SAG is its sensitivity to the substrate preparation and the growth conditions, which must be carefully selected to inhibit deposition on the dielectric mask.

The pressure-dependent growth behaviour during SAG and SMG can be applied to grow layers with different thickness reductions in a single growth step, just by varying the reactor pressure during growth. Changing from low pressure to atmospheric pressure allows a change from a large relative growth rate enhancement (reduction) to a small relative growth rate (reduction) for SAG (SMG).

IV. Applications

Lateral thickness and bandgap variations are very important for the fabrication of PICs, where several passive and active optical components need to be integrated on the same substrate. A first example of such a PIC is a laser with integrated spot size converter or taper. A tapered laser generally consists of an active section in which the light is generated, and a passive section, which is transparent for the light emitted and of which the waveguide dimensions are reduced in order to increase the optical mode size and, hence decrease the beam divergence. SAG tapered lasers have been successfully realised by growing the active section between two oxide stripes, while the tapered section is deposited in an unmasked region [16]. SMG tapered lasers using a monocrystalline mask [17] as well as a mechanical Si mask [14] have been realised. The 3 types of tapered lasers all exhibit low threshold currents (resp. 9 mA, 8 mA and 12 mA) and narrow beam divergences (below 15° in

both directions). For the tapered laser application the SMG technique is advantageous to the SAG technique because the active layer can be grown in the non-masked area of the substrate, assuring high quality layers, while during SAG the active layers are selectively deposited. However when the dimensions of the passive area becomes much larger than the active section, SAG might be more suited. An example of such an application is a multi wavelength laser consisting of amplifiers integrated with a phased array waveguide (de)multiplexer [18].

Another well known application of SAG is the integration of a laser with an electro-absorption modulator, where again the laser is grown between two oxide stripes and the modulator, which needs a higher bandgap energy, in the unmasked area. SAG laser/modulator devices with superior performances have been realised: a 2.5 Gbit/s penalty-free data transmission over 80 km normal single mode fibre has been demonstrated [19].

One of the most impressive realisations is perhaps a complete SAG-based transceiver PIC where a DFB laserdiode, a monitor photodiode and a receiver photodiode are monolithically integrated with a Y-shaped branch waveguide: excellent characteristics, such as a fibre output of more than 1 mW in the DFB laserdiode and a bandwidth of 7 GHz for the receiver photodiode, were obtained [20].

V. Conclusion

In this paper the principle of SAG and SMG have been reviewed. It has been demonstrated that both techniques have the potential to realise advanced PICs where different bandgap energies are required for the different integrated components.

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EFFECT ON REGROWTH INTERFACE QUALITY OF A NEW TREATMENT, ACE* IN A PROCESS USING HYDROCARBON GAS RIE TO FABRICATE InP-BASED BH-LD**

*ACE: Ammonium sulfide Combined Etching
*BH-LD: Buried-Heterostructure Laser Diodes

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Introduction

ACE (ammonium sulfide combined etching) is a new treatment designed for use in the hydrocarbon-gas-RIE-based fabrication of InP-based buried-heterostructure (BH) laser diodes (LD). ACE involves dipping a sample in ammonium sulfide (NH_4S_x) solution at RT for 10 min. and then treating it again with sulfuric acid prior to regrowth. We found that ACE improves regrowth interface quality and LD characteristics due to its ability to remove impurities incorporated during the process.

I. Background

In InP-based buried-heterostructure (BH) laser diodes (LD) fabrication, a process based on reactive ion etching (RIE) with hydrocarbon gases has attracted much attention [1-5]. The process consists of RIE, oxygen plasma treatment for the removal of polymers deposited during RIE, chemical treatment, and metalorganic vapor phase epitaxy (MOVPE) BH regrowth. Although RIE can accurately form a mesa shape in the LD, there remains a problem that plasma damage and impurities are induced in the mesa surface during the process [6]. In regrowing the BH structure on the mesa surface, the damage and impurities remain at the regrowth interface and result in a leakage current that increases the threshold current (I_{th}) during BH-LD operation. In particular, the oxygen plasma treatment can oxidize the mesa surface; oxygen is incorporated into the regrowth interface and this affects the LD characteristics. Thus, oxygen is thought to be an important impurity that could affect the regrowth interface quality in the BH-LDs. There is also a problem that the densities of the damage and impurities tend to be different with each process run.

This could degrade reproducibility in the BH-LD fabrication. Therefore, it is essential to remove the damage and the impurities from the processed surface prior to BH regrowth. In this work, we describe a new treatment, ACE (ammonium sulfide combined etching), that can remove impurities incorporated when hydrocarbon gas RIE is used in the fabrication of BH-LDs. We also discuss the effect of ACE on regrowth interface quality and device characteristics based on results of its application to the BH-LD fabrication process.

II. ACE basic effect

A. Surface electrical properties

We studied ACE effect on the electrical properties of InP surface damaged by CH_4/H_2-RIE process. We grew a 1-μm-thick Zn-doped (3×10^{17} /cm^3) p-InP layer on p-InP (100) substrate by MOVPE (referred to as sample A). First, AuZnNi ohmic contacts were formed on the back side of the sample in order to prevent the heat treatment for alloying them from altering the damage. Next, the surface was treated by a process consisting of CH_4/H_2 RIE (sample B), oxygen plasma

treatment(sample C), sulfuric acid treatment (sample D) and ACE (sample E) in succession. The ACE treatment was performed by dipping the sample in ammonium sulfide (NH_4S_x) solution at RT for 10 min. and then treating it again with sulfuric acid. After the process, Au Schottky barriers were evaporated on the surfaces. Current-voltage (I-V) characteristics were used for the electrical evaluation.

Fig. 1 shows forward I-V characteristics during each step of the process using CH_4/H_2-RIE. The as-grown surface before RIE showed good Schottky forward I-V characteristics with Schottky barrier height ϕ of around 0.70 eV (sample A). After RIE, forward I-V characteristics degraded because of the high leakage current, which increased by more than two orders of magnitude due to the RIE damage (sample B). The oxygen plasma treatment put the forward I-V characteristics out of the ideal exponential curve (sample C). This is because the treatment causes surface oxidation. The characteristics of samples A, B, and C were similar to those described in Ref. 6. After sulfuric acid treatment, the I-V characteristics did not follow an exponential curve (sample D). This shows damage or impurities caused by the RIE and oxygen plasma treatment still remained on the surface. After performing ACE, the I-V characteristics had an exponential curve, although they did not completely return to those of as-grown layer. This means the

ACE treatment removed most of the surface damage or oxide induced by the CH_4/H_2-RIE process. This means ACE is effective for recovering surface electrical properties.

B. Impurity pile-up at regrowth interface

We studied ACE effect on pile-up of impurities incorporated during the CH_4/H_2-RIE process at the regrowth interface. This was measured by secondary ion mass spectroscopy (SIMS) at the regrowth interface of the undoped InP layer regrown on (100) n-InP surface treated by the CH_4/H_2-RIE process. Fig. 2 shows oxygen profiles around the interfaces on the surface with and without ACE. The impurity pile-up concentrations at the interfaces are listed in Table 1. Without ACE, the oxygen concentration was as high as 1×10^{18} /cm^3. Silicon (Si) and carbon (C) were also observed. Their concentrations were 2×10^{17} and 4×10^{16} /cm^3, respectively. With ACE, on the other hand, the oxygen and Si concentrations were drastically decreased (oxygen; 2×10^{17}, Si; 6×10^{16} /cm^3), and C was not detected. In addition, sulfur, which could adhere on the processed surface during NH_4S_x treatment, was not detected at the interface treated with ACE. This shows that the sulfur could be removed by the sulfuric acid treatment performed successively after NH_4S_x treatment in ACE. These results show ACE suppresses impurity incorporation

Fig. 1. Forward I-V characteristics during each step of the process using CH_4/H_2 RIE; (A) as-grown, (B) RIE, (C) oxygen plasma treatment, (D) sulfuric acid treatment, and (E) ACE.
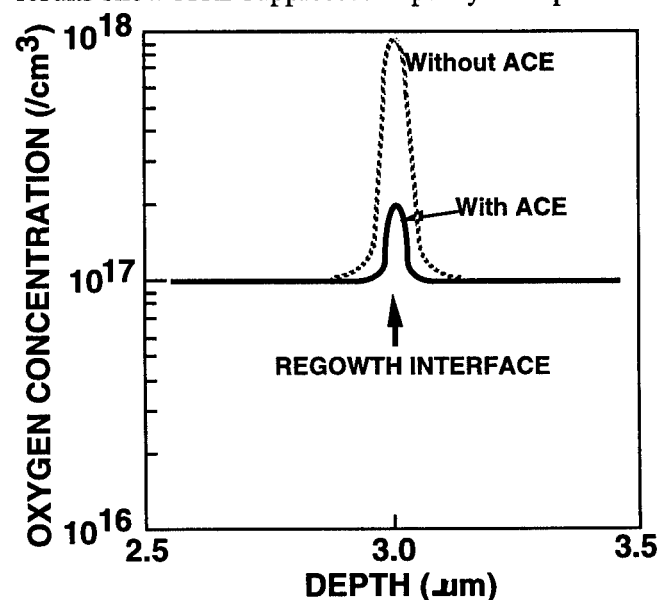
Fig. 2. SIMS profiles of oxygen around the interfaces regrown after the processes with and without ACE.

615

Table 1. SIMS impurity pile-up concentrations at the regrowth interfaces.

Treatment	Impurity concentration (/cm^3)		
	Oxygen	Silicon	Carbon
Without ACE	1×10^{18}	2×10^{17}	4×10^{16}
With ACE	2×10^{17}	6×10^{16}	not detected

at the regrowth interface. Exactly how ACE removes impurities has not been clarified, but it might be that sulfur adhesion to the processed surface during NH_4S_x treatment changes the bonding state between impurities and the InP surface.

III. ACE application to BH-LD fabrication

A. Experimental

We fabricated BH-LDs with pn-blocking layers. The LD structure was grown on an n-InP substrate by MOVPE. The multiple-quantum-well active layer consisted of eight 6-nm-thick InGaAsP strained wells ($\varepsilon=1.2\%$) and seven 8-nm-thick InGaAsP barriers ($\lambda_g=1.1$ μm). After the mesa structure was formed by RIE using CH_4/H_2 gas, the mesa surface was successively treated with oxygen plasma, sulfuric acid and ACE. Finally, the mesa structure was embedded by buffer-layer-inserted (BI)-BH MOVPE regrowth [3], in which the p- and n- dopants were Zn and Se, respectively. For reference, we also fabricated a BH-LD without ACE.

B. Leakage current

Fig. 3 shows forward I-V characteristics for BH-LDs fabricated with and without ACE. For both LDs, the I-V characteristics in the low-forward-bias region are not exponential but linear. This shows that the forward current is a leakage current that does not flow through the pn-junction in the active layer but flows through the degraded regrowth interface with high conductivity at the mesa side. In high-forward-bias region, the I-V characteristics are exponential. In other words, the forward current begins to flow through the pn junction because the electrostatic potential difference across the pn-junction is lowered. For the BH-LDs fabricated with and without ACE, the leakage currents at a forward bias of 0.5 V were 0.01 and 0.7 mA, respectively. Thus, the leakage current for the BH-LD fabricated with ACE was about two orders of magnitude lower than that for the one fabricated without ACE. This means that ACE can improve the electrical properties of the mesa-side regrowth interface in the BH structure.

C. LD characteristics

Fig. 4 shows light-current characteristics of the BH-LDs fabricated with and without ACE in the measurement temperature range from 25 to 85 °C. The cavity length was 300 μm and both facets were cleaved. ACE lowered threshold currents (I_{th}s) from 6.2 to 5.2 mA at 25 °C and from 30.7 to 20.3 mA at

Fig. 3. Forward I-V characteristics for BH-LDs fabricated by the processes with and without ACE.
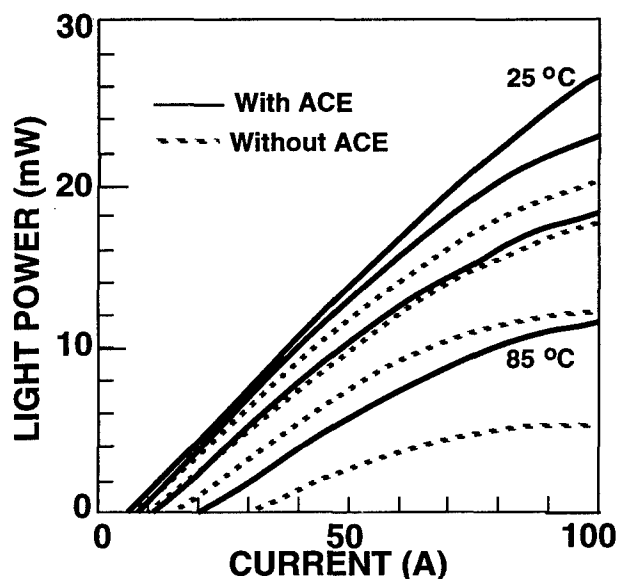
Fig. 4. Light-current characteristics of the BH-LDs fabricated with and without ACE at the measurement temperatures of 25, 45, 65, and 85 °C.

85 °C. ACE also enhanced the slope efficiencies from 0.29 to 0.33 W/A at 25 °C, and from 0.13 to 0.22 W/A at 85 °C. While these characteristics are not as good as those reported for a BI-BH LD corresponding to the LD fabricated without ACE [5], it is apparent that ACE can suppress the degradation of LD characteristics. This suggests that ACE is effective at the least for improving reproducibility in the BH-LD fabrication process using CH_4/H_2-RIE.

D. Discussion

We try to estimate the leakage current at the threshold in BH-LD operation. For this purpose, we measured the dependence of threshold current on stripe width for BH-LDs. The threshold current I_{th} is given by

$$I_{th} = (I_{th})_{pn} + I_{leak} \qquad (1),$$

where $(I_{th})_{pn}$ is a forward current at the threshold which flows through the pn junction and I_{leak} is a leakage current which flows along the mesa sides. Since $(I_{th})_{pn}$ is proportional to stripe width W and I_{leak} is constant, independent of W,

$$I_{th} = (J_{th})_{pn} W L + I_{leak} \qquad (2),$$

where $(J_{th})_{pn}$ is the density of current flowing through the pn junction and L is cavity length. As seen from Eq. (2), $I_{th} = I_{leak}$ when W = 0. In other words, plotting I_{th}s as a function of W, the point where the extension of the plot and the vertical axis intersect corresponds to the leakage current at the threshold. Fig. 5 shows I_{th} plots as a function of W

for BH-LD fabricated with and without ACE. From the plots, we obtained I_{leak}s of BH-LDs fabricated with and without ACE of 0.1 and 3 mA, respectively. This shows ACE also works to lower the leakage current at the threshold in BH-LD operation.

IV. Summary

We proposed a new treatment called ACE (ammonium sulfide combined etching) for use in the fabrication of InP-based BH-LDs by hydrocarbon gas RIE. ACE involves dipping a sample in ammonium sulfide (NH_4S_x) solution at RT for 10 min. and then treating it again with sulfuric acid prior to regrowth. We found that ACE can (1) remove impurities incorporated during the process, (2) lower leakage current flowing through the degraded regrowth interface with high conductivity at the mesa side, and (3) improve BH-LD characteristics. With these abilities, ACE is effective for improving reproducibility in BH-LD fabrication using hydrocarbon gas RIE.

Acknowledgments

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Fig. 5. I_{th} dependence on stripe widths for BH-LD fabricated with and without ACE.

617

LOW THRESHOLD CURRENT BH LASERS FABRICATED BY UHV CHEMICAL BEAM ETCHING AND GSMBE REGROWTH

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Introduction

A new chlorine-based chemical beam etching technique (CBET) compatible with MBE or CBE technology has been introduced recently (1-4). The process sequence combining these two techniques in the same MBE growth chamber is very attractive for the realisation of high performance discrete or integrated optoelectronic devices. In this paper, we present for the first time results on devices fabricated using this new processing technique. Fabry-Perrot type 1.3 and 1.48μm Buried Heterostructure lasers with low threshold current values have been obtained. These results, comparable to the state of the art, pass a milestone in the development of this new technology and open the way to a larger range of applications.

I. Background

Local pattern etching followed by epitaxial regrowth is a generic sequence found in most optoelectronic device wafer processing. The development of an Ultra High Vacuum chemical beam etching technique fully compatible with MBE technology makes the realisation of this etching and regrowth sequence possible in one single run (1, 4). The samples are etched at high temperature inside the growth chamber and regrown without any possibility of external contamination. This should lead to *in-situ* buried interfaces of very high structural and electrical quality. In addition, the purely chemical nature of the etching process makes damages, or defects induced by etching unlikely, contrary to the case of more conventional dry etching techniques. Etching results have been reported for a number of materials, such as: InP (1-4), GaAs (2, 5, 6), AlGaAs (7, 8), InGaAsP and InP/InGaAsP heterostructures (4), but, to our knowledge, no device results have been reported up to now. The purpose of this work was to demonstrate on a simple test-device the performances of this new combined process.

II. Process optimisation

Etching with PCl₃ and regrowth experiments have been performed in a RIBER 2300 MBE chamber (4). PCl₃ is directly evaporated through a mass flow controller and injected in the growth chamber with a gas injection cell. This set-up is very simple and practical and led to very reproducible etch results (3).

The etch conditions for InP, InGaAsP and InP/InGaAsP heterostructures have been optimized and smooth etching conditions found at temperature below 425°C (4). In this low temperature range the etch rate decreases rapidly with temperature (fig. 1), the etch process being limited by the surface reaction kinetics with an apparent activation energy of about 28 kCal/mole. The etch rate for InGaAsP follows a similar trend with rates reduced compared to InP, due to the preferential etching of Indium compared to Gallium (4).
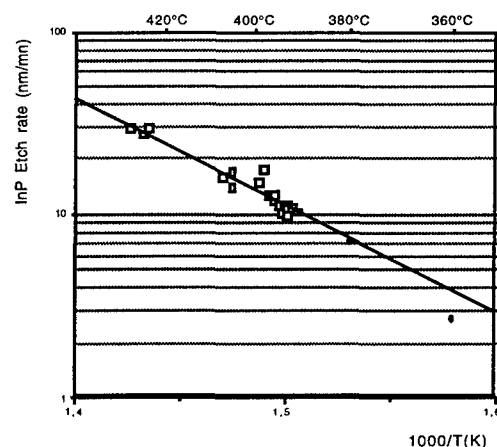
Fig. 1 : Etch rate for InP as a function inverse of temperature in the low temperature range.

618

For the application to laser stripe etching and regrowth, the knowledge and controle of etch profiles at mask edges is of prime importance. For that purpose, InP samples patterned with SiO_2 stripes oriented along the [011] and [01-1] directions have been prepared and *in-situ* etched. In the [011] direction, the profile is mostly determined by the very slow etch rate of the (111)B facet, compared to (100). This produces a characteristic mesa shape with very limited etching under the SiO_2 mask. This mesa shape is particularly well suited to regrowth by GSMBE or related techniques. Indeed, the very limited mask underetching and the external mesa shape produces no shadow effect during regrowth. Furthermore, the growth rate along the (111)B facet being also much slower than along (100), a nearly planar regrowth is observed around the mesa in the etched trenches (fig. 2). This feature is specific to the described technique, and makes regrowth around mesa structures more precise and controllable than with other techniques.
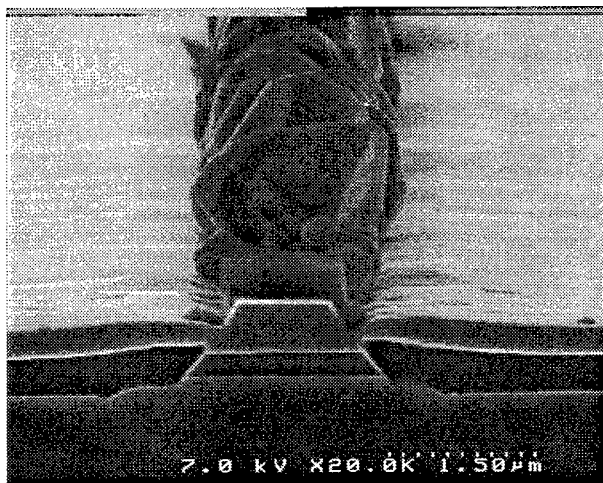
Fig. 2 : SEM view of *in-situ* etched mesa stripe regrown with p/n blocking layers.

III. Experimental

The test-devices used to evaluate the performances of the *in-situ* etching and regrowth process were FP 1.3μm or 1.48μm lasers of standard designs. The vertical structure of the lasers were grown by GSMBE in a first step. The active structures consisted of compressively strained InGaAsP QW's and lattice matched InGaAsP barriers. After SiO_2 mask patterning with standard lithography and etching techniques, mesa etching and blocking layer regrowth was performed with the new *in-situ* process, as described above. The regrowth process being non selective, polycristalline deposit is found on the SiO_2 mask after the etch and regrowth step, as can be seen on figure 2. The polycristalline material is easily lifted-off during the SiO_2 mask removal. A final regrowth step, performed by GSMBE or MOVPE, completes the whole BH laser structure (fig. 3).

Further processing steps follow the standard Buried Ridge Stripe laser technology flow-chart: p contact metalisation, proton implantation for isolation, wafer thining, n contact metalisation.
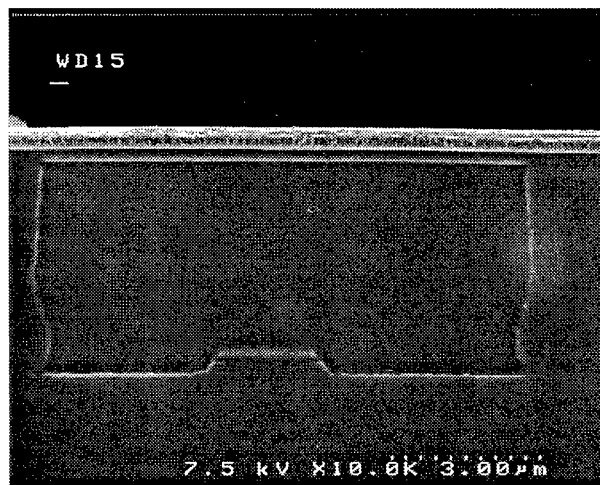
Fig. 3 : SEM view of pn-BH laser stripe after SiO_2 mask lift-off and final MOVPE regrowth step.

Fabrication of different BH laser structures, such as BRS or pn-BH, are possible and have been demonstrated with the *in-situ* etching and regrowth technique. In the case of the laser results discussed in this work, lasers had a simple BRS structure, and final regrowth step was performed by MOVPE.

IV. Laser results and discussion

Preliminary results showed high threshold current values, in excess of 20 mA at room temperature for PF 1.3μm lasers of 300 μm long with cleaved facets. This rather high threshold currents were due to a high lateral junction leakage, as confirmed on test structures. An optimization of the laser structure has been necessary to solve that problem. On figure 4, the threshold current of PF 1.3μm lasers prepared by *in-situ* etching and regrowth is represented as a function of the nominal Silicon doping level in the InP buffer layer.

A good correlation is found between threshold current and Si doping level. For Si doping values higher than $2x10^{17}$ cm^{-3}, the threshold current is found to increase very rapidly with increasing Si doping level. For Si doping values equal or lower than that value, the threshold current is found constant at values around 10 mA. This threshold current value is typical for that structure and the stripe dimensions used.

The detrimental effect of Si buffer layer doping level on laser performances is most probably due to surface accumulation of Si during etching in the buffer layer. Indeed, it has been shown in a previous work (4) that Silicon, for which volatile chlorides are not formed in the normal etch conditions, is not etched at all and is accumulated at the surface during etching and buried after regrowth. When etching a Si doped InP layer, to the precision of the SIMS analysis, 100% of the Si dose present in the etched layer is found at the etch/regrowth interface as a δ–doped layer. This leads to a very high Si

619

interface concentration of about 5×10^{13} cm^{-2} in the usual etch conditions: (nominal Si doping level 2×10^{18} cm^{-3}, etch depth 0.25 μm).
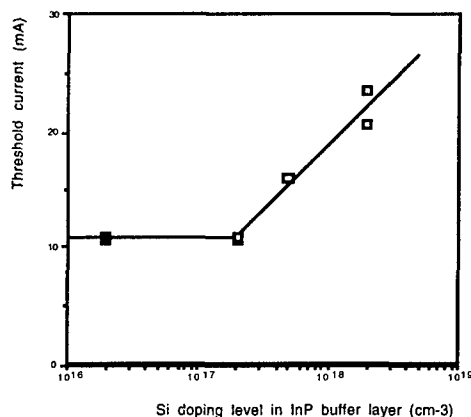
Fig. 4 : Threshold current of PF 1.3μm lasers (L=300μm, cleaved facets) as a function of InP buffer layer Si doping level.

This δ-doped Si layer present at the etch/regrowth interface is responsible for the increase of lateral junction leakage current, and in consequence, for the increase in laser threshold current. For Si doping levels equal or lower than 2×10^{17} cm^{-3}, which corresponds to interface concentrations equal or lower than about 5×10^{12} cm^{-2}, the lateral leakage current due to the Si interface layer becomes negligible and the threshold current saturates at a low value.

This result points out the impact of interface contamination on lateral junction leakage and laser performances, and sets a maximum limit at about 5×10^{12} cm^{-2} for Silicon interface concentration. If this condition is satisfied, very good performances are obtained for both 1.3μm and 1.48μm PF laser structures.
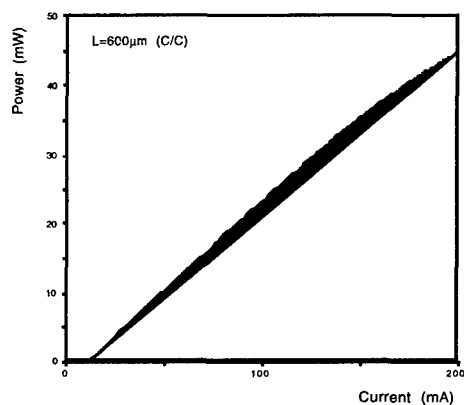
Fig. 5 : P(I) characteristic of PF 1.48μm laser, device length 600μm, cleaved facets.

The P(I) characteristic of a 1.48μm PF laser, 600 μm long with cleaved facets, is given on figure 5.

Threshold current and differential efficiency are comparable to the best results obtained on lasers processed with conventional techniques. A linear P(I) characteristic is obtained up to about 150 mA, confirming the very low value of lateral p/n junction leakage current. At higher driving current, the emitted power saturates, as for conventional BRS lasers.

Preliminary lifetest results have shown that BH lasers prepared with this new *in-situ* etching and regrowth technique are extremely stable in hard burn-in test conditions.

V. Conclusion

A first demonstration of device fabrication with the new *in-situ* etching and regrowth technique has been made. Well defined mesa profiles and excellent regrowth morphologies have been obtained. The effect of interface contamination has been pointed out, in particular for the case of Silicon for which a direct effect on laser results has been shown. In spite of this problem, excellent performances have been obtained for both 1.3 and 1.48μm PF lasers. All these results demonstrate the performances of this combined *in-situ* processing technique and open the way to a larger range of applications.

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BUTT-COUPLED WAVEGUIDE-MODULATORS BY LOW TEMPERATURE EMBEDDED CBE REGROWTH FOR HIGH SPEED MODULATION (42GHZ) OR LARGE EXTINCTION RATIO (>50DB)

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Introduction

The monolithic integration of optical waveguides with various active photonic devices is an essential step towards the fabrication of complex photonic integrated circuits (PICs). This integration requires on the same substrate side by side planar areas of usually thick (around 3µm) InP/GaInAsP/InP double heterostructure (DH) with wide differences in bandgap and doping level between the low loss waveguide and the active device. Such different material properties across the wafer can be obtained by a multi-step epitaxial process using embedded selective-area epitaxy [1].

We demonstrate in this study that selective-area chemical beam epitaxy (SA-CBE) offers several interesting features for this application: (i) a low regrowth temperature (around 500°C) which minimizes thermal degradation of the initial device structure especially when it contains strained quantum wells and fast diffusing dopants, (ii) a perfect growth selectivity into deep grooves (≥ 3µm) with a planar surface and with reduced overgrowth at mask edges and (iii) efficient butt-coupling free of air gaps between the waveguide and the device active layer [2,3]. We have successfully applied this technique to the selectively embedded regrowth of a waveguide butt-coupled to multi-quantum well (MQW) electroabsorption (EA) modulators. Two integrated modules have been fabricated and characterized: (a) a photonic circuit including two modulators optically connected through a waveguide to generate short optical pulses with a large extinction ratio (>50dB) for optical temporal multiplexing up to 80Gb/s and (b) a very short (L=50µm) discrete modulator with waveguides integrated on both ends showing high modulation bandwidth (42 GHz).

I Experimental

A InP:Si / undoped MQW / InP:Zn modulator structure is first grown by MOVPE on n-type (100) nominal InP substrate. The 300nm thick active layer consists of 13 lattice-matched GaInAsP (λ=1,57µm) / GaInAsP (λ=1,15µm) quantum wells [4]. Part of this wafer is processed to record the reference performances of the modulators. The rest of it is covered with a SiN$_x$ mask deposited by plasma-enhanced chemical vapor deposition (PECVD). The conventional photolithography followed by SF$_6$ reactive ion etching (RIE) is just employed to define [0-11] oriented stripe-shaped windows in the nitride mask. Next using CH$_4$/H$_2$ RIE, the semiconductor structure is etched down to the lower InP cladding layer to realize 2.5 to 3µm deep grooves with vertical sidewalls. Prior to regrowth, the RIE surface damage is removed by a slight chemical etching with equivalent etch rates on InP and GaInAsP. Subsequently, an undoped InP (535nm) / GaInAsP (350nm, λ=1.27µm) / InP (1320nm) DH waveguide structure is selectively regrown by CBE into the grooves. The two group III precursors trimethylgallium (TMGa) and trimethylindium (TMIn) are injected together normal to the wafer to minimize the lateral growth on the sidewalls [5]. Pure arsine and phosphine are used as group V sources. A constant growth temperature of 508°C and a growth rate close to 1µm/h for both materials are used. Finally, [011] oriented stripes are defined by dry etching through the modulator and the regrown waveguide areas. Ti/Au ohmic contacts are deposited on top of the modulators.

Fig.1 shows the tilted SEM micrograph of the view of a part of an integrated module including regrown waveguides on both ends of a modulator.
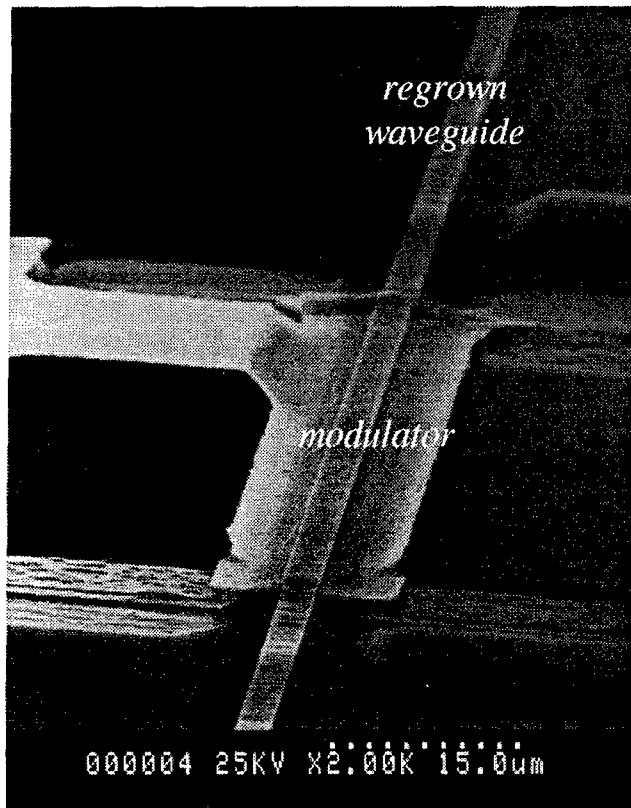
Fig 1. Tilted SEM micrograph view showing a part of the modulators tandem

II Results

II.1 Characterization of SA-CBE regrowth

The CBE growth selectivity of InP and GaInAs(P) is found to be dependent on the mask composition and quality. In the present case, the optimized growth temperature (508°C) of high quality InP/GaInAsP heterostructure is close to the critical temperature for selective growth above which no deposition occurs on the SiN$_x$ mask [3]. Furthermore, the mask quality is degraded during the RIE processing of the semiconductor. Indeed, during this step the nitride is directly in contact with the plasma. Thus, the damaged mask favors nucleation on its surface during selective regrowth. To overcome this problem, the nitride mask is protected during RIE by a Mn film deposited on the SiN$_x$ mask. Subsequently, the Mn mask is removed during the desoxydation step of the semiconductor surface prior to regrowth.

The scanning electron microscopy (SEM) cross-sectional view of the embedded SA-CBE regrowth of the waveguide structure is shown in Fig.2a. One can observe here a perfect growth selectivity with no deposition on the surface of the mask coating the modulator. A planar filling of the groove is obtained despite its 3μm depth. The butt-joint in the direction of light propagation shows a good alignment, free of air gaps, between the waveguide and the MQW modulator active layer. A lateral growth on the sidewalls can be deduced from the presence of a very thin vertical quaternary layer. Indeed, the vertical sidewalls are partially exposed to the incident molecular beams. The ratio of lateral to vertical growth rate is decreased to less than 15% in our experimental conditions because the group III precursors injection is perpendicular to the substrate surface [4]. Nevertheless, this lateral growth leads to the formation of a small overgrowth localized at the mask edge with dimensions similar to the thickness of regrown material [6]. As shown in Fig.2b such overgrowths as well as residual nucleation on the mask can be easily removed during the nitride mask elimination.

Our earlier investigations by spatially resolved photoluminescence measurements of selectively grown embedded DH have shown a good composition uniformity of GaInAsP waveguide close to the sidewall independent of the substrate mask coverage [3].
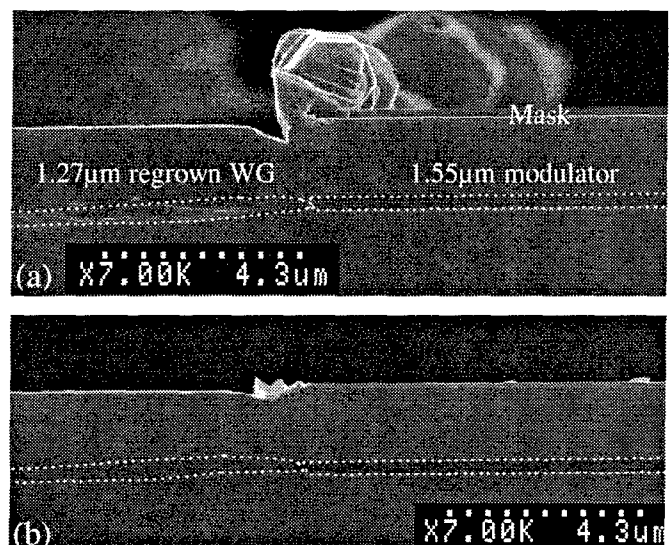
Fig.2. Embedded SA-CBE of InP/GaInAsP DH waveguide in a 3μm deep groove etched into the modulator structure covered by the nitride mask : SEM micrograph cross-sectional view (a) after waveguide regrowth and (b) after mask removal.

II.2. Characterization of butt-coupled waveguide and modulators

The electro-optical characteristics of modulators before and after waveguide regrowth by SA-CBE are compared in Fig.3. Thanks to the low temperature of the regrowth process, we see no drastic degradation of the extinction ratio characteristics after regrowth.
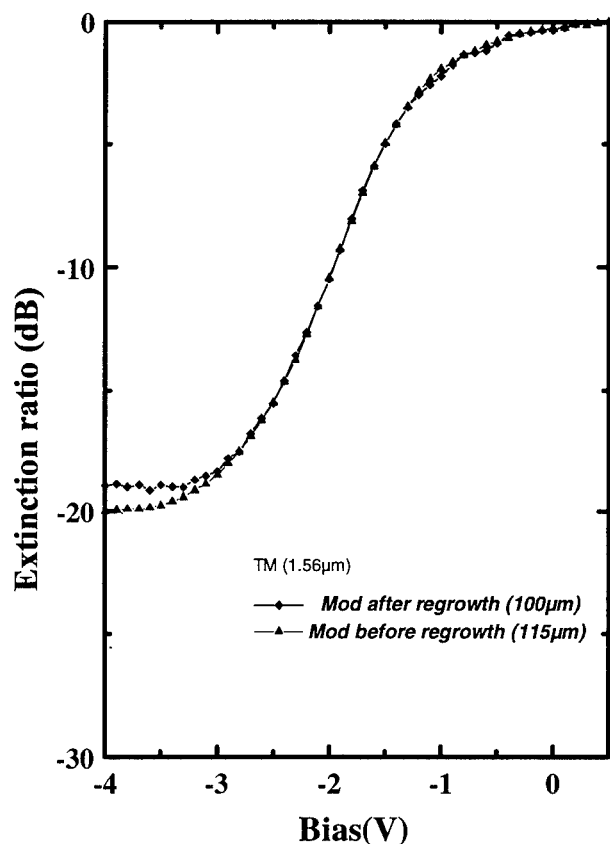
Fig.3. Extinction ratio characteristics versus applied bias of a modulator (L=100μm) after waveguide regrowth compared to a reference modulator (L=115μm)

Two integrated modules consisting of butt-coupled waveguide and modulator have been fabricated and characterized. In the first example as shown schematically in Fig.4 (integrated module a), a photonic circuit containing two modulators (148μm long each) optically connected through a 500μm long waveguide has been realized to obtain a large extinction ratio for the generation of short optical pulses. In the second example, reported in Fig.5 (integrated module b), a very short (L=50μm) discrete modulator has been integrated with two lateral waveguides (300μm long each) to improve the modulation bandwidth. Indeed, the modulation speed of an EA modulator is limited by its capacitance and consequently an improvement of its performance can

be obtained simply by decreasing the device length. However the fabrication of small length devices by cleavage and their connection to optical fibers cannot always be easily achieved. On the contrary, the present integrated module is long enough (650μm) for fabrication as well as for packaging while keeping a short modulation region.

Optical characterization using the TM polarized laser light yields a fiber to fiber loss of 15 and 11dB for integrated modules a and b, respectively. A loss of 1,4dB / butt-joint is deduced from similar experiments with a reference modulator.

The electro-optical characteristics of a tandem of modulators (module a) is shown in Fig.4. A very high

Integrated module (a)
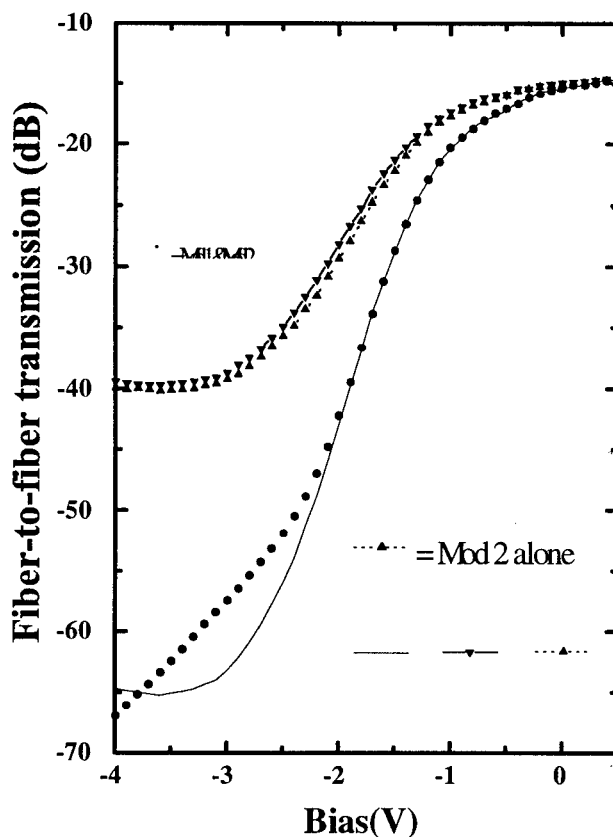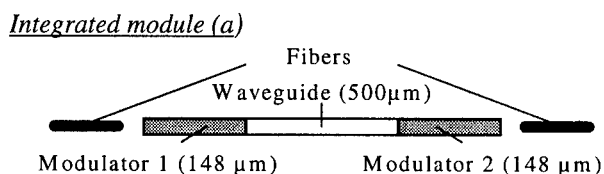
Fig 4: Extinction ratio of a modulator tandem versus applied bias: characteristics of each modulator separately operated (up and down triangles) and of the two modulators operated together (circles). The solid line represents the sum of the extinction ratio curves of each modulator.

extinction ratio (>50dB) is measured when the two modulators are simultaneously operated. The experimental extinction ratio characteristic of the modulator tandem is very close to the theoretical curve (full line) calculated by summing the extinction ratios of the two modulators for the same polarization. Such high modulation depth performance is particularly important when EA modulators are used for the generation of short optical pulses with low background intensity in optically time division multiplexed (OTDM) systems.

The frequency response of the short modulator integrated with its lateral waveguides (module b) is shown in Fig.5. The experimental bandwidth defined by a fall of electrical 3dB from the base line is as high as 42 GHz.

Integrated module (b)

Waveguides (300 μm)

Modulator (50 μm)
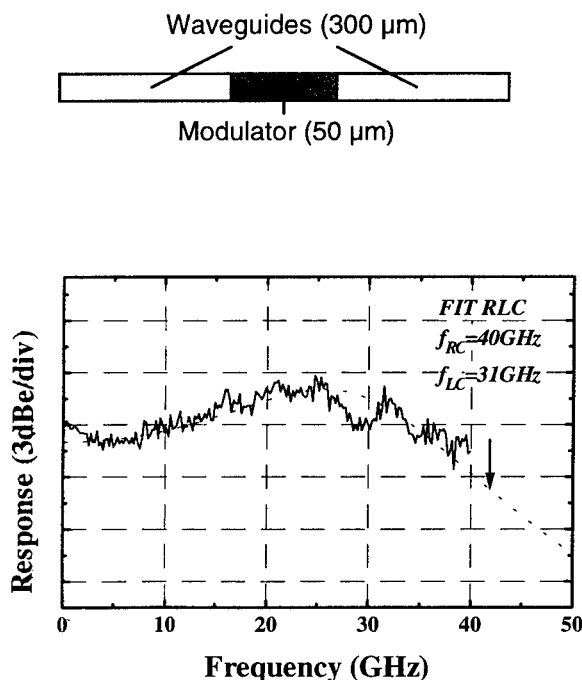
Frequency (GHz)

Fig.5. Frequency response of the 50μm modulator-waveguide. The modulator is 2,5V reverse biased and the optical input power at the facet is 0 dBm.

III Conclusion

We have shown in this study that SA-CBE is well suited to the embedded regrowth of thick undoped waveguide structures butt-coupled to active photonic devices. As demonstrated by the two examples of integrated modules, this technique permits to realize planarized surfaces to ease the subsequent technological processing of photonic circuits. Besides,

it helps to grow butt-joint free of air gaps showing high coupling efficiency between the regrown waveguide and the device active layer. Most importantly, the low regrowth temperature close to 500°C keeps the initial device performances unchanged. This technique has been successfully applied to the integration of a short EA modulator with waveguides to improve modulation bandwith up to 42 GHz. Also a large extinction ratio higher than 50dB has been measured on a tandem of modulators optically connected through a regrown waveguide.

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624

Monolithic InP HEMT/HBT Integrated Circuit Technology by Selective Molecular Beam Epitaxy

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Introduction

InP-based HEMTs and HBTs have demonstrated superior characteristics over GaAs-based technologies at the device and integrated circuit levels, including record millimeter-wave performance for low noise amplifiers, power amplifiers, oscillators and mixers [1-4]. The ability to incorporate high quality InP HEMTs and HBTs monolithically allows each transistor technology to be matched to its optimal function without the need for expensive multi-chip packages or bandwidth limiting interconnect bondwires. High frequency monolithically integrated transceivers such as those required for anti-collision radar and wireless LANs would be possible at reduced size and cost while offering better performance than present hybrid or single technology solutions.

I. Growth and Fabrication

The creation of the active InP HEMT and HBT regions was achieved by selective epitaxy on 2 inch SI InP substrates in a conventional solid source MBE reactor using Si and Be as n- and p-type dopants, respectively [5]. Selective epitaxy avoids the stacked or shared layer approaches for integrating multiple device technologies which inevitably compromise the performance of one or more of the devices. The InP HBT layers were grown first at a nominal substrate temperature, T_{sub}=500°C. Using a patterned PECVD Si_3N_4 mask, the HBT material was etched for the HEMT layer regrowth. Following regrowth, the polycrytalline material deposited on the nitride was removed leaving HEMT and HBT islands. The growth order and conditions for both devices as well as the surface preparation prior to regrowth were optimized for best surface morphology and device characteristics [6]. Fig. 1 illustrates the two device technologies implemented on separately grown mesas while Fig. 2 details the fabrication sequence.

The InAlAs/InGaAs HBT structure features a linearly graded InGaAlAs emitter-base junction for low, stable V_{be}. The $1 \times 10^{16} cm^{-3}$ 7000Å InGaAs collector represents a compromise of breakdown voltage, current handling capability and f_t. The 800Å base is Be-doped at $3 \times 10^{19} cm^{-3}$ yielding a 460 Ω/sq sheet resistance. The 1μm minimum emitter geometry was realized with self-aligned emitter and base metals.

High Linearity HBT

Low Noise HEMT
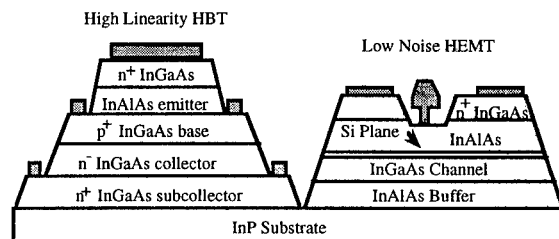
Fig. 1. Integrated InP HBT and HEMT Cross Section
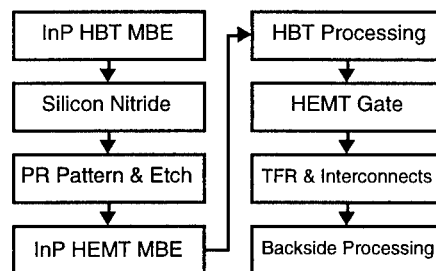
Fig. 2. Selective epi process flow diagram

The HEMT structure features a pseudomorphic InGaAs channel with 60% In and an InAlAs barrier with a Si planar-doped donor layer. This ensures a high channel aspect ratio and a high electron transfer efficiency. Typical sheet charge densities and 300K (77K) Hall mobilities for this profile are $3.5 \times 10^{12} cm^{-2}$ and 10000 (30000) cm^2/Vs. A source drain spacing of 1μm contains the TiPtAu 0.1μm Schottky T-shaped gate defined by electron beam lithography. AuGe ohmic contacts were alloyed through the InGaAs cap to access the channel region.
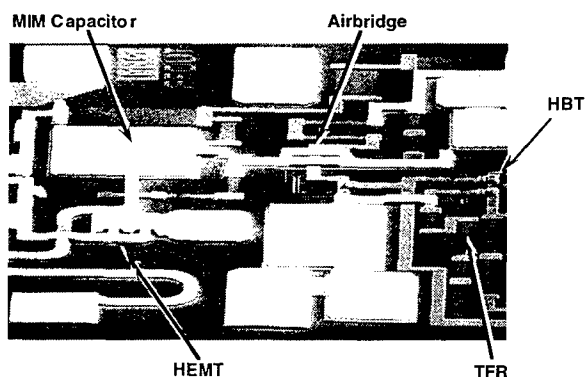
Fig. 3. Integrated circuit illustrating monolithic InP HEMTs, HBTs, airbridges and passive components.

Both devices were mesa etched down to the substrate for proper isloation and passivated with 1000Å of Si$_3$N$_4$ which provides a dielectric for the first interconnect level. A second level of thicker interconnect metal is used for the microstrip lines and airbridges. The wafers were then thinned and polished to a thickness of 4 mils and backside vias were etched and metalized to form the ground plane. The different devices technologies and the passive components are shown in Fig. 3.

II. Transistor Characteristics

The DC and RF characteristics were measured on microwave devices arranged in a coplanar pad layout. The DC characterisitcs for a 1x10µm^2 quad emitter InAlAs/InGaAs HBT and for a 0.15µm x 40µm T-gate InAlAs/InGaAs pseudomorphic HEMT are given in Figs. 4 and 5, respectively. The HBT exhibits a peak ß = 23, a $V_{be(on)}$=0.9V and a $V_{ce(os)}$=0.25V; while the HEMT provides a peak g_m=900mS/mm, I_{ds}(@g_{mp})=240mA/mm and a V_{gp}=0V. Note that the HEMTs exhibit no kink effect and pinch off completely, indicating excellent regrown material quality.

The RF characteristics were measured from 0.05-50 GHz on an HP8510 network analyser and no pad de-embedding was performed. The HBT provided f_t=56 GHz and f_{max}=135 GHz at moderate operating conditions of I_c=20mA and V_{ce}=2V. The 0.1µm x 200µm HEMT biased near peak g_m at V_{ds}=1V exhibited an f_t=173 GHz and an MSG=10dB at 50 GHz where stability was still conditional.
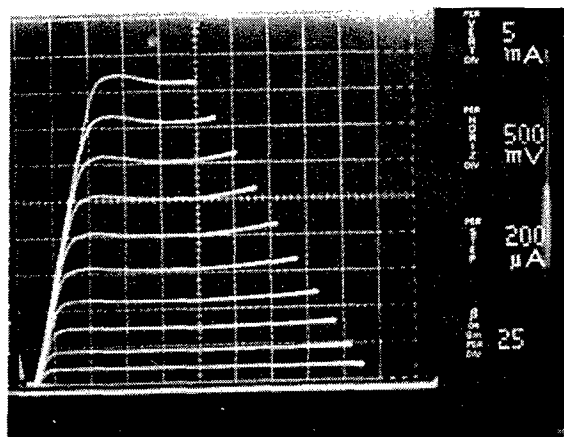
Fig. 4. Common-emitter characteristics for a quad emitter 1x10µm^2 quad InAlAs/InGaAs HBT.
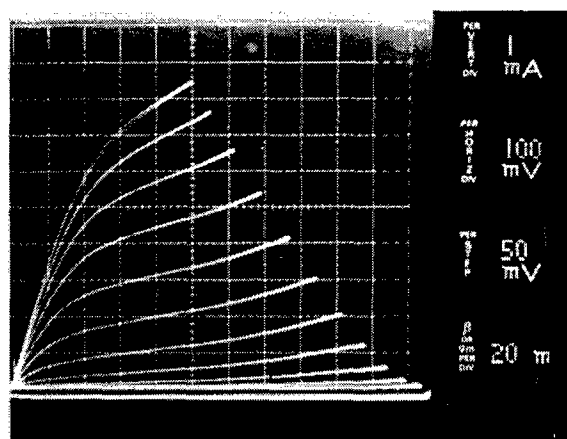
Fig. 5. Common-drain characteristics for a 0.1µm gate x 40µm InAlAs/InGaAs PHEMT.

III. Comparison with Standard InP Technologies

An important advantage of the selective epitaxy approach is that the device characteristics of the individual stand-alone technologies are preserved. Therefore, existing subcell and microcell libraries can be imported without changes. Table 1 illustrates the the various device parameters that characterize HEMTs and HBTs and compares these parameters in the monolithic HEMT-HBT technology with those in our standard individual technologies.

The parameters for the selective epitaxy HEMTs fall within the typical range of TRW's InP HEMTs. Figs. 6 and 7 show a distribution of peak g_m and f_t, respectively, on multiple sites from 2 wafers. The data suggests excellent uniformity over the 2-inch wafer. A slightly lower f_t is expected since the thicker SiN passivation shared with the HBT leads to higher parasitic C_{gs}. The reproducibility of peak g_m, peak I_{ds} and V_{gp} as well as the excellent surface morphology indicate that the regrown HEMT material

quality is comparable to that of TRWs standard profile.

The distribution of V_{be} and f_t for the selective epi HBT are shown in Figs. 8 and 9. The HBT shows 200mV higher V_{be} and lower f_t than in the standard technology due to Be diffusion out of the base during the HEMT regrowth. The amount of diffusion is estimated to be 250Å from the change in V_{be} leading to a thicker effective base and slightly lower ß and f_t. These effects can be alleviated by optimizing the growth conditions and profile structure.

Tech.	Parameter	Sel. Epi	Standard	Conditions
HEMT	g_m(mS/mm)	860	900	V_{ds}=1V
HEMT	I_{dsp}(mA/mm)	200	220	V_{ds}=1V
HEMT	f_t (GHz)	167	180	V_{ds}=1V
HEMT	V_{gp} (V)	0.0	0.0-0.2	V_{ds}=1V
HBT	V_{be} (mV)	610	420	I_c=1μA
HBT	ß	20	25	I_c=30mA
HBT	f_t (GHz)	52	60	I_c=20mA
HBT	f_{max} (GHz)	125	140	I_c=20mA

Table 1. Key parameter comparison with standard InP device technologies at TRW.
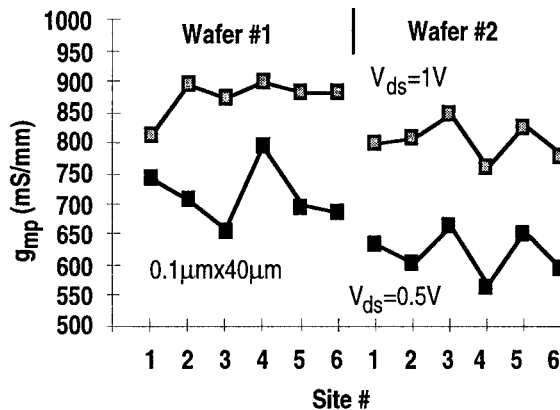
Fig. 6. Distribution of peak g_m for the 0.1μm gate InP HEMT with a 40μm gate periphery.
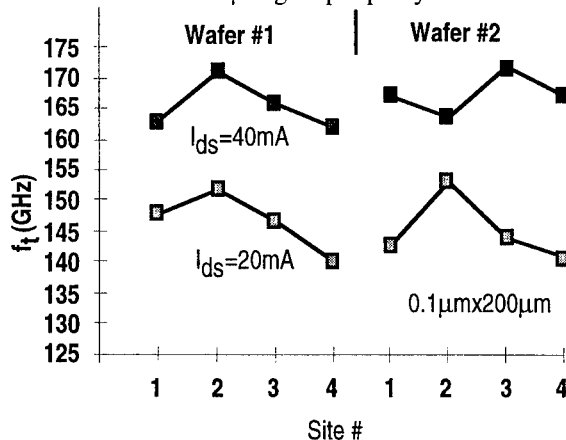
Fig. 7. Distribution of f_t for the 0.1μm gate InP HEMT with a 200μm gate periphery.
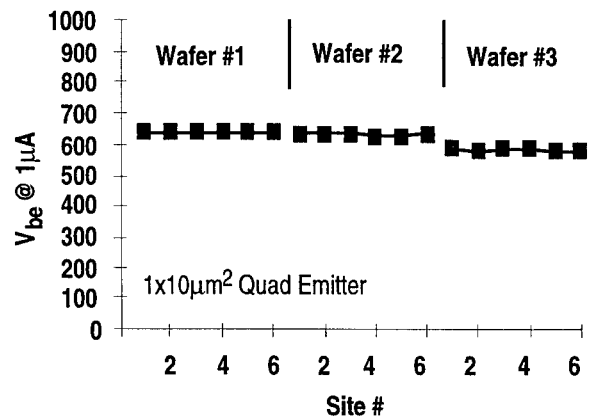
Fig. 8. Distribution of V_{be} for the 1x10μm^2 quad emitter InP HBT.
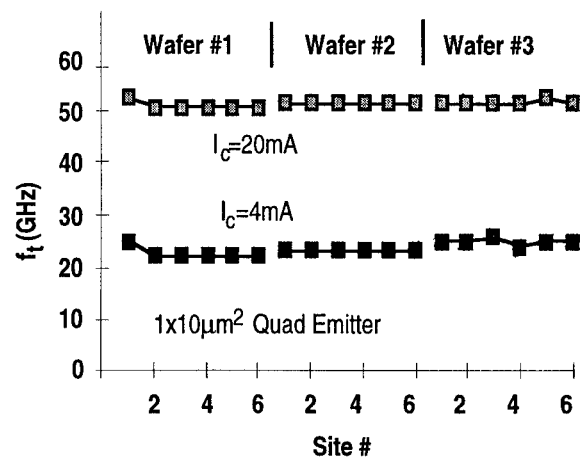
Fig. 9. Distribution of f_t for the 1x10μm^2 quad emitter InP HBT.

IV. Integrated Circuit Performance

A variety of different integrated circuits targeting millimeter-wave functions were implemented in selective epi technology. The 23 GHz HBT amplifier delivered >5dB gain while the 47 GHz HEMT amplifier offered >16dB gain. Fig. 10 shows a 94 GHz HEMT low noise amplifier with an HBT-based bias regulator. The single stage amplifier offers a noise figure = 4.8dB with 5.4dB gain at 94 GHz. Fig. 11 demonstrates the first InP-based integrated circuit that features active HEMTs and HBTs. It consists of a common-collector 23 GHz HBT tunable oscillator followed by a HEMT amplifier. Its spectral response given in Fig. 12 represents an output power of 1dBm. It is expected to provide ultra-low phase noise due to the low inherent 1/f noise in InP HBTs as compared to HEMTs and GaAs HBTs.

627

V. Conclusions

Co-integration of high performance InP HEMTs and HBT has been achieved using selective MBE. The merged device technologies maintain the performance of their stand-alone conterparts and show excellent yield and uniformity. The first monolithic integrated circuits featuring both InP HEMTs and HBT have been presented. The successful merging of these technologies on the same InP substrate represents a significant step towards larger scale millimeter wave integration and innovative system architectues.
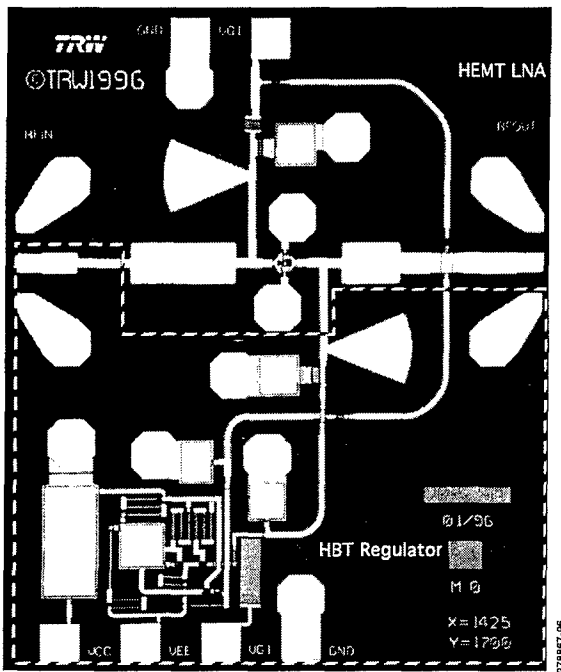
Fig. 10. 94 GHz InP HEMT low noise amplifier with HBT bias regulation.
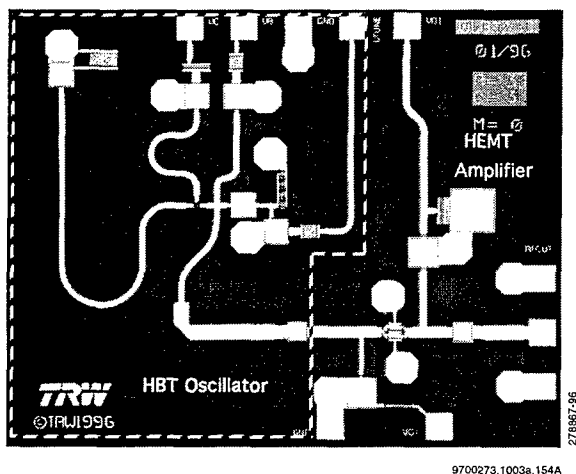
Fig. 11. 23 GHz InP HBT oscillator with a HEMT post amplifier.

Center 24.65 GHz   Span 100.0 MHz
RBW 1.0 MHz   VBW 10kHz   SWP 50.0ms
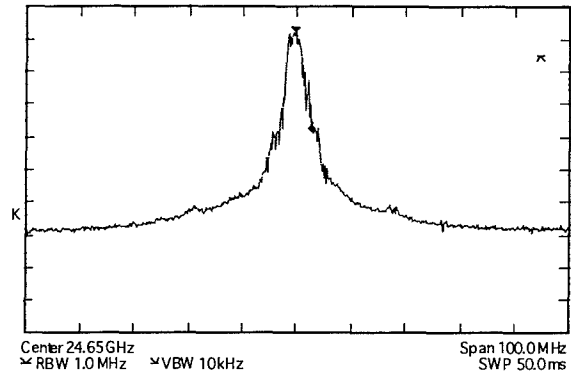
Fig. 11. 23 GHz InP HBT VCO with a HEMT amplifier.

VII. Acknowledgments

VII. References

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InP HBT TECHNOLOGY FOR HIGH SPEED CIRCUITS AND OEICs

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Introduction

Two areas currently motivate the efforts put into development of InP-based heterojunction bipolar transistors (HBTs). Due to excellent high speed properties and a DC-characteristic similar to conventional Si-based bipolars, it is an extremely interesting technique for fabrication of high speed integrated circuit prototypes. Further, since the device is based on the same material as, and has a structure similar to, optoelectronic devices used for optical communication, it is also an advantageous choice for optoelectronic integrated circuits (OEICs). The motivations for development of OEICs are potentially higher complexity and higher frequencies at a lower cost, as compared with hybrid solutions, but the main emphasis is on high frequencies at the research level, so the two areas have a common interest in developing high speed integrated circuits.

I. Background

An excellent application for InP-HBTs, requiring high speed, small to medium scale electronic as well as optoelectronic integrated circuits, is a 40-Gb/s optical communication system. An appropriate HBT-technology must fulfill several requirements to make realisation of a complete system possible:

- *High uniformity.* The optimum circuit complexity is a trade off between yield and performance. A high degree of integration reduces the number of high frequency in- and outputs, by that decreasing signal degradation due to bonding wires as well as power consumption caused by interface matching. However, it also limits the possibilities for individual adjustment of the bias point for smaller sub-circuits, increasing the demand for a uniform fabrication process.

- *High yield.* The largest blocks, i.e. 4:1 MUX, 1:4 DMUX, and clock recovery, consist of around 500 devices each, and even a yield of 99% for discrete devices amounts to less than 1% yield for a 500-device circuit.

- *Low power dissipation.* Low turn-on voltage and high cutoff frequencies at low currents are needed to allow dense packing. At least three times the maximum frequency of the analogue circuits is often required in practice. Depending on system requirements, this means more than 80 GHz for 40-Gb/s circuits.

- *A fabrication technique allowing for integration of optoelectronic components,* such as photodetectors and lasers.

II. The HBT structure

With increasing demands for improved performances, the epitaxial structure of an HBT becomes ever more complex, requiring advanced epitaxial techniques to be employed. Today, both MOCVD and different types of MBE-techniques are used for growth of the HBT-structures, but the low growth temperature required in MBE-growth is favourable, reducing diffusion broadening of the heavily doped base layer, and by that facilitating both uniform characteristics and excellent high speed performances.

Employing gas-source or solid-source MBE techniques (GSMBE and SSMBE, respectively) makes it possible to use InP for the emitter layer, offering a favourable energy band structure, as compared with AlInAs used in conventional MBE-growth. Although the energy bandgap of InP is smaller, the alignment to InGaAs is advantageous (Table 1), resulting in a better hole barrier and a lower electron barrier at the heterointerface (larger ΔE_V and lower ΔE_C, respectively).

As in conventional MBE growth, standard effusion cells supply the fluxes of indium and gallium, as well as the n- and p-type dopants silicon and beryllium. The two methods are distinguished by the techniques to supply and adjust the fluxes of As_2 and P_2. Separate valved cracker cells loaded with elemental arsenic and red phosphorus are employed in SSMBE, while provided by high-temperature cracking of phosphine and arsine

Table 1. *Energy bandgap (E_g), valence band discontinuity (ΔE_V), and conduction band discontinuity (ΔE_C) for several HBT compounds. All values in [eV].*

	AlInAs/ InGaAs	InP/ InGaAs	AlGaAs/ GaAs
$E_{g,emitter}$	1.48	1.35	1.86
$E_{g,base}$	0.76	0.76	1.43
ΔE_V	0.24	0.34	0.15
ΔE_C	0.48	0.25	0.28
$E_{g,base} + \Delta E_C$	1.24	1.01	1.71

in GSMBE. Both techniques have proven successful, but SSMBE grown material was chosen for the devices presented here. The epitaxial structures where grown on 2" SI (100) InP-substrates, at a growth temperature below 500°C.

A high electron velocity through the base may be beneficial for both the transit frequency and the current gain, and is often achieved by employing the conduction band spike as a launching ramp. The resulting quasi-ballistic transport is not believed to be sustained through the entire base width, though, and the base transit time (τ_b) is less than 0.1 ps for high speed HBTs even for non-ballistic transport, which is almost negligible considering the cutoff frequencies. The large hole barrier facilitates a high emitter injection efficiency, so the current gain is limited by recombination in the base layer due to an extremely short electron life time in the heavily p-doped base. In spite of the high doping density, the electron life time (τ_n) is around 15 ps, by that offering a current gain $\beta = \tau_n/\tau_b \approx 150$. An important drawback using this technique is an increase in the turn-on voltage. Approximating the HBT as a narrow diode, and neglecting all parasitics, the collector current characteristics can be written as

$$ J_C = J_0 \cdot \exp\left[\frac{V_{BE}}{V_T}\right] \tag{1} $$

where $V_T = kT/q$ is the thermal voltage. The term J_0 includes the bandgap profile dependence of the collector current, according to

$$ J_0 = \frac{q \cdot D_n}{N_A \cdot w_B} \cdot N_C \cdot N_V \cdot \exp\left[-\frac{E_{g,base} + \Delta E_C}{V_T}\right] \tag{2} $$

where all notations have their usual meaning. From table 1, it can be seen that the threshold voltage for an abrupt heterojunction,

being proportional to the sum of $E_{g,base} + \Delta E_C$, is increased by more than 30% even for an InP-emitter, as compared with a graded junction. The launching ramp has therefore been sacrificed in favour of a possibility to reduce the turn-on voltage. A low-doped p-type spacer, or setback layer, is introduced between the emitter and the base. It is wider than needed to allow for the diffusion broadening of the base layer, so a part of it remains low-doped. The depleted spacer decreases the conduction band spike at the cost of a deeper notch on the emitter side of the base, but it is found possible to do so without increasing the interface recombination to an unacceptable degree.

III. HBT fabrication

Two of the most difficult steps in fabrication of high speed InP HBTs circuits are to achieve a reliable planarisation process and a self-aligned base contact for small-area devices. This is in sharp contrast to the more mature GaAs HBT process, where proton implantation is used to create a semi-insulating region outside the active areas, eliminating the need for planarisation and limiting the required self-alignment to two parallel sides only.

A. Planarisation

A silicon nitride (SiN) layer has been adopted for this purpose, with a thickness equal to the device height. It offers the possibility to connect all contact metals outside the active device area, very similar to the conventional GaAs technique. Through this method, the external parasitic capacitances are reduced, being important when scaling down the device area to reduce the collector current and by that the power dissipation. As shown in Fig. 1, cutoff frequencies of more than 80 GHz at only 0.2 mA have been obtained using this technique.
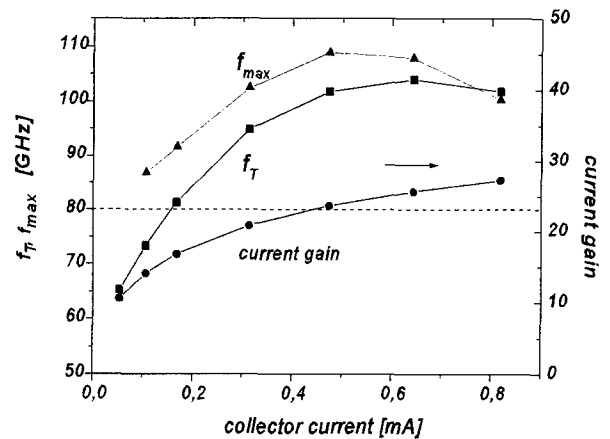
Fig. 1. *Cutoff frequencies and current gain at $V_{CE} = 1.2$ V for an HBT with a nominal emitter area of $2.5 \cdot 2.5$ μm.*

630

B. Self-alignment

A self-aligned base contact metal reduces both base resistance (R_B) and base-collector capacitance (C_{BC}), and is also of vital importance to obtain uniform values. A critical step in self-aligned HBT fabrication is the required undercutting of the emitter metal, since the etch-rate is strongly crystal orientation dependent. Using the SiN-planarisation technique, it is possible to let the emitter metal overlap the active area, protecting both short sides of the rectangular mesa, that is, the sides not facing the base contacts, during emitter mesa formation. By aligning the two remaining sides in the [011] direction, the need for excessive etching is reduced. The SiN layer is then etched in a high-pressure CF_4-plasma in a subsequent step to extend the emitter mesa into the surrounding SiN-surface. Complete self-alignment is now possible due to uniform undercutting of the emitter metal outside the device, since the etch-rate of SiN is isotropic. The emitter area is thus defined by the size of the active device area in one dimension, and the width of the emitter metal in the other.

The maximum frequency of oscillation (f_{max}) is strongly related to R_B and C_{BC} through:

$$f_{max} = \sqrt{\frac{f_T}{8\pi\cdot\tau_{BC}}} \qquad (3)$$

where f_T is the transit frequency and $\tau_{BC} = R_B \cdot C_{BC}$. Two wafers including 40 devices with a nominal emitter area of 2.5·2.5 μm where evaluated, and the cutoff frequencies were $f_T = 94.7\pm2.6$ GHz, and $f_{max} = 95.1\pm4.4$ GHz, at a base current of 15 μA and a collector-to-emitter voltage of 1.2 V. Such uniform f_{max} values are a good verification of a successful self-alignment.

IV. Optoelectronic integration

When using InP HBTs for OEICs, techniques are also needed to integrate optoelectronic devices without sacrificing the HBT performances. The two most common OEICs are optoelectronic receivers and transmitters, introducing different demands both on the HBT design and the fabrication process.

A. Optoelectronic receivers

Photodetectors are readily obtained through the PIN-structure formed by the base-collector-subcollector region of an HBT. The thickness of the absorbing i-layer must be chosen as a compromise between speed and quantum efficiency, as shown in Fig. 2. It is reasonable to believe 28 GHz would be sufficient for 40 Gb/s transmission, which can be obtained using a 10 μm wide PIN-diode with a 0.7 μm thick i-layer, offering an internal quantum efficiency of 40%. The influence of an increased
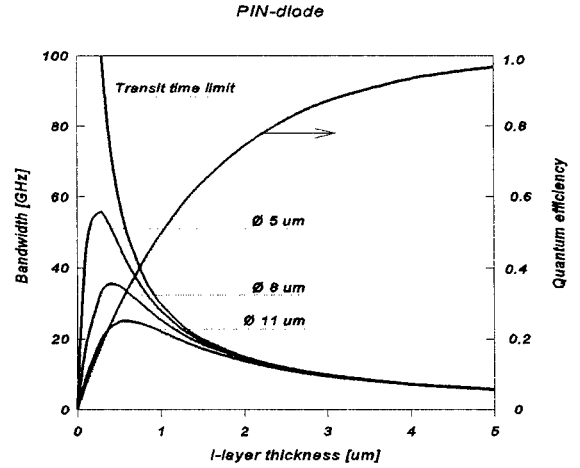
Fig. 2. Transit time delay and RC-delay for several pin-detector areas. The quantum efficiency is also shown.

collector thickness on the HBT properties is a slight decrease in the transit frequency, but an increase in the maximum oscillation frequency. As indicated in Fig. 3, the f_{max} to f_T ratio is almost three at a high bias voltage.
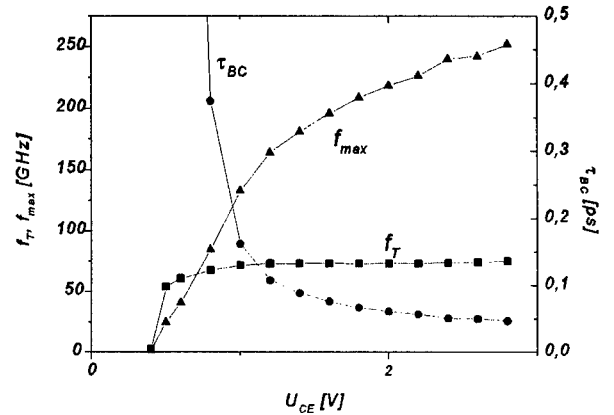
Fig. 3. Cutoff frequencies and base-collector time delay for a self-aligned HBT with 2.5·10 μm nominal emitter area, for a constant base current of 70 μA.

In addition to this, a barrier is needed in the collector-subcollector interface to prevent slow holes generated below the electric field from diffusing into the collector. This is achieved through a second heterojunction with a proper stepgrading on the collector side.

Optical receivers have been designed with a transimpedance front-end amplifier for several bitrates, some results are shown in Table 2. No modifications were needed in the fabrication process to include the HBT-based photodetectors. The discrepancy in the

bandwidth is partly due to the PIN-diode model, and should be possible to correct by a minor decrease in the thin film resistances.

Table 2. *Transimpedance, -3dB bandwidth, and sensitivity according to simulations and measurements for optoelectronic receivers, including a 10 μm PIN-detector with 0.3 A/W responsivity. The sensitivities are estimated from noise measurements, and the power dissipation was in the range 50 to 100 mW. *=approximate value.*

Bitrate Gb/s	Z_{trans} kΩ	BW GHz	P_{min} dBm	Z_{trans} kΩ	BW GHz	P_{min} dBm
	Simulated			Measured		
10	1.33	8.0	-21	1.39	7.7	-21
20	0.82	15	-17	0.86	14.2	-17
40	0.30	28	-12	0.32	24.5	-12*

B. Optoelectronic transmitters

Including high speed light emitters is more difficult than receivers, due to different vertical structures of an HBT and a laser, both regarding dimensions and material composition. Two techniques are currently being developed: Fabrication of the laser in trenches to achieve a planar surface, and selective conversion of the HBT-structure to a laser, as indicated in Fig. 4.
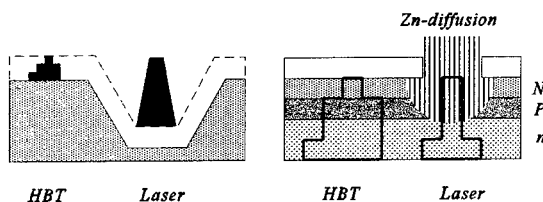
Fig. 4. Laser integration techniques: A trench grown laser to the left, and a converted HBT to the right.

In the first technique, the laser structure is grown on top of the HBT-structure on a patterned substrate, in one epitaxial run. The thick laser structure is then selectively removed outside the trenches. This method only puts demand on subsequent epitaxial regrowth not to degrade the HBT performance, ie, induce diffusion broadening of the base layer. It is found that a temperature below 550°C is required.

In the second method, the HBT-structure is designed according to a laser, and the top n-layer converted to p-type by zinc diffusion through openings in a silicon nitride cap. A current gain of 400 has been obtained for the HBTs, and the converted lasers offered a threshold current of 18 mA and a 3dB bandwidth

of 12 GHz.

Both methods have thus been successful, and the choice must be based on the application. Converted HBT lasers are preferred for higher complexities, ie arrays, and trench grown lasers for higher speeds. It can also be a choice between surface emitting lasers being convenient for the conversion technique, and edge emitting lasers that are more suited for the trench structure.

Looking at 40 Gb/s, the chirp associated with direct modulation of lasers motivates the use of external modulators. Such modulators require a higher bias voltage than the lasers, so HBTs used for the drivers would benefit from a higher breakdown voltage than the two volts regularly offered by single heterostructure transistors. Turning to double heterostructure transistors (DHBTs) would solve the problem since they can handle at least eight volts. The draw back of adopting this solution is that the collector no longer can be used as a photodetector, making integration of light emitters and detectors on the same chip impossible, and growing a third structure for the photodetector is not an attractive alternative. An increased voltage handling capability with a preserved possibility to fabricate PIN-diodes can be achieved by employing a heterostructure collector and a careful design of the collector doping profile.

A high speed laser can be treated as a resistive load of about five ohms, while the modulator is a capacitive load of only 0.5 pF. Independent of the chosen solution, high speed light emitters therefore require a relatively high drive current of 50 to 100 mA. This is a strong motivation to employ HBTs for the drivers, due to the excellent current handling capability.

V. Conclusions

Cutoff frequencies well above 100 GHz are readily available for discrete InP-HBTs today, expected to be sufficient for 40 Gb/s operation. Monolithic optoelectronic receivers are close to 40 Gb/s, and will probably offer this bitrate through further refinement. The monolithic transmitters are still limited to lower bitrates, although lasers have been fabricated with a bandwidth of 30 GHz. We believe high frequency operation of both IC and OEIC to be limited by an immature fabrication process and insufficient models for the active devices as well as the interconnections. The main effort will therefore be to increase the complexity level in the future, rather than the cutoff frequencies to even higher values. The goals will be yield and uniformity, which also are prerequisites for generation of reliable equivalent models for the design work.

A 277 GHz f_{max} Transferred-Substrate Heterojunction Bipolar Transistor

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Abstract

We report a AlInAs/GaInAs transferred-substrate Schottky-collector heterojunction bipolar transistor. A device with aligned 0.7 μm emitter and 1.6 μm collector stripes has extrapolated 277 GHz f_{max} and 127 GHz f_τ respectively.

I. Introduction

Heterojunction bipolar transistors have applications in medium-scale integrated circuits operating at GHz frequencies [1, 2]. Target applications include digital phase-locked loops for microwave frequency synthesis, chip-sets for fiber-optic transmission, and analog-digital converters. In these applications, both the transistor current gain cut-off frequency f_τ, and the power gain cut-off frequency f_{max} must be considerably higher than the signal frequencies involved. 100 Gbps optical-fiber transmission ICs will require HBTs having f_τ and f_{max} greater than 200-250 GHz [3, 4]. A second-order $\Sigma - \Delta$ analog-digital converter [5] having a 50 GHz sample rate would require HBTs with f_τ and $f_{max} \sim$ 200-300 GHz, but might provide 12 bits resolution at 1 GHz bandwidth. Broadband amplifiers [6] for 40 & 100 Gbps communication would require HBTs with similar performance. HBTs with bandwidths of several hundred GHz will benefit many similar applications.

While f_τ is primarily controlled by the thickness and transport parameters of the base and collector epitaxial layers, the product of the base resistance r_{bb}, and the collector-base capacitance C_{cb} is strongly determined by the widths of the emitter-base and collector-base junctions. Obtaining high $f_{max} \simeq \sqrt{f_\tau/8\pi r_{bb}C_{cb}}$ thus requires both vertical and lateral scaling of the device. We had earlier reported HBTs fabricated in a substrate transfer process [7, 8]. The process allows fabrication of narrow emitter and collector stripes on opposing sides of the base epitaxial layer [9]. $r_{bb}C_{cb}$ becomes proportional to the process minimum feature size, and f_{max} will increase rapidly with submicron scaling.

In our earlier work, the transistor epitaxial layers were directly attached to the transfer substrate by epoxy. Because of the poor thermal conductivity of the epoxy, this demonstration process was unsuitable for IC fabrication. Here we report improved tranferred-substrate HBTs with f_{max} = 277 GHz and f_τ = 127 GHz. These devices have 0.7 μm emitter width and 1.6 μm collector width. They were fabricated in a new substrate transfer process providing improved thermal performance. With small modifications, the process can be used for fabrication of medium-scale HBT ICs operating at high frequencies.

II. Fabrication

The HBT epitaxial layer structure (fig. 1b) is grown by molecular beam epitaxy on a Fe-doped semi-insulating (100) InP substrate, starting with a 1000 Å AlInAs buffer layer and two sacrificial 1000 Å GaInAs and AlInAs etch-stop layers. The GaInAs collector is 3000 Å thick, is Si-doped at $1 \times 10^{16}/cm^3$ and contains a $5 \times 10^{11}/cm^2$ Si pulse-doped layer 400 Å from the base. This pulse-doped layer delays the onset of base push-out [10]. The 500 Å GaInAs base is Be-doped at $5 \times 10^{19}/cm^3$. This is graded in 300 Å to the AlInAs emitter. The first 67 Å of the grade is Be-doped at $2 \times 10^{18}/cm^3$ and the remainder is Si-doped at $8 \times 10^{17}/cm^3$. The emitter ohmic contacts are to an InAs cap layer.

Fig. 1a shows a schematic cross-section of the device. The fabrication process starts with the evaporation of Ti/Pt/Au emitter contacts. A combination of a dry etch, a selective wet etch, and a non-selective wet etch is then used to etch down to the base epitaxial layer. Self-aligned Ti/Pt/Au base metal is evaporated and sintered at 300 °C for 1 minute. Transistors are then isolated by forming mesas using a dry etch, stopping on the AlInAs layer. The devices are passivated and planarized by polyimide, and the emitters contacted by electroplated Au airbridges. To this point, the process is similar to [1].

The substrate transfer process starts with the deposition of a 5000 Å SiN layer by PECVD. The wafer is then coated with 13 μm of Benzocyclobutene (BCB,
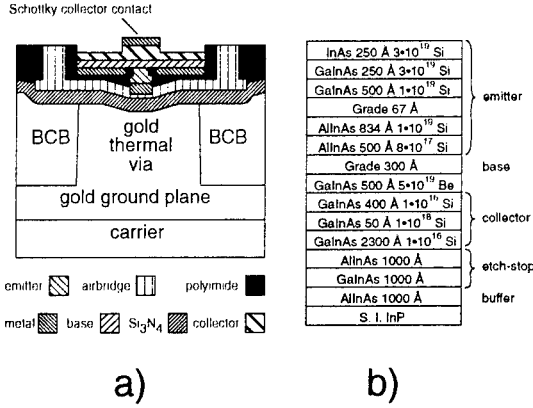
Figure 1: *a) Schematic cross-section and b) layer structure of the device.*
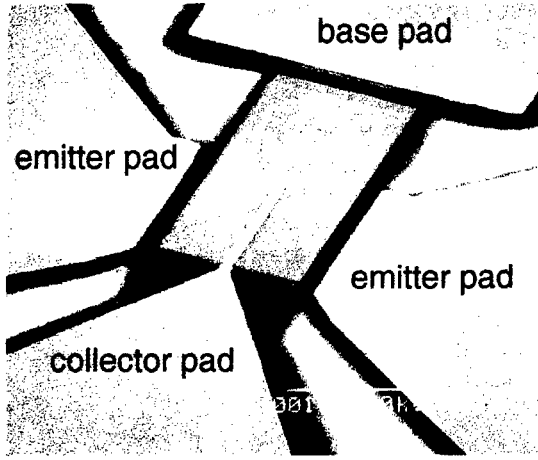
Figure 2: *Electron micrograph of a transferred-substrate HBT.*

Figure 3: *DC commom-emitter characteristics of a device with a 0.7 × 25 μm^2 emitter and a 1.6 × 29 μm^2 collector.*

$\epsilon_r = 2.7$). Thermal vias are formed by dry etching openings in the BCB and then filling them with thick Au by electroplating. This also forms an electrically and thermally conducting ground plane, thus grounding all emitters.

Transistors with non-grounded emitters (required in ICs) can also be fabricated by protecting the insulator layer during the via formation etch. SiN has $\epsilon_r = 6$ and $\sim$ 10-30 W/m-K thermal conductivity. For a HBT with a 0.7 × 25 μm^2 emitter, the thermal via is 10 × 24 μm^2. For non-grounded emitter devices, the calculated capacitance from the emitter airbridge to the grounded substrate is 25 fF, which is much smaller than 570 pF base-emitter capacitance. The calculated 67-200 K/W thermal resistance of the SiN layer should result in less than 3.5 °C additional temperature rise for a device biased at 10^5 A/cm^2 and 1.0 V.
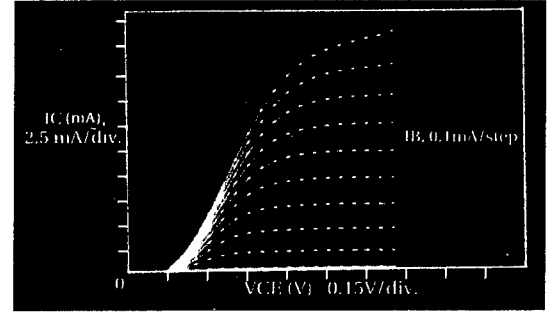
The wafer is then inverted and bonded to a GaAs transfer substrate. In the devices here reported, the bond was formed with die-attach epoxy. Presently we are processing devices with the bond formed by a In/Pb/Ag solder and with an n$^+$-Si transfer substrate. The InP substrate is removed by a selective wet etch, the GaInAs etch-stop layer by a non-selective etch and the AlInAs by a selective etch. Ti/Pt/Au Schottky collector contacts are then deposited. Outside the active collector area, 1500 Å of the collector drift region is then removed by a self-aligned wet etch. Fig. 2 shows a photomicrograph of a completed device.

III. Measurements

Fig. 3 shows the DC common-emitter characteristics. The small signal current gain at dc (β) is 27. BV_{ceo} is $\sim$ 2 V, decreasing to 1.5 V at 10^5 A/cm^2.

The devices were then charactrerized by on-wafer network analysis to 40 GHz. Fig. 4 shows the short-circuit current gain h_{21}, and Mason's [11] unilateral power gain U for a device with a 0.7 × 25 μm^2 emitter and a 1.6 × 29 μm^2 collector. The device is biased at $I_c = 14$ mA and $V_{ce} = 1.0$ V. Extrapolating at -20 dB/decade, $f_{max} = 277$ GHz and $f_\tau = 127$ GHz. The high f_{max} is due to the reduced $r_{bb}C'_{cb}$ time constant due to low resistance base ohmic contacts and the low intrinsic collector-base capacitance.

We have used Mason's gain for extrapolating f_{max} because of its characteristic -20 dB/decade slope, its independence of the transistor configuration (commom-base vs. common emitter), and its independence of pad inductive and capacitive parasitics.

From measurements of $(1/2\pi f_\tau)$ vs. emitter current density, it is determined that $\tau_{base} + \tau_{collector} =$

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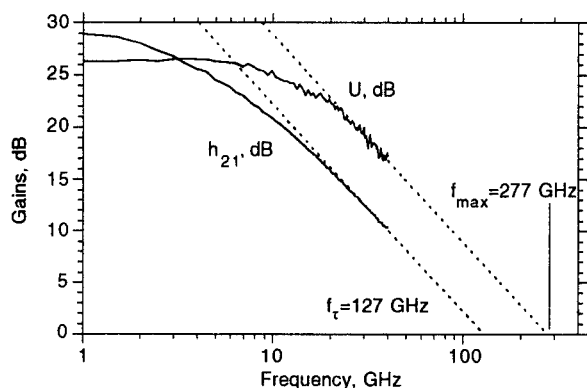
Figure 4: *RF characteristics of a device with a* 0.7×25 *μm^2 emitter and a 1.6×29 μm^2 collector, biased at* $I_c = 14$ *mA and* $V_{ce} = 1.0$ *V.*
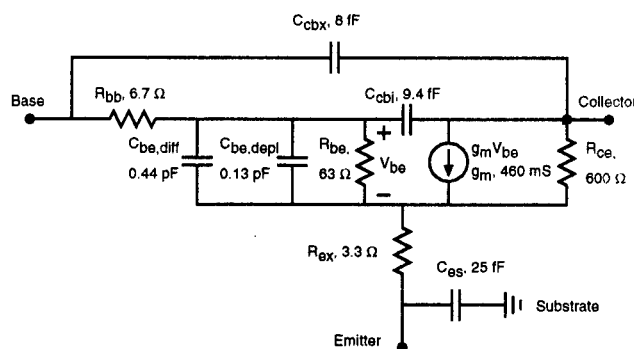
Figure 5: *Hybrid-pi model of device with 0.7×25 μm^2 emitter, 1.6×29 μm^2 collector, $I_c = 14$ mA and $V_{ce} = 1.0$ V.*

0.95 ps. A hybrid-pi model of the device is extracted from measured S-parameters at varying bias conditions (fig. 5). The pad parasitics are negligible.

IV. Conclusions

We have demonstrated transferred-substrate Schottky-collector emitter-up AlInAs/GaInAs transistors. These devices exhibit a β of 27, a f_{max} of 277 GHz and a f_τ of 127 GHz. With the replacement of die-attach epoxy with In/Pb/Ag solder and the GaAs substrate with Si, the process is suitable for integrated circuit fabrication. Further dimensional scaling of the device should lead to progressive improvement in transistor bandwidth.

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PASSIVATION OF INP-BASED HBT'S
FOR HIGH BIT RATE CIRCUIT APPLICATIONS

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Introduction

A large amount of work has been devoted recently to InP/InGaAs Heterojunction Bipolar Transistors (HBT's), with OEIC's in perspective. Very high microwave performances have already been reported [1]. For circuit applications, an important step in the InP HBT fabrication process is planarization, since device isolation is most commonly realized by mesa etching, which leads to rather thick devices and structured wafer surfaces. However, the planarization step imposes the deposition of a passivating layer, and device passivation is still a difficult issue for InP HBT's. The dielectric materials commonly used for passivation are silicon nitride or oxide, but they have been shown to generate important degradation on the electrical characteristics of InP-based HBT's [2, 3]. In this paper, we study the influence of various materials (SiN_x, SiO_2, polyimide), and deposition techniques (PECVD, UVCVD, spin coating) on the static characteristics of the HBT, and present device and circuit performances obtained with polyimide passivation.

I. How to characterize the effect of the passivation layer?

In order to evaluate the influence of a passivation layer on the static performances of the device, we have defined a quality factor, G, given by:

$$G = \frac{A_{p.}}{A_{u.p.}} = \frac{\int \beta_{passivated\ HBT}\ d(log(Ic))}{\int \beta_{unpassivated\ HBT}\ d(log(Ic))} \quad (1)$$

where β is the current gain of the device (Ic/Ib). Figure 1 shows a typical representation of the gain versus the collector current which is obtained from Gummel plots. The factor G is the ratio between the area below the $\beta(Ic)$ curve of the passivated device (A_p) to that of the unpassivated device ($A_{u.p.}$). In (1), the logarithm of the collector current is used in order to take into account the whole current range considered (here, 10 nA to 50 mA).
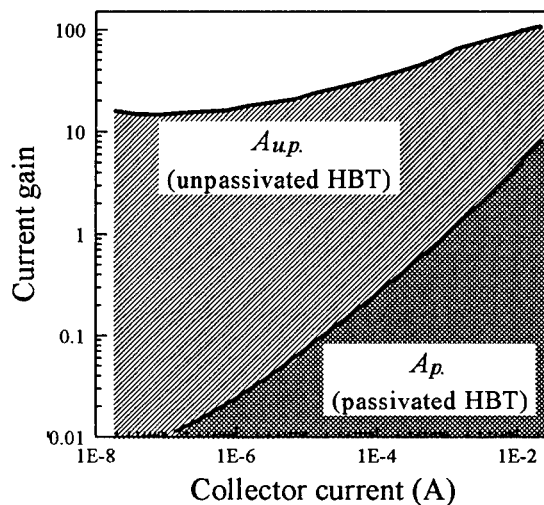
Fig. 1: Current gain vs. collector current for a passivated and an unpassivated device.

Ideally, one should expect G to be larger than unity, since one of the main purposes of

passivation is to eliminate surface recombination current, thus improving the gain uniformity with Ic. A unity value would correspond to an absence of improvement or degradation by the passivation layer, and a value lower than 1 indicates a degradation of the surface recombination characteristics related to passivation.

II. Device fabrication

All the samples used in this study have a double heterojunction structure (similar to the one presented in table 2), including several InGaAsP thin layers at the base-collector heterojunction to prevent current blocking effects.

To investigate the effect of various passivation layers, large area devices (Seb = 110 x 180 μm^2) were used so that probe contacts can be laid directly on the emitter, base and collector metallizations for passivated and unpassivated devices.

The emitter mesa was realized by chemical etching in order to reduce surface defects created during the etching step. Special care has been devoted to the base mesa etching and base metallization to minimize parasitic base-collector leakage currents. The details have been reported elsewhere [4]. For small size devices and circuits, the fabrication process has been reported previously [5].

As for passivation materials, various dielectrics (SiN_x, SiO_2, polyimide), deposition techniques (PECVD, UVCVD, spin coating) and deposition temperatures have been investigated.

III. Results

Table 1 gives the quality factor G, obtained for large area devices. All silicon nitrides deposited by either PECVD or UVCVD lead to a very low value of G. Various surface treatments (NH_3, XeF_2) prior to SiN_x deposition by UVCVD (which gave good results for HFET's and

photodiodes [6]), were tested, but did not lead to any improvement for the HBT.

Table 1: Factor G for various passivation layers.

Material	Deposition Technique	Deposition Temperature	G
Si_3N_4	PECVD	200°C	0,04
Si_3N_4	PECVD	300°C	0,03
SiN	UVCVD*	240°C	0,02
SiN	UVCVD*	100°C	0,09
Si_3N_4	UVCVD**	240°C	0,06
Si_3N_4	UVCVD**	100°C	0,13
Si_3N_4	UVCVD***	270°C	0,04
Si_3N_4	DECR-PECVD	< 100°C	0,47
SiO_2	UVCVD*	100°C	0,61
Polyimide	Spin coating	R.T.	0,92

(*) indirect photolysis; (**) direct photolysis (Hg lamps); (***) direct photolysis (Kr lamps).

The important degradation of the current gain is mainly related to a large increase of the base current on the Gummel plots, which can be attributed to surface recombination currents. An interesting feature to notice is that for almost all the dielectric materials tested, the degradation was reversible after chemical removal of the passivation layer. This confirms that no damage is created inside the bulk of the device, and that the leakage currents created by passivation are located at the interface between the semiconductor and the dielectric layer.

Finally, it appears that polyimide (deposited by spin coating, and then annealed at 300°C for 30 minutes) induces the lowest current gain degradation, leading to a value of G close to 1.

Figure 2 shows the evolution of the current gain with Peb/Seb for small scale transistors passivated with polyimide (the gain was measured at Vce = 2 V and Jc = 40,000 A/cm², for 16 devices of each size, and then averaged). Peb and Seb are the emitter mesa perimeter and area respectively. For this wafer, the 550 Å thick base layer doping level is p = 2x10^{19} cm^{-3}.
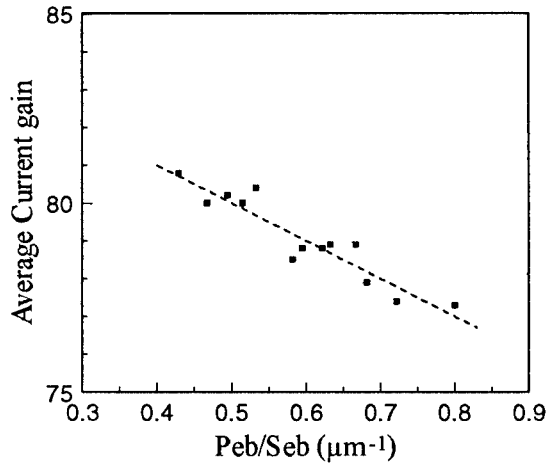
Fig. 2: Evolution of the current gain Ic/Ib at Vce = 2V and Jc = 40 kA/cm² with the emitter mesa perimeter over emitter area ratio.

A linear regression gives a correlation coefficient of 0.94, which is close to unity. This linear variation shows that β is still faintly limited by surface recombination at the emitter-base junction periphery. This result points out that although polyimide gives the best result in term of our quality factor G, it is not perfect yet, and InP-based HBT passivation should be further improved.

However, on our sample, the current gain does not vary much (5 %) for the various geometry tested (Seb varies from 16 to 129 µm²), and the dispersion for each kind of device is less that 3 % on a 2" wafer. This gain homogeneity, combined with the good planarization induced by the polyimide, is particularly interesting for circuit applications. Furthermore, it has been reported that polyimide passivated InP-based HBT's can

stand electrical stress, where a GaAs-based HBT cannot [7].

IV. Device and circuits results

Table 2 gives the HBT layer structure used for circuit applications. This structure was grown by GSMBE; the n-type and p-type dopants are Si and Be respectively.

Table 2: HBT layer structure.

InGaAs	1000 Å	n = 8x10^{18} cm^{-3}
InP	700 Å	n = 9x10^{18} cm^{-3}
InP	1700 Å	n = 3x10^{17} cm^{-3}
InGaAs	700 Å	p = 3x10^{19} cm^{-3}
InGaAs	400 Å	n = 2x10^{16} cm^{-3}
InGaAsP (0,95 eV)	200 Å	n = 2x10^{16} cm^{-3}
InGaAsP (1,15 eV)	200 Å	n = 2x10^{16} cm^{-3}
InP	6000 Å	n = 2x10^{16} cm^{-3}
InP	500 Å	n = 5x10^{18} cm^{-3}
InGaAs	1000 Å	n = 5x10^{18} cm^{-3}
InP	5000 Å	n = 7x10^{18} cm^{-3}

Transistors were fabricated with the technology described above, including polyimide passivation. For an average size device (Seb = 4x11 µm²), the current gain is around 100, the offset voltage is 130 mV, and the breakdown voltage is 18 V. As for dynamic performances, the cut-off frequencies at Vce = 2 V and Ic = 15 mA, are f$_T$ = 60 GHz and f$_{max}$ = 50 GHz.

Various digital circuits based on a differential architecture were designed and realized [8]: a 2:1 multiplexer showed a clear eye diagram up to 36 Gb/s with a voltage swing of 0.5 V (fig. 3). A 25 Gb/s 1:2 demultiplexer and a 19 Gb/s decision circuit were also successfully fabricated.

20 ps/div
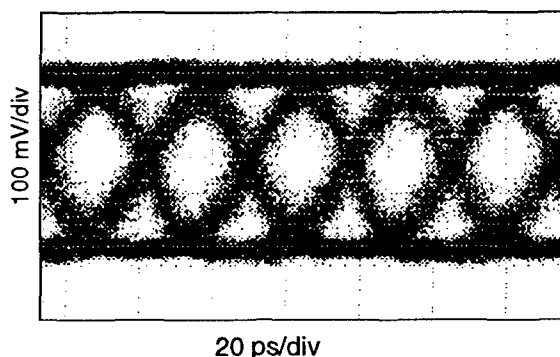
Fig. 3: 36 Gb/s output eye diagram
of the 2:1 multiplexer.

V. Conclusion

In summary, we have studied different materials (silicon nitride, silicon oxide, polyimide) for passivating InP-based HBT's, and their influence on the device electrical performances. Polyimide was found to induce the least degradation after passivation. A double-heterojunction InP/InGaAs HBT fabrication process, including polyimide passivation and planarization, has been assembled, allowing to realize high bit-rate circuits, such as a 36 Gb/s 2:1 multiplexer.

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Compositionally Graded C-doped In$_{1-x}$Ga$_x$As Base in InP/InGaAs D-HBTs Grown by MOCVD with Low Base Sheet Resistance and High Current Gain

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Abstract

MOCVD-grown carbon(C)-doped InGaAs layers using CBr$_4$ as a C source were investigated with the Van der Pauw method and PL measurement. A hole concentration of as high as 7×10^{19} cm^{-3} was obtained at a growth temperature of 385 ℃. However, PL intensity of the C-InGaAs depends on the growth temperature, and was weaker than that of Mg- or Zn-doped InGaAs at a range of over 1×10^{19} cm^{-3}. Furthermore, DC measurement of D-HBTs revealed that there existed a strict tradeoff between the current gain and base sheet resistance of C-InGaAs uniform-base D-HBTs. To break through the tradeoff, we have fabricated D-HBTs with 150-nm-thick strain-compensated graded-In$_{1-x}$Ga$_x$As-base (X=0.42⇒0.53). As a result, a current gain of 55 with a base sheet resistance of 480 $\Omega/\square$ were achieved.

1. Introduction

InP-based heterojunction bipolar transistors (HBTs) are promising devices as an alternative HBT technology to state-of-the-art GaAs-based HBTs for higher-speed [1] and lower-power [2] performance because of the high electron mobility, high electron drift velocity and small bandgap in In$_{0.53}$Ga$_{0.47}$As. Also, the small surface recombination velocity in both InP and InGaAs are advantages for fabricating very small-size devices without sacrificing current gain.

The most important aspect of growth of Npn HBTs is the magnitude and shape of the p-type dopant profiles. From the points of view, carbon (C) is supposed to be the most promising dopant for high reliable HBTs because its diffusion coefficient is smaller than that of any other dopant. In the GaAs-based HBTs, C-doping has been the well-known state-of-the-art technology with every growth technique. In the InP-based HBTs, there have been already reported high performance C-doped InGaAs base HBTs with ultrahigh vacuum deposition methods such as MOMBE [3] and CBE [4-6]. Recently, MOCVD-grown InP/InGaAs HBTs with C-doped base have been reported [7,8]. However, the hole concentration in C-doped base of MOCVD-grown HBTs is lower than that of the CBE or

GSMBE-grown HBTs, because the effects of the hydrogenation of C acceptor of MOCVD-grown InGaAs are remarkable. Also, there is a strict tradeoff between the current gain and hole concentration, in other words, base sheet resistance of MOCVD-grown C-InGaAs base HBTs [8]. This tradeoff makes the HBT design for high speed IC application more difficult than that using any other dopant such as Zn, Mg and Be.

This report describes the MOCVD growth of C-doped InGaAs layers and DC characteristics of compositionally graded C-InGaAs base D-HBTs to break through the tradeoff.

2. MOCVD Growth of C-doped InGaAs

2.1 Basic doping characteristics of C-InGaAs

C-doped InGaAs layers were grown by low-pressure (10kPa) MOCVD on (100) InP substrates with tetrabromocarbon (CBr$_4$) used as a C source with various V/III ratio and growth temperature. Halides such as CBr$_4$ are known as etching gasses for semiconductor. Moreover, the etching rate of InGaAs by CBr$_4$ depends on the growth temperature, flow rate of CBr$_4$ and V/III ratio. Therefore, to investigate the dependence of doping characteristics on the growth temperature, we have fixed the growth rate of C-doped

InGaAs at around 0.9 μm/h varying the V/III ratio and molar flow rate of trimethylindium (TMI) and triethygallium (TEG). The growth temperature on the InP substrate in a reactor was calibrated at the melting point of aluminum. Hall measurement was performed using the standard Van der Pauw method with samples ranging in thickness from 0.5 μm to 0.2 μm before and after a post-growth anneal at 500 ℃ in N_2 ambient for 5 min. It was confirmed that this condition of the post-growth anneal had dissociated hydrogen in as-grown InGaAs layers by SIMS analysis.

Figure 1 shows the maximum hole concentration of C-doped InGaAs layers as a function of the growth temperature for the maximum CBr_4 flow rate of 3.2 $\times 10^{-6}$ mol/min before and after the post-growth anneal. The growth mode of GaAs using TEG was in the kinetically limited in these temperature. The maximum doping level after the post-growth anneal of 7×10^{19} cm^{-3} was achieved at a growth temperature of 385 ℃ which supposed to be lower limit temperature without the effect of immiscible phenomenon. Among MOCVD-grown InGaAs, this is not only higher than that of any other dopant, which is one of the advantage of C-doing, but also the same value as high as the highest value ever reported using CCl_4 as the C source [7].
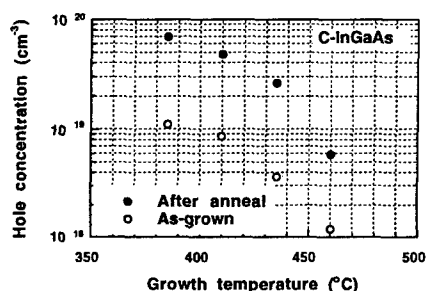
Figure 1. The maximum hole concentration of C-doped InGaAs layers as a function of the growth temperature for the maximum CBr_4 flow rate of 3.2 $\times 10^{-6}$ mol/min.

Figure 2 shows photoluminescence (PL) intensity comparison of Zn-, Mg- and C-doped InGaAs with a hole concentration of over 1×10^{19} cm^{-3}. Zn- and Mg-doped [9] InGaAs layers were grown at 510 ℃, whereas C-InGaAs was grown at 410 ℃ and 435 ℃ with the post-growth anneal. The PL intensity of C-InGaAs was dependent on the growth temperature and weaker than that of Zn- or Mg-doped InGaAs, which indicates that the crystalline quality related to nonradiative recombination center of C-InGaAs is

inferior to that of high-temperature-grown InGaAs using Zn or Mg.
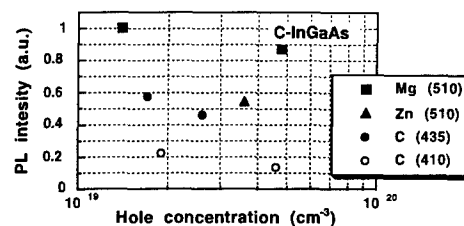
Figure 2. Photoluminescence (PL) intensity comparison of Zn-, Mg- and C-doped InGaAs with a hole concentration of over 1×10^{19} cm^{-3}. The numerals in the parenthesis indicate the growth temperature.

2.2 Activation of C in InGaAs with InP

Figure 3 shows the hole concentration of C-doped InGaAs layers with n-InP cap layers as a function of the growth temperature. The growth temperature of C-InGaAs and n-InP was 435 ℃ and 510 ℃, respectively. These results show that the growth of n-InP cap layers activate the C acceptor despite of the H_2 ambient during the additional growth. However, an activation ratio of the C acceptors was estimated as low as 40 % when it was compared with the hole concentration after the post-growth anneal shown in Fig. 1. These results indicate that there may be a tradeoff of MOCVD-grown C-InGaAs base HBTs between current gain and base sheet resistance since the current gain depends on the actual doping concentration of the base in general.
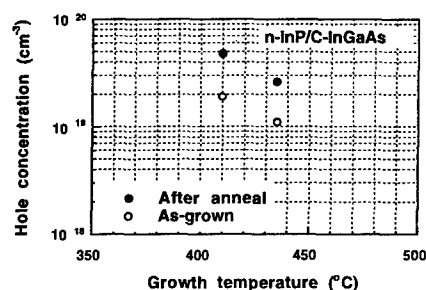
Figure 3. The hole concentration of C-doped InGaAs layers with n-InP cap layers as a function of the growth temperature.

3. Epitaxial Layer Structure of D-HBTs

Table 1 shows the epitaxial layer structure of emitter-up D-HBTs with composite collector [10].

642

The emitter layers comprised 25-nm-thick n-doped and 75-nm-thick n+-doped InP. No spacer layer was prepared at the emitter/base interface. The collector layers were composed of undoped 300-nm-thick InGaAs layer, compositionally graded InGaAsP layers and 100-nm-thick n-doped InP layer.

To reduce the base sheet resistance of D-HBTs, we have employed thick base layers with thickness of 100 nm and 150 nm. Furthermore, to suppress decrease of the current gain of HBTs with the thick-base, the compositionally strained and graded structure [11,12] was introduced into the base region, which is so-called graded-base HBTs. The base region consisted of four steps of InGaAs for 100-nm-thick-base and six steps for 150-nm-thick-base. To minimize amount of strain in the base, the GaAs fraction of X in the 100-nm-thick $In_{1-X}Ga_XAs$ base is increased from X=0.42 (compressive-strain) at the base/collector junction to X=0.49 (tensile-strain) at the emitter/base junction, which is so-called strain-compensated structure. Also, X in the 150-nm-thick $In_{1-X}Ga_XAs$ base is increased from X=0.42 at the base/collector junction to X=0.53 at the emitter/base junction. An internal built-in field for the electrons in the graded-base is about 7.4 kV/cm in 100-nm-thick base and 7.9 kV/cm in 150-nm-thick base. For comparison, we have prepared D-HBTs with C-, Zn- and Mg-doped uniform-base. The growth temperature of the C-doped base layer was 435 °C from the point of view of the tradeoff between the hole concentration and PL intensity, and the rest layers were grown at 510 °C for the emitter and 575 °C for the collector.

Table 1. The epitaxial layer structure of emitter-up D-HBTs.

Layer	Material	Thickness (nm)	Doping (cm⁻³)
Emitter Cap	n+-InGaAs	50	2×10¹⁹
Emitter	n-InP	25	1×10¹⁹
	n-InP	75	3×10¹⁷
Base	p+-In₁₋ₓGaₓAs	50~120	1~2×10¹⁹
	φ-InGaAs	300	
Collector	φ-InGaAsP (×2~3)	40~60	
	Si-InP	100	3×10¹⁷
Sub Collector	n+-InGaAs	500	3×10¹⁹
Substrate	S.I. InP		

After epitaxial growth of the whole layers, mesa structure HBT devices were fabricated by wet chemical selective etching process and liftoff technique. A 100 nm thick plasma-assisted CVD SiN films was deposited for surface passivation. The devices employed Ti/Au non-alloyed ohmic contacts to emitter cap, base and subcollector layers.

4. HBT Characteristics

Figure 4 shows common emitter I-V characteristics of the C-doped 100-nm-thick graded-base D-HBT device (100 μm in an emitter diameter). Measured DC current gain (β) was 85 at a collector current of 85 mA, which corresponds to a collector current density of 1.1×10^3 A/cm². TLM measurement showed that the sheet resistance (R_{BS}) of the base layer was 970 Ω/□. On the other hand, β and R_{BS} of the C-doped 100-nm-thick uniform-base HBT were 50 and 880 Ω/□, respectively.
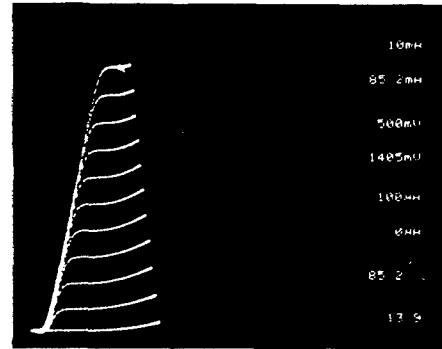
Figure 4. Common emitter I-V characteristics of the C-doped 100-nm-thick graded-base D-HBT device. The emitter diameter is 100 μm.

Figure 5 shows β as a function of R_{BS} of D-HBTs with 4 ×20 μm² emitter areas. Assuming that the emitter injection efficiency is unity and the minority electron lifetime in the base region is limited by the Auger recombination, β is expressed as follows,

$$\beta = 2qk_BT\mu_h^2\mu_eA^{-1}R_{BS}^2, \qquad (4.1)$$
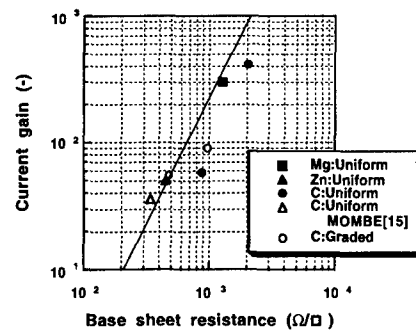
Figure 5. The current gain (β) as a function of the base sheet resistance (R_{BS}) of D-HBTs with 4 ×20 μm², together with data from ref. [15]. The solid line shows the theoretical limit of the current gain calculated from the expression (4.1).

, where k_B is the Boltzman constant, T is the temperature, μ_h is the majority hole mobility, μ_e is the minority electron mobility and A is the Auger coefficient. The solid line calculated from the expression (4.1) shows the theoretical limit of the current gain of uniform-base HBTs assuming A of 4×10^{-29} cm^6/s [13] and μ_e of 2000 cm^2/Vs [14]. The uniform-base HBTs with C-doped InGaAs base were inferior to that with Zn- and Mg-doped InGaAs base under the β-R_{BS} relation, which is consistent with the results of the PL intensity comparison in Fig. 2. These results indicate that the electron lifetime of C-InGaAs depends on the recombination due to the low growth temperature in addition to the Auger recombination. Furthermore, D-HBTs with strain-compensated graded C-InGaAs base is comparable to that with any other base-dopant under the β-R_{BS} relation. It is concluded that MOCVD-grown C-doped base InP/InGaAs HBTs are competitive with devices with the other base-dopants and the other growth techniques.

5. Summary

MOCVD-grown C-doped InGaAs layers using CBr$_4$ as the C source were investigated. The PL intensity of C-InGaAs depended on the growth-temperature, and was weaker than that of Mg- or Zn-doped InGaAs, which indicates that nonradiative recombination center of heavily doped p-type InGaAs increased with decreasing the growth temperature.

Under the β-R_{BS} relation, D-HBTs with C-InGaAs base were inferior to that of Mg- or Zn-doped InGaAs base, that is to say, there exists the strict tradeoff between the current gain and the base sheet resistance. To break through the tradeoff, we have fabricated D-HBTs with 150-nm-thick strain-compensated graded-In$_{1-x}$Ga$_x$As-base (X=0.42$\Rightarrow$0.53). As a result, β of 55 with R_{BS} of 480 $\Omega/\square$ was achieved, which was comparable to HBTs with the other base-dopants and the other growth techniques.

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Double Heterojunction Bipolar Transistors with Chirped InGaAs/InP Superlattice Base-Collector Junction Grown by CBE

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Abstract

We report the performance of InP DHBT's with a chirped InGaAs/InP superlattice B-C junction grown by CBE. The B-C junction of the DHBT was graded with a 10-period InGaAs/InP chirped superlattice (CSL) between the InGaAs base and the lightly doped InP collector. A highly doped thin layer was also included at the end of the CSL to offset the quasielectric field arising from the grade and suppress further the carrier blocking effect across the B-C heterojunction. The InP/InGaAs CSL DHBT demonstrated a high BV_{CEO} of 18 V with a typical current gain of 55 with minimal carrier blocking up to high current densities. Maximum cutoff frequencies of f_{max} = 146 GHz and f_T = 71 GHz were obtained from the fabricated $2 \times 10 \mu m^2$-emitter DHBT.

Introduction

InP-based heterojunction bipolar transistors have demonstrated impressive high-speed performance due to their excellent intrinsic material properties. InP single heterojunction bipolar transistors (SHBT's) have shown maximum cutoff frequencies greater than 200 GHz [1,2]. However, the low breakdown voltages of the SHBT's associated with high impact-ionization rates of InGaAs have limited their use mainly to low-power high-speed applications [3,4].

In order to improve the breakdown characteristics of InP HBT's for micro-/millimeter-wave power applications, InP-based double heterojunction bipolar transistors (DHBT's) with different base-collector (B-C) designs have been investigated recently. These designs include a tunneling InP collector [3], quaternary linearly-graded InGaAlAs or step-graded InGaAsP B-C junctions [5,6], and InGaAs/InP or InGaAs/InAlAs chirped superlattice linear-graded B-C designs [7-9]. The CSL design has been recently demonstrated using the InGaAs/InAlAs layers in an InP-collector DHBT [8]. However, there have been very few reports on InGaAs/InP CSL B-C junctions due to the growth difficulty associated with the Group-V intermixing [9,10], although this material system is much more favored due to the superior transport properties of InP and smaller conduction-band offset of InGaAs/InP.

In this paper, the performance characteristics of InGaAs/InP CSL B-C junction DHBT's are presented. This is to our knowledge the first study of InP/InGaAs DHBT's with InP emitter and collector, and an InGaAs/InP CSL B-C junction, which were grown by chemical beam epitaxy (CBE).

Device Structure and Fabrication

The InP/InGaAs DHBT heterostructures were grown by CBE. The detail of the epitaxial profile is shown in Fig. 1. The main features of the layer

1000Å	InGaAs	n^+=1x10^{19}cm^{-3}	Contact
500Å	InP	n^+=1x10^{19}	Contact
1500Å	InP	n=5 x10^{17}	Emitter
20Å	InGaAs	undoped	Spacer
600Å	InGaAs	p^+=3x10^{19}	Base
20Å	InGaAs	undoped	Spacer
500Å 10-period InGaAs/InP CSL		n^-=3x10^{16}	Grade
40Å	InP	n=4x10^{18}	Delta doping
6000Å	InP	n^-=3x10^{16}	Collector
6000Å	InGaAs	n^+=1x10^{19}	Subcollector
S.I. InP:Fe Substrate			

Fig. 1. Epitaxial layer structure of the InP/InGaAs CSL DHBT grown by CBE.

645

structure include a 6000Å-thick (n = 3 × 10^{16} cm^{-3}) InP collector and 500Å InGaAs/InP CSL graded B-C junction. The compositional grading was achieved with a 10-period CSL of InGaAs/InP. Each period of the superlattice was 50Å-thick in which the thicknesses of layers were varied in a linear scale. A 40Å n-type layer, delta-doped at 4 × 10^{18} cm^{-3}, was inserted prior to the collector to compensate the quasielectric field generated by the compositional grade. To further improve the common-emitter output characteristics of the DHBT, a thin undoped InGaAs spacer was used between the 600Å-thick Be-doped p$^+$-InGaAs base and the CSL grade. Through a series of DC chacterization and growth of test devices with different spacer thicknesses, the spacer thickness was optimized to be 20Å.

A self-aligned emitter-base mesa process was used to fabricate the HBT's with nonalloyed Ti/Pt/Au metallization for the emitter and collector ohmic contacts and Pt/Ti/Pt/Au for the base contact. Chemical wet etchants of H$_3$PO$_4$:H$_2$O$_2$:H$_2$O and HCl: H$_3$PO$_4$ were used to selectively etch the InP and InGaAs with precise undercut control for the self-aligned emitter-base contacts. The CSL structure was etched by either a RIE or a non-selective wet etch.

Results and Discussion

The Gummel plot of a typical InP DHBT is shown in Fig. 2. The device demonstrated the ideality factors of the collector and base currents of 1.3 and 1.65, respectively. The ideality factors of the DHBT were found comparable to those

obtaind from a test SHBT with a similar InP/InGaAs E-B structure. No DC blocking was observed up to the collector current density (J$_C$) of 4 × 10^4 A/cm^2. The results indicate that the used InGaAs/InP CSL grade effectively eliminates the conduction band barrier at the B-C junction up to high current densities, typically used under normal operating conditions. At higher current densities, the current gain started to degrade due to the Kirk effect occurring across the lightly doped CSL B-C junction. The measured DC current gain of the CSL DHBT is shown in Fig. 3. The device showed a peak current gain of approximately 55 at high current levels.

The common-emitter I-V characteristics of the DHBT are shown in Fig. 4. The device demonstrated a high breakdown voltage of
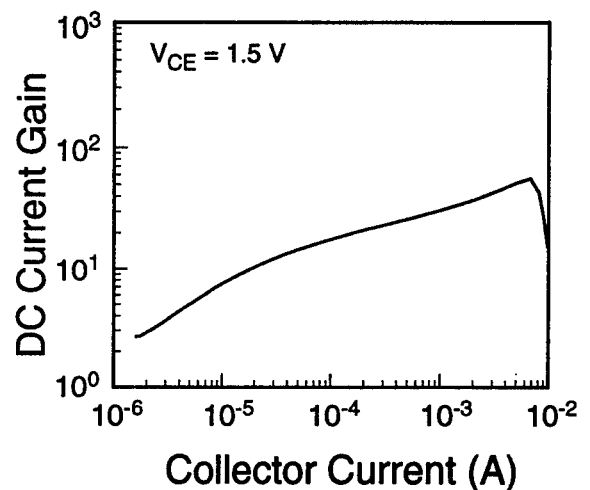
Fig. 3. DC current gain of the CSL DHBT as a function of I$_C$ at V$_{CE}$ = 1.5 V.

Fig. 2. Gummel plot of a typical InP/InGaAs CSL DHBT.
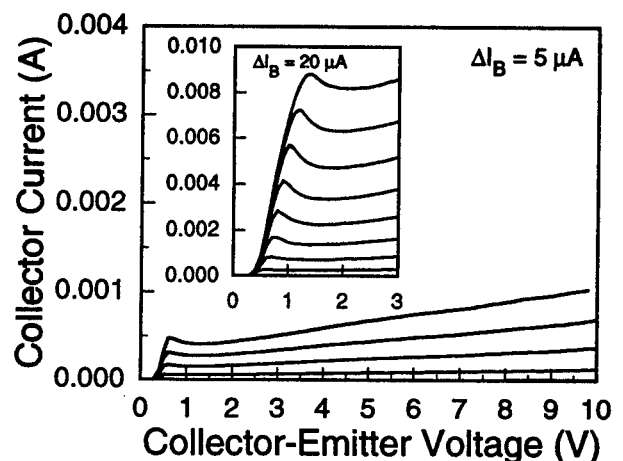
Fig. 4. Common-emitter I-V characteristics of the CSL DHBT.

BV_{CEO} = 18 V and a collector-emitter offset voltage of $V_{CE,OFF}$ = 0.2 V. The B-C junction I-V characteristic of the device is shown in Fig. 5. The base-collector breakdown voltage (BV_{BCO}) of the device, which was measured at a collector current of 100 μA, was 22.8 V.
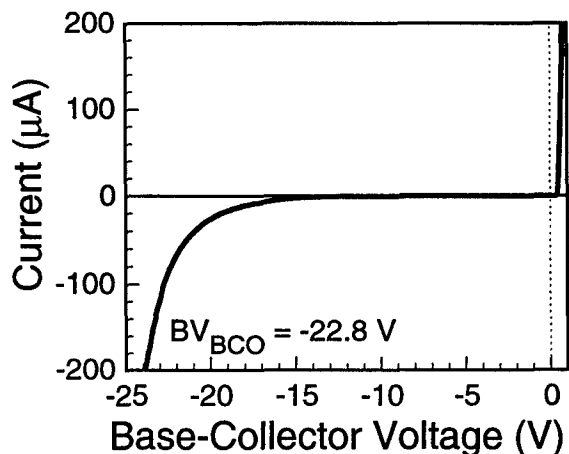
Fig. 5. Base-collector junction I-V characteristic of the CSL DHBT.

As is shown in the output characteristics of the inset of Fig. 4, the DHBT exhibited excellent injection properties up to $J_C = \sim 4 \times 10^4$ A/cm² with a sharp current rising slope from the device saturation regime. At the end of the collector current rising edge, a collector current kink was observed. Similar current kink effects have been observed in the common-emitter I-V characteristics of InP-based DHBT's [9] and SHBT's [11,12]. This effect, observed in SHBT's, has been attributed to the enhanced electron drift velocities, arising from non-equilibrium carrier transport processes across the B-C junction at low electric-field densities [12].

The collector current peaking of the fabricated CSL DHBT was observed mostly in a bias range of V_{CE} less than ~1.5 V. Compared to other DHBT's, which often show slow current rising edges or large knee voltages, the sharp rising I-V characteristics of the fabricated device indicate that the CSL B-C design used in the present work effectively suppresses the carrier blocking effect occurring at the B-C junction.

Small-signal S-parameters of the devices were measured in a frequency range from 0.5 to 26 GHz using an HP8510. Fig. 6 shows the gain-frequency characteristics of the CSL DHBT with an emitter area of 2×10μm², measured at a bias point of $I_C = 6$ mA and V_{CE} = 3.5 V. The unity current gain cutoff
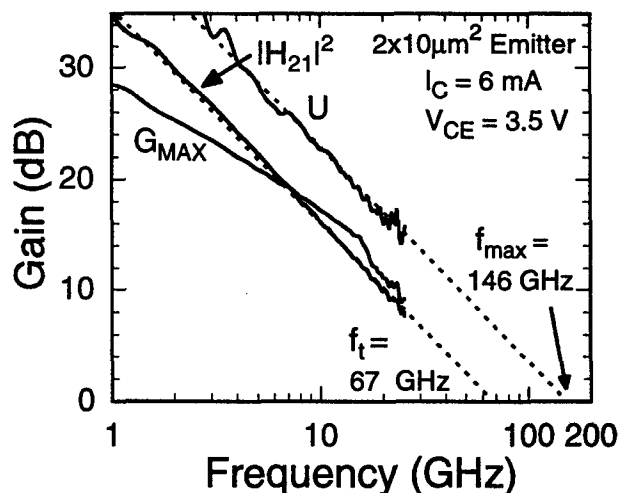
Fig. 6. Gain-frequency characteristics of a 2×10μm²-emitter CSL DHBT biased at I_C = 6mA and V_{CE} = 3.5 V.
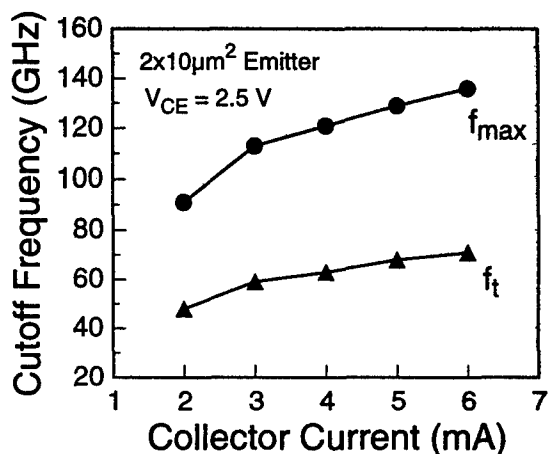
(a)
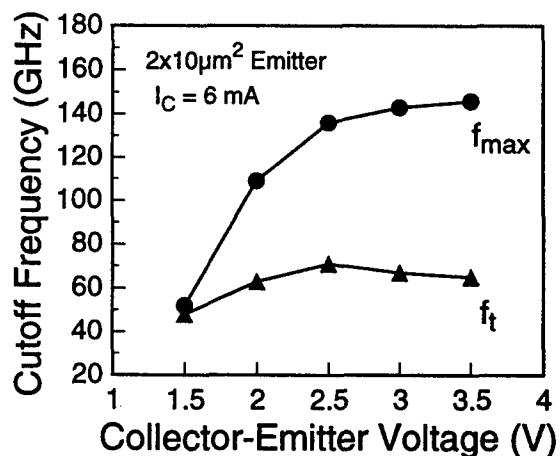
(b)

Fig. 7. Bias dependence of cutoff frequencies of the 2×10μm²-emitter CSL DHBT on (a) I_C and (b) V_{CE}.

647

frequency f_T and maximum oscillation frequency f_{max} of the HBT were obtained by extrapolating the measured current gain ($|H_{21}|^2$) and Mason's unilateral gain (U) with a 6 dB/octave falloff slope. The bias dependence of f_T and f_{max} of the device, obtained from the measured S-parameter data at different biases, is shown in Fig. 7. The peak f_{max} of the device was 146 GHz and the peak f_T was 71 GHz. The obtained f_{max} value of 146 GHz from the fabricated CSL DHBT is to our knowledge the highest reported to date for an InP-based DHBT, which has an InP collector with a BV_{CEO} larger than 17 V. Fig. 7 (a) shows that the cutoff frequencies of the DHBT increase as the injection current increases at a collector-emitter bias of 2.5 V. At a collector current density of 3×10^4 A/cm^2, the cutoff frequencies of the device remained fairly constant as V_{CE} varies from 2 V to 3.5 V. At higher values of V_{CE} and I_C, the degradation of RF performance was observed due to the thermal effects associated with the unthinned substrate.

Conclusion

The InP/InGaAs DHBT's, of which B-C junction was graded with a 10-period chirped InGaAs/InP superlattice along with a delta-doped layer design, were grown by CBE. The fabricated self-aligned emitter-base DHBT's with an InP collector demonstrated large breakdown voltages of BV_{CEO} = 18 V and BV_{BCO} = 22.8 V with a typical current gain of 55. The device also exhibited excellent injection properties up to $J_C = 4 \times 10^4$ A/cm^2 with the minimal current blocking at the B-C heterojunction. The maximum cutoff frequencies of f_{max} = 146 GHz and f_T = 71 GHz were obtained from the 2×10μm^2-emitter device. These results demonstrate that the InP/InGaAs DHBT's, which were grown by CBE with an optimized CSL B-C design, are very promising for micro-/millimeter-wave high-power applications.

Acknowledgements

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Minimization of the Noise Measure of InP/InGaAs HBTs

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Introduction

A complete noise characterization as a function of emitter-geometry, temperature, bias-point and frequency $(2 - 26\ GHz)$ of InP/InGaAs HBTs was carried out. Measurements and simulations have shown that there is an optimum emitter geometry and bias point for achieving a minimum noise measure. The noise measure is very important figure of merit in broadband amplifier design because not only the noise but also the gain of the device is taken into account. The measured noise characteristics are validated by an equivalent circuit model with associated noise sources at different device temperatures.

I. Background

In addition to the small- and large-signal properties, the noise of the transistor limits the circuit performance since it sets the lower limit to the signal level which can be processed. For optimal circuit design of e.g. low-noise broadband amplifiers, not only the noise figure but also the gain of the device has to be taken into account. Therefore, the noise measure

$$M = \frac{F-1}{1-1/G_a} \qquad (I.1)$$

which includes the stage gain, has to be minimized. M is the measure of noisiness of a stage which consists of an infinite number of stages with the noise figures F and the gains G_a. Hence, we analyze the area-, bias-, temperature- and frequency-dependences of InP/InGaAs HBT characteristics including the noise measure M.

A. Device Structure

InP-based HBTs are advantageous for optoelectronic, microwave and high-speed digital applications because of the excellent optical and transport properties of both InP and InGaAs. Using a MOCVD-grown epitaxial layer structure (Tab. 1) and a self-aligned emitter technology, high-speed InP/InGaAs HBTs with f_T and f_{max} of 80 and 120 GHz, respectively, were successfully fabricated [1].

Table 1: Device layer structure of the InP/InGaAs HBT

Layer	Material	Type	Thickness [nm]	Doping [cm^{-3}]
Cap	InGaAs	n^+	300	$2.0 \cdot 10^{19}$
Emitter	InP	n^+	50	$1.0 \cdot 10^{19}$
Emitter	InP	n	250	$4.0 \cdot 10^{17}$
Spacer	InGaAs		7	undoped
Base	InGaAs	p^+	80	$3.5 \cdot 10^{19}$
Collector	InGaAs	n^-	600	$1 \cdot 10^{16}$
Collector	InGaAs	n^+	50	$1.0 \cdot 10^{19}$
Subcollector	InGaAs	n^+	1100	$1.0 \cdot 10^{19}$
Substrate	InP	S.I.		

The simplified cross-sectional view of the HBT in Figure 1 presents the lateral geometry of the transistor together with the vertical structure.

B. Measurements

Microwave S-parameters and noise characteristics were measured from 2 to 26 GHz on wafer at different collector currents and temperatures using a network analyzer and noise parameter test set. A peltier element was used to set the temperature to 20, 40, and 60°C. In order to optimize the emitter geometry we have varied the emitter widths W_E from 1 μm to 2.5 μm in steps of 0.5 μm with emitter length L_E of 5 μm, 8 μm and 16 μm. The noise figure, the available gain and the resulting noise measure were determined.
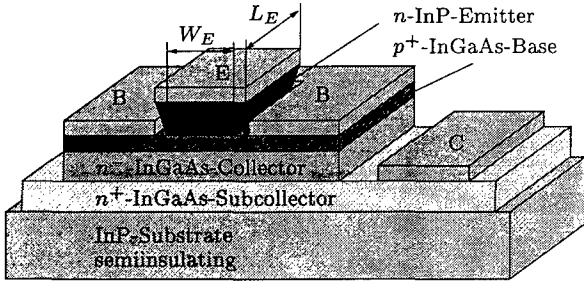
Figure 1: Cross-sectional view of the HBT

II. Model

We developed a small-signal noise model (Fig. 2) which consists of two correlated shot noise sources and the thermal noise sources of the parasitic resistances in addition to the small-signal elements [2].
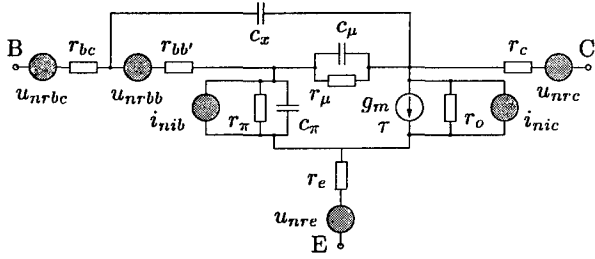
Figure 2: Equivalent circuit model

The determination of the model elements was performed by direct extraction from measured S-parameters and by an optimization procedure. In this procedure, the simulated noise- and S-parameters were simultaneously fitted to the measured data. The resulting equivalent model parameters (EMP) are listed in Table 2 for a temperature of $20°C$ and a collector current of $2\ mA$.

Table 2: Equivalent model parameter (EMP) at $I_C = 2.0\ mA, I_B = 210\ \mu A, V_{CE} = 1.5\ V$, and $T_C = 20°C$

EMP	Value	EMP	Value
r_{bc}	3.6 Ω	c_{mu}	2.7 fF
$r_{bb'}$	21.0 Ω	c_{bcx}	12.2 fF
r_c	2.1 Ω	r_o	100 $k\Omega$
r_e	1.8 Ω	C_{BEP}	10.2 fF
r_π	242 Ω	C_{CEP}	16.4 fF
c_π	133 fF	C_{BCP}	1.8 fF
g_m	50.1 mS	L_{BP}	38.1 pH
τ	1.11 pS	L_{CP}	11.5 pH
r_μ	250 $k\Omega$	L_{EP}	6.0 pH

The spectral power densities of the base and collector shot noise sources are $\overline{i^2_{nib}} = 2qI_B$ and $\overline{i^2_{nic}} = 2qI_C$, respectively. The spectral densities of the noise of the

resistors are $\overline{u^2_{nrx}} = 4kT_xR_x$. The resistors are supposed to be at two different temperature. First, the resistors r_{bc}, and r_c are at case temperature T_C, which is the temperature of the substrate adjusted by the peltier element. The resistor $r_{bb'}$ which models the internal base resistance and r_e are at the junction temperature T_J. Because it is almost impossible to measure the junction temperature accurately, T_J was determined from g_m assuming $g_m = I_C/(N_F V_T)$ where $V_T = kT_J/q$ and N_F is the forward current emission coefficient.

The parameters C_{XYP} and L_{XP} in Table 2 (not drawn in Figure 2) model the pads which are necessary for the on-wafer measurements.

Figure 3 shows the simulated and measured results of the minimum noise figure. A very good agreement between measurements and simulation has been achieved even at different temperatures.
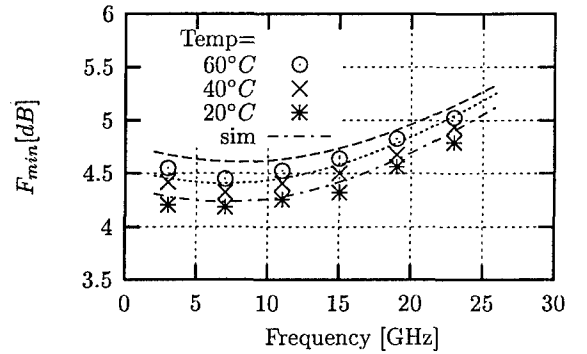
Figure 3: Minimum noise figure of a $1.5 \times 8\ \mu m^2$ HBT for the temperatures of 20, 40 and $60°C$ at $I_C = 2\ mA$

In a circuit design model not only the noise but also the small-signal behavior must be described accurately. Since the noise measure M is calculated from the noise behavior (F_{min}) and the small-signal behavior (G_a) (Eq. I.1), M is an appropriate measure to verify the a noise model. The excellent correspondence of the simulated and measured noise measure is demonstrated in Figure 4.

III. Results

There is a significant difference between the bias dependence of the noise measure M and the minimum noise figure F_{min} as depicted in Figure 5. In contrast to the minimum noise figure, a pronounced minimum of the noise measure exists at a collector current of around $2\ mA$ for an $1.5 \times 8\ \mu m^2$ HBT.

It becomes obvious that design of a low-noise circuit does not lead to the same bias-points when the transistors are operated in optimal noise measure instead of noise figure conditions. The Figures 6 and 7 show the dependence of the noise measure as a function of the

650
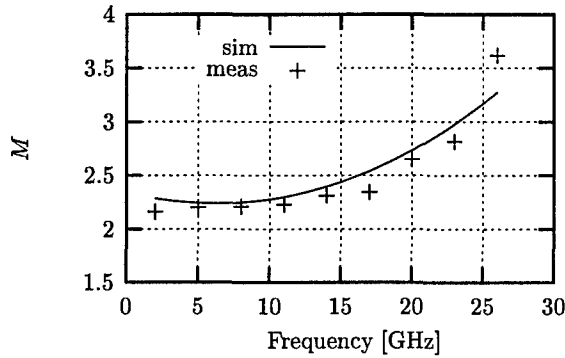
Figure 4: Comparison between measured and simulated data for the noise measure vs frequency at $I_C = 5.7\ mA$ and $T_C = 20°C$ for the emitter area of $1.5 \times 8\ \mu m^2$
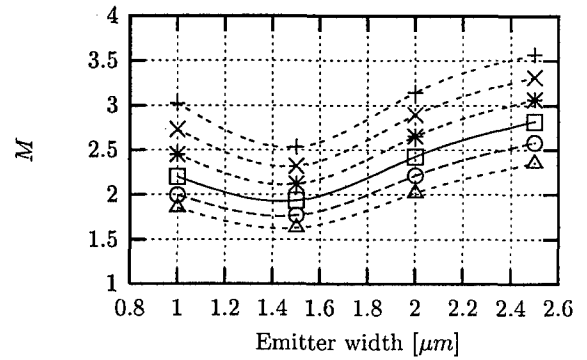
Figure 6: Measured noise measure M vs the emitter width W_E at an emitter length $L_E = 8\ \mu m$, $f = 10\ GHz$, $I_C = 2\ mA$ ($\triangle$) $\ldots 7\ mA$ (+)
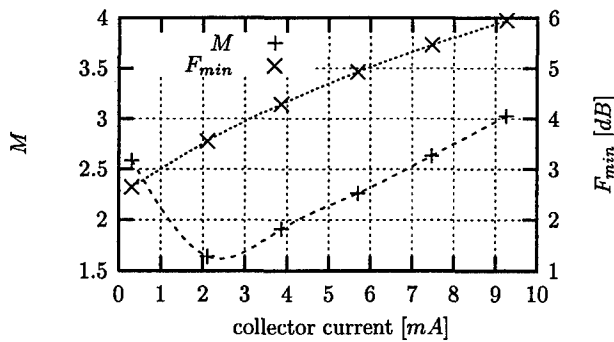
Figure 5: Measured noise measure and noise figure vs the collector current of an $1.5 \times 8\ \mu m^2$ at $f = 10\ GHz$
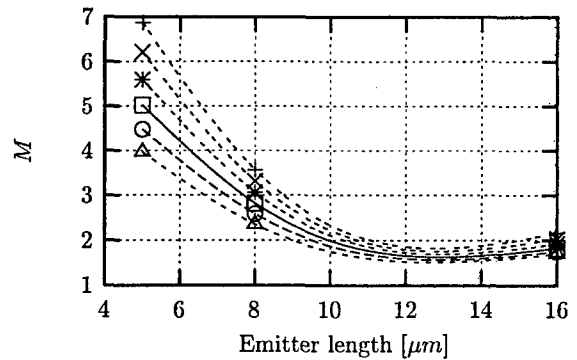
Figure 7: Measured noise measure M vs the emitter and vs emitter length L_E at $W_E = 1.5\ \mu m$, $f = 10\ GHz$, $I_C = 2\ mA$ ($\triangle$) $\ldots 7\ mA$ (+)

emitter geometries i.e. emitter lengths L_E and widths W_E.

The Figures 6 and 7 show the dependence of the noise measure as a function of the emitter geometries i.e. emitter lengths L_E and widths W_E.

A minimum noise measure resulted at the same emitter width $W_E = 1.5\ \mu m$ for all frequencies and bias points (Fig. 6) setting the parameter for optimal emitter design. To find the optimal noise measure M at the emitter width $W_E = 1.5\ \mu m$ is especially favorable for high-speed low-noise circuit design because we observed the best high frequency characteristics of these transistors for this emitter width as well.

As expected, a longer emitter reduces the noise of the transistors (Fig. 7). This is due to the fact that a larger emitter length reduces the resistances and hence, the noise contribution arising from the thermal noise of the base resistance. This considerably diminishes the overall noise of the transistor because the noise of the base resistance is, in addition to the shot noise, one of the dominant noise. Further measurements of even longer transistors will turn out if there is optimal emitter length L_E for the noise measure M. An increase of M would happen due to the degradation of the small-signal prop-

erties of the device when going to longer emitters.

IV. Conclusion

There is a significant difference between the bias dependence of the noise measure M and the minimum noise figure F_{min}. A collector current I_C is found where the noise measure is minimal, but the minimum noise figure increases continuously with I_C. Further, we have demonstrated that there is an optimal emitter geometry for achieving a minimum noise measure. Thus, we are able to determine the emitter area and bias-point which will provide the lowest noise measure M. The very good agreement between measurement and simulation of the noise figure and noise measure, even at different temperatures, confirms the quality of our model. The good correspondence of the model and the measurement can be observed in a wide range of bias-point and transistor geometry. Hence, this model is a well suitable tool for designing low-noise circuits.

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652

Fabrication Technology of
Spot-size Converter Integrated Laser Diodes (SS-LDs)

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Introduction

Laser diodes (LDs), in which the spot-size of the oscillating light can be expanded to match an optical fiber, are attractive devices for system application. These provide low-loss coupling to optical fiber and waveguides without lenses as well as large alignment tolerance in assembling optical modules. Especially for access network application, good high-temperature characteristics and high reliability are strongly required. Several investigations have been carried out to realize this LD[1]~[16]. Spot-size converters have been monolithically integrated with conventional Fabri-Perot LDs.

We have recently developed 1.3-μm spot-size converter integrated lasers (SS-LDs) [5]. Key fabrication technologies are selective butt-jointing for integration and dry etching to form mesa structure in a 2-inch wafer. This paper describes uniform fabrication technologies for 2-inch wafers and demonstrates the stable and reliable high-temperature characteristics of 1.3-μm spot-size converter integrated lasers fabricated using those technologies.

1. Structure and design for 1.3μm SS-LD

The structure of the SS-LD is shown in Figure 1. The low-loss taper waveguide for the spot-size converter (SS) is butt-jointed to the strained multi-quantum-well (MQW) active waveguide. The thickness of the taper waveguide in the SS region changes exponentially from the butt-joint portion to the front facet. This structure offers the advantage that a vertically tapered waveguide with a bandgap wavelength (λg) of 1.1 μm and strained MQW active region with λg of 1.3 μm were independently optimized, while the step of epitaxial growth increased.

the thickness t_0 and the bandgap wavelength λg at the front facet of the tapered waveguide.

(a)

(b)
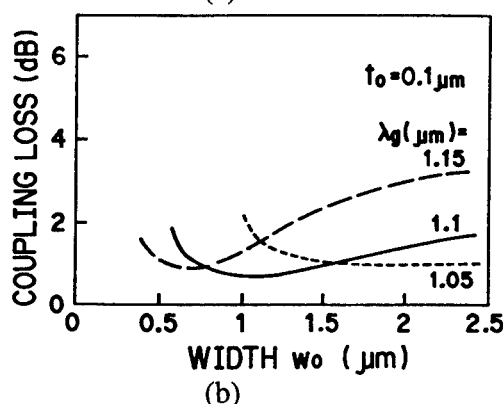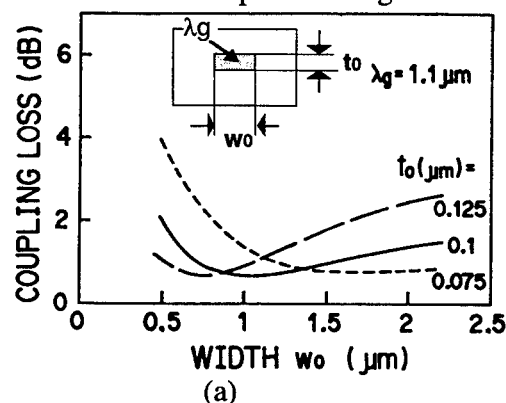
Fig. 2 Calculated coupling loss of spot-size converter to dispersion sifted fiber. The parameters are (a) taper layer thickness t_0 at the front facet and (b) bandgap wavelength λg of taper layer at the front facet.

Fig. 1 Schematic structure of a 1.3-μm spot-size converter integrated laser.

Figure 2 (a) and (b) show the calculated coupling loss to dispersion sifted fiber (DSF, core radius = 4μm) with the front facet width W_0 of the tapered waveguide. The parameters are

The parameters are (a) taper layer thickness t_0 at the front facet and (b) bandgap wavelength λ_g of taper layer at the front facet.

To achieve a coupling loss smaller than 2 dB, the thickness and λ_g should be within 0.075 to 0.125 μm and 1.05 to 1.1 μm, while the width is within 1.0 to 1.5μm, respectively. These tolerance in thickness, λ_g, and width are advantage of this design because it is large enough for the 2-inch LD fabrication process to control these values within the tolerance.

2. Fabrication

In the active layer the compressive strain in the range of 1.0~1.2% in InGaAsP wells is introduced to improve the temperature dependence of the lasing characteristics by suppressing carrier overflow at high temperatures [17]. The number of wells was optimized, i.e., 8 wells, to increase the maximum operation temperature effectively [18].

The part of the active layer where the SS region is to be formed is removed by wet etching using a SiNx mask. The MQW-wet etching characteristics were uniform in the wafer [19]. After etching off the active layer the side-etching depth from the SiNx mask are about 0.40 μm in the wafer. In the SS region, a low-loss InGaAsP bulk taper layer was selectively grown during the butt joint growth. Figure 3 shows the micro-photoluminescence (PL) profile at the SS region. After the butt-joint growth, the micro-photoluminescence (PL) reveals that PL wavelength changes from 1.13 μm to 1.09 μm at a joint and a facet portion respectively.
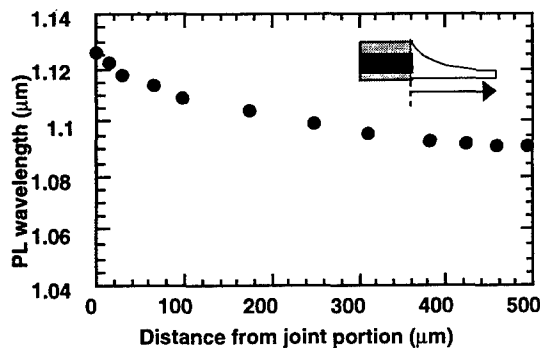
Fig. 3 Micro-photoluminescence distribution in the SS region.

Methane/hydrogen reactive ion etching (CH4/H2 RIE) using a 1.5-μm-wide SiO2 mask were employed for mesa structure formation. The distribution of waveguide-width in the wafer after dry etching is shown in Figure 4. The
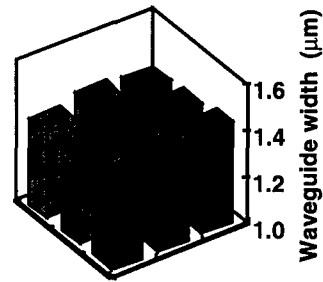
Fig. 4 Distribution of waveguide-width in the wafer after dry etching.

The mesa is embedded by p-and n-InP blocking layers. Figure 5 shows the cross-section of (a) the waveguide at the facet of the tapered waveguide and (b) the active region. The thickness at the end of the tapered waveguide was about 0.1 μm while the active layer thickness was around 0.3 μm. The width of the waveguide was 1.4 μm.

(a)

$1.0\,\mu\mathrm{m}$

(b)
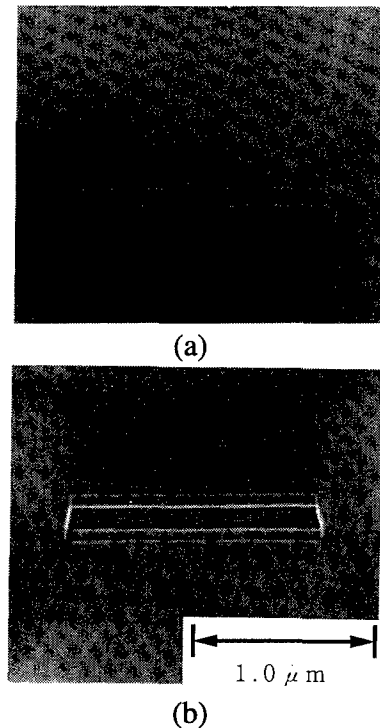
Fig. 5 Cross-section of (a) the structure at the facet of the tapered waveguide and (b) the active region

A buffer layer is inserted between the side wall of the dry-etched mesa and the p-InP blocking layer to eliminate Zn diffusion[20]. The thickness of each blocking layer is adjusted to keep the as grown surface flat because LD surface flatness is important for the application of the passive alignment between a LD and a passive waveguide. A 4-μm-thick p-InP over-cladding layer and a 0.5-μm contact layer are then grown on the

654

whole wafer. The surface of the device is almost perfectly flat except for the slight step of less than 0.2-μm above the mesa structure.

The device length for both the active and SS regions is 300 μm.

3. Characteristics

3-1. Uniformity

Figures 5-(a) to (c) show the averaged value distributions of the threshold current (Ith), full width of half maximum (FWHM) of horizontal, and vertical far-field patters (FFP) in the wafers. The devices measured are both cleaved. Each value is an average of 80 chips in each square region divided from the wafer.

(a)

(b) **(c)**
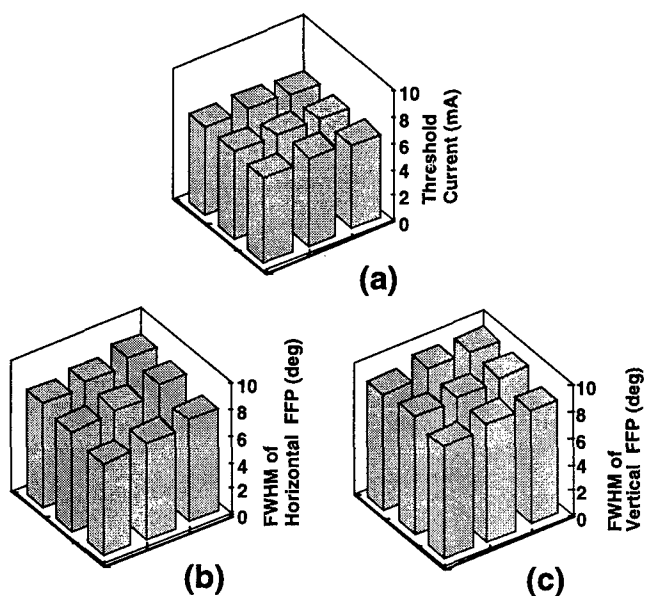
Fig. 5 Averaged value distribution in a 2-inch wafer. (a) Ith, (b) FWHM of horizontal FFP, (c) FWHM of vertical FFP

The average values of Ith, FWHM of horizontal, and vertical FFP are 6.6 mA, 7.7 °, and 8.9 ° respectively. STD of Ith is about 2% in the wafers, and those of FWHM of horizontal and vertical FFP are both 6%. The FFP variation are believed to be brought about a slight change of λg of taper-waveguide in the wafer.

Figures 6(a) and (b) show the cumulative distribution of Ith, and FWHM of horizontal and vertical FFP. More than 90% of the lasers had an Ith of less than 7 mA, FWHM of FFPs less than 8.5° and 9.5° in the horizontal and vertical directions.

(a)

(b)
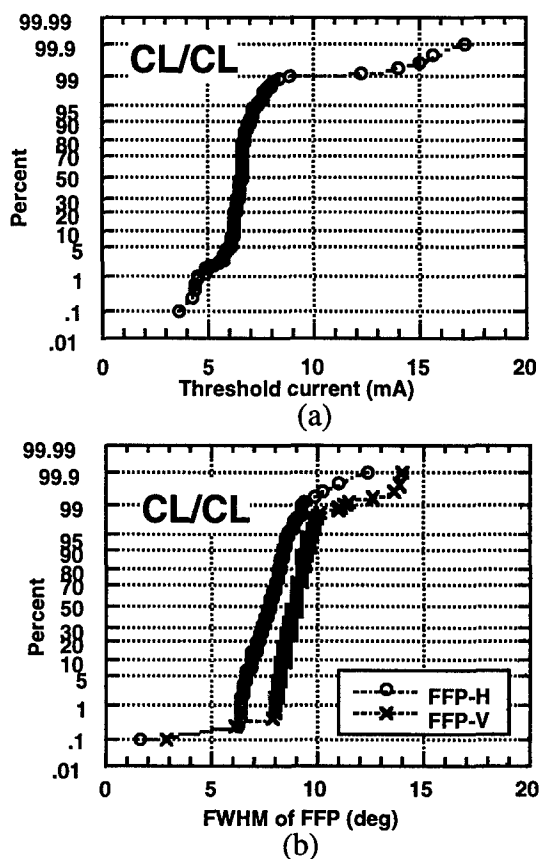
Fig. 6 Cumulative distribution of (a) Ith, and (b) FWHMs of horizontal and vertical FFP.

3-2. High temperature characteristics

Temperature dependence of light to current characteristics are shown in Figure 7. Ith were typically 5.6 and 15.8 mA at 25 and 85 °C respectively for the HR (95%) coated sample.

Fig. 7 Temperature dependence of light to current characteristics.

655
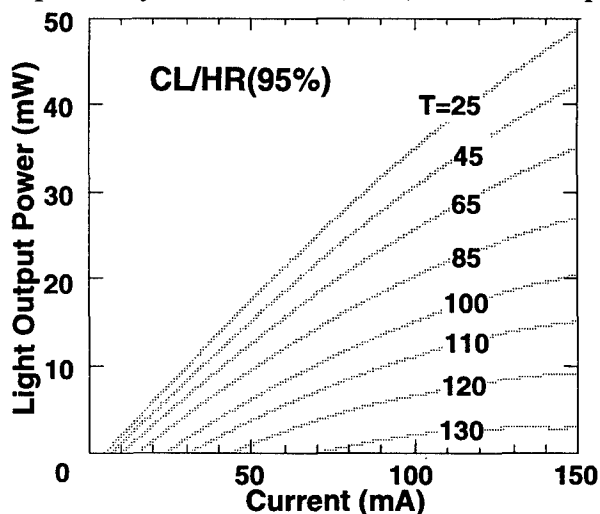
Output power of more than 50 mW was observed at 25°C. Moreover a maximum operation temperature of 134 °C was also achieved. The characteristic temperature of the threshold current up to 85 °C was 60 °C. The threshold current without the SS region was 3.9 mA and 12.4 mA at 25 and 85 °C. The difference reflects the loss of SS region. The loss in the SS region is estimated to be 12 cm^{-1}.

To confirm the temperature dependence of the coupling characteristics, the coupling losses to DSF were measured. The results are shown in Figure 8. The DSF is coated with anti-reflection film.
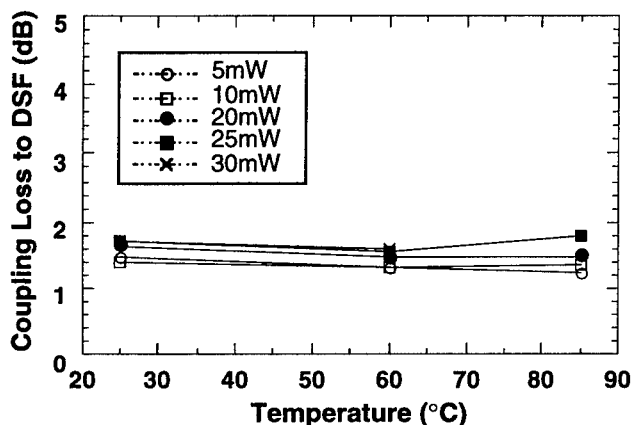
Fig. 8 Temperature dependence of coupling loss to DSF.

The coupling loss was stable at less than 1.8 dB in the temperature range from 25 °C to 85 °C and up to the high output power of 30 mW. This means that high temperature have little effect on the beam spot of the SS-LD.

4. Reliability

Long-term stability was confirmed for these lasers without screening. As shown in Fig. 9, on SS-LD has been operating under constant power operations (APC) of 10 mW at 60 °C for more than 4000 hours.
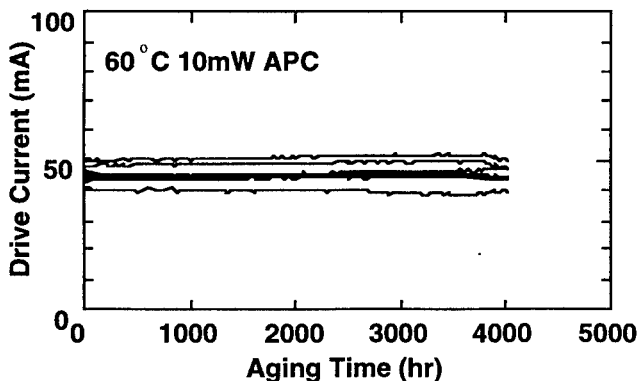
Fig. 9 Aging test under a constant output power of 10 mW at 60 °C

5. Conclusion

1.3-μm SS-LDs have been successfully fabricated by butt-joint for integration of SS region and dry etching for mesa structure. Uniformity with low threshold current and a narrow emitted beam are obtained using 2-inch full-wafer fabrication technology. Good high-temperature characteristics are demonstrated for threshold current, output power, and coupling. Long-term stability was also confirmed for the SS-LDs.

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Spot-size Expanded High Efficiency 1.3 μm MQW Laser Diodes with Laterally Tapered Active Stripe

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Abstract

A large spot-size laser diode (LD) with tapered active stripe has been realized. The threshold current and the slope efficiency were 14mA and 0.43 W/A, respectively at 85 °C. These characteristics are comparable to those of conventional straight stripe LDs. The full width at half maximum (FWHM) of lateral and vertical far field patterns (FFPs) were 14° and 16°, respectively. The maximum coupling efficiency of the tapered LD to a 10 μm φ -core single mode fiber was -6.2 dB and horizontal 1 dB-down tolerance was ±2.0 μm.

I. Introduction

Low cost optical module is strongly demanded, as the application area of optical communications is expanding to subscriber system and local area networks (LAN). Uncooled large spot-size laser diode (LD) is a key device to realize a low cost optical module, because a temperature controller and a lens can be eliminated and wide alignment tolerance reduces assembly cost.   Although several types of spot-size converted LDs (SSC-LDs) have been proposed so far[1],[2],[3], a tapered active stripe SSC-LD[4] is attractive, compared with tapered passive transformer integrated LDs. This is because no complicated fabrication processes are needed, and shorter cavity (~300 μm) leads to higher production yield, which is essential for cost effective LDs.

However, it is crucial for the SSC-LDs to achieve excellent temperature characteristics by compensating both additional loss along the tapered waveguide and reduced optical confinement factor Γ. This paper reports tapered active stripe LDs with improved fiber coupling and excellent temperature characteristics.

II. Experimental
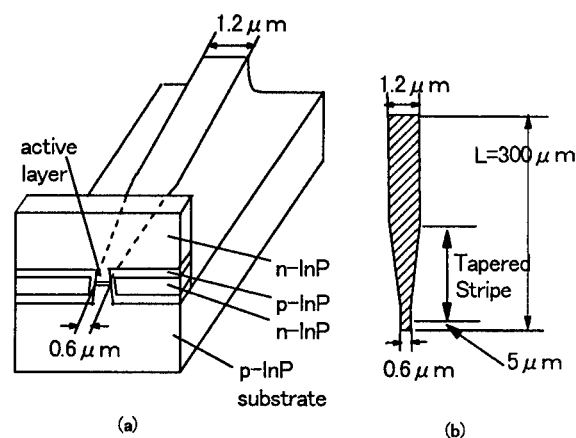
Fig. 1. Schematic structure of the LD (a) and the stripe profile (b). The cavity length is 300 μm, while the tapered length varies from 45 to 295 μm.
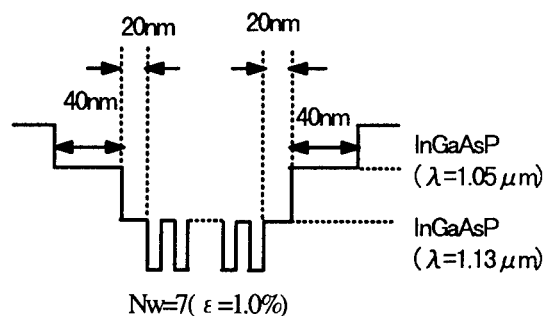
Fig.2 Schematic band diagram of the active region. Two-step SCH layers were employed to reduce carrier spill-over from MQW into SCH.
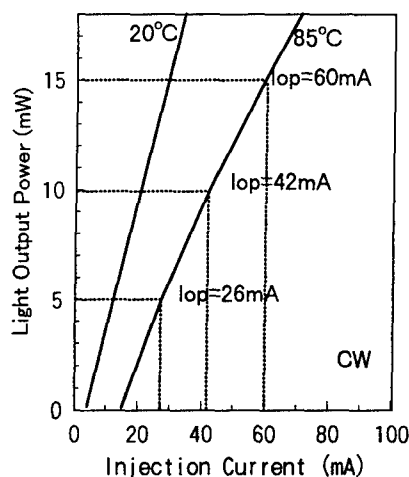
Fig.3 Light output power versus operating current characteristics. Cavity length was 300 μm with cleaved front facet and 95 % coated rear facet. Tapered stripe length was 45 μm.

(a)

(b)

Fig. 4 Threshold current (a) and operating current (b) characteristics as a function of tapered stripe length.

Figure 1 shows a schematic structure of the fabricated LDs. Base epi-wafers for the LDs were entirely grown by metal organic vapor phase epitaxy (MOVPE) on p-InP substrates. The epi-wafer was chemically etched to tapered mesa stripes. To reduce carrier leakage current flowing outside an active region, pnp current blocking layers were employed[5]. This fabrication process is almost the same as that of conventional straight stripe LDs. The front and rear active stripe width are fixed to 0.6 μm and 1.2 μm, respectively. The LD has a fixed cavity length of 300 μm with a front facet cleaved and a rear facet 95 % coated, while the tapered stripe length ranges from 45 μm to 295 μm, as shown in Fig.1(b).

An active region consists of compressive 1.0 % strained seven InGaAsP quantum wells (MQW) separated by InGaAsP (λg=1.13 μm) barriers, as shown in Fig.2. Two-step separated confinement heterostrucure (SCH), consisted of 20 nm thick InGaAsP (λg=1.13 μm) and 40 nm thick InGaAsP (λg=1.05 μm), was introduced. The SCH layers are effective to reduce carrier spill-over from the MQW into SCH layers at high temperatures[6]. After MOVPE growth, n-side and p-side electrodes are formed.

III. Results and Discussion

Figure 3 shows a temperature dependence of light output power versus operating current characteristics for a 45 μm-long tapered stripe LD. The threshold current were 3 mA and 14 mA at 20 °C and 85 °C, respectively. The slope efficiency were 0.60 W/A and 0.43 W/A at 20 °C and 85 °C, respectively. The operating current at 10 mW and 15 mW were as low as 42 mA and 60 mA, respectively at 85°C. These values are almost comparable to those for conventional straight active stripe LDs. The threshold and operating current increased as tapered stripe length increased, as shown in Fig.4, due to increase in carrier leakage flowing outside the active region for the active layer width less than 1.0 μm. However, the threshold and operating current increase was negligible for the tapered stripe length less than 100 μm.
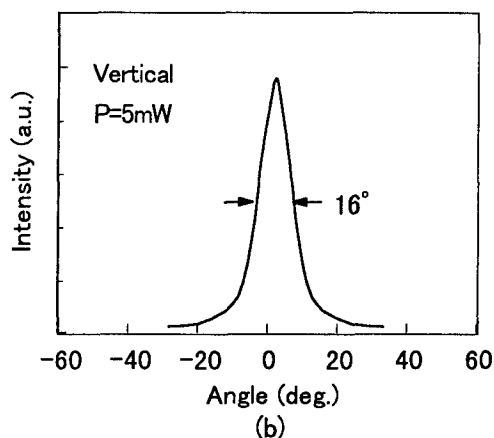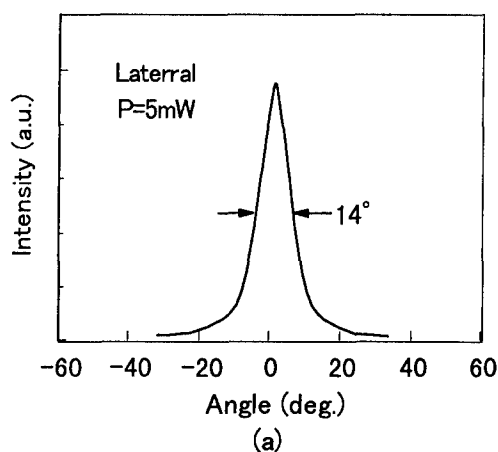
Fig.5 Experimental lateral and vertical far field patterns (FFPs) for the LD with 295 μm long tapered region.

Fig.6 Experimental full width at half maximum (FWHM) for lateral (a) and vertical (b) as a function of tapered stripe length. Calculated lateral FWHM is also shown (a).

Figures 5 (a) and 5 (b) show lateral and vertical far field patterns (FFPs) at 5 mW output for the LD with 295 μm-long tapered stripe. Single mode peaks were observed. The full width at half maximum (FWHM) of the lateral and vertical FFP were 14° and 16°, respectively. By introducing tapered stripe, the FWHM of FFPs were reduced to 60~70 % of those for conventional straight stripe LDs, as shown in Fig.6 (a) and (b). In Fig.6(a), calculated lateral FWFM, based on equivalent refractive index method, is also shown as a dotted line. The lateral FWHM decreases as the tapered stripe length increases. However, the dependence becomes weak for the tapered stripe length greater than 100 μm. Experimental lateral and vertical FWHM slightly changed from 16° to 14°, 17° to 16°, respectively, as the tapered stripe length increased from 45 μm to 295 μm. A little discrepancy between the calculated and the experimental results may be caused by parameter difference in the equivalent refractive index.

Butt-coupling efficiency to a normal flat-end 10 μm φ core diameter single mode fiber (SMF) was investigated, as shown in Fig.7. The minimum coupling loss was 6.2 dB at Z-axis displacement of 20 μm. Horizontal 1dB-down tolerance was ±2 μm at Z= 20 μm. The coupling efficiency was improved by 3 dB, compared with conventional straight active stripe LDs.

IV. summary

We have achieved the beam spot-size expanded uncooled laser diode with short cavity laterally tapered active stripe. The minimum operation current for 10 mW output power was as low as 42 mA at 85 °C. The FWHM of lateral and vertical FFP were
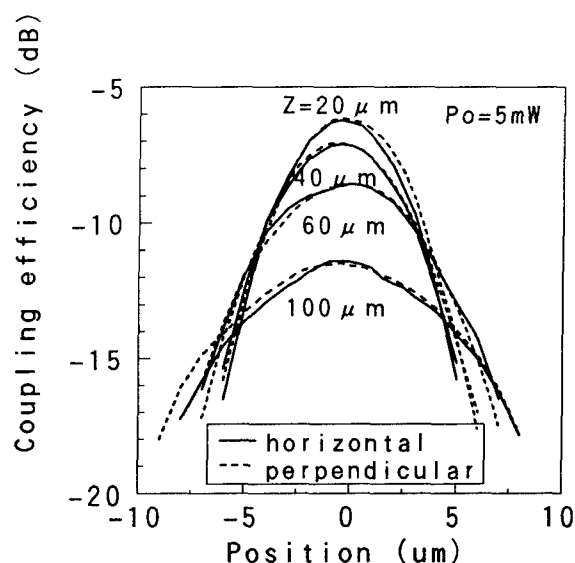
Fig.7 Experimental coupling efficiency of the fabricated LD to a 10 μm core diameter single mode optical fiber.

14° and 16°, respectively. The coupling efficiency to SMF was improved by 3dB, compared with conventional LDs. This performance makes it possible to realize cost-effective optical module for practical use in optical access networks.

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BUTT JOINED INTEGRATED GaInAsP MQW LASER AND WAVEGUIDE GROWN BY SELECTIVE CBE

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Introduction

We report the successful realization of 1.55 μm buried MQW SCH lasers with all quaternary quantum wells and butt joint between laser and waveguide structure by the selective in-filling growth of laser structures into etched grooves. The grooves were etched into the basic layers, e.g., InP or the waveguide structure, grown in a preceding epitaxial run. These structures were contacted and cleaved to stripe lasers of different length and width. The electrical and optical performance of laser diodes for different substrate orientation, aperture of grooves and basic layer design were studied. 220 μm long buried 6 QW lasers grown into 3 μm wide grooves, etched in an exactly oriented substrate showed threshold currents less than 10 mA for cw operation at 20°C. 6 QW SCH laser structures were grown into basic waveguide layers, giving a butt joint. By comparing the threshold current of butt joined and cleaved lasers, coupling coefficients between 60% to 80% were estimated.

I. Background

We have previously shown the high quality of strained and strain symmetrized all quaternary (GaIn)(AsP) MQW structures grown by Chemical Beam Epitaxy (CBE) (1). The high growth selectivity and the in-filling growth of (GaAs)(InP) makes CBE an ideal tool for monolithic integration of optoelectronic devices. There are two concepts for the integration of active and passive structures, e.g. laser and waveguide or blocking layers:

(a) The active layers are grown first. After patterning and etching the required lateral structures, passive layers are regrown (Fig. 1.a).

(b) The passive layers are grown first. The active structures are grown in the regrowth step into the grooves, patterned and etched in the passive layers (Fig. 1.b).

Smaller interaction of active materials with the epitaxy mask (Si_3N_4) or blocking layers (Fe-doped InP for semiisolation), lower thermal stress during the regrowth step and reduced crystal damage caused by lateral processing and etching of the active layers are the main advantages of the second concept. However the shadow effects and the lateral growth on the side walls of etched grooves can result in growth distortions and electrical shorts in the final structures. In this work we show the realization of buried MQW laser structures and laser/waveguide butt joint following the second concept.

II. Buried 6 QW structures: Fabrication

A 100 nm Si_3N_4 layer, deposited and patterned by PECVD and optical lithography simultaneously formed the etch mask, epitaxy mask and later p-contact isolation mask. Either wet chemical etching or ECR/RIE ($CH_4/H_2/N_2$) was used to etch grooves of 1.4 μm depth and different widths in InP basic layer. The latter etch nearly rectangular groove profiles in all direction, while the chemical wet etching with $HCl:H_3PO_4$ yielded perfectly rectangular profiles for grooves in [011] direction only. An etch stop layer consisting of 50 nm GaInAsP (λ_{PL} = 1.2 μm) ensured homogeneous etch depth in this case. To reduce the lateral growth on the side walls, the grooves were etched laterally with $HCl:H_2O$ solution, giving a 300 nm wide undercut under the Si_3N_4 mask.

Subsequently the grooves were filled with 700 nm InP:Si buffer layer. Decreasing the growth rate for high V/III ratios enforced the planar growth of the buffer.

The active layer was then grown on this buffer, followed by
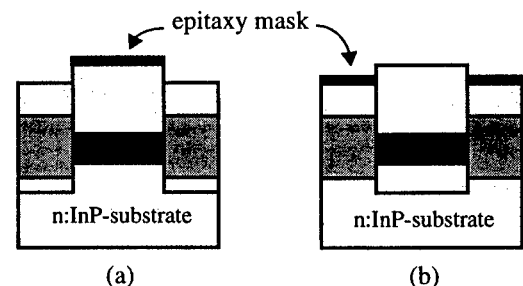
Fig. 1: Schematic diagram for the two possible integration concepts. (a) The active layers are grown first. (b) The passive layers are grown first. The active layers are then grown in the grooves, etched into the passive basic layers (in-filling).

1300 nm InP:Be p-cladding and 200 nm GaInAs:Be p-contact layer.

The samples were processed and cleaved to stripe lasers. To describe the influence of material and basic layer composition and substrate orientation we compare four samples (A to D) with differing growth and processing. All samples are 6 QW SCH lasers.

The active layer of sample A consists of a ternary/quaternary SCH laser structure with six compressively strained GaInAs quantum wells each 5 nm thick and 10 nm thick GaInAsP (1.2 µm) barriers, sandwiched between two 120 nm thick GaInAsP (1.2 µm) SCH layers. This structure was buried in an undoped InP basic layer grown in a first epitaxial run.

Sample B,C and D consist of the all quaternary step graded SCH laser structure with six 1.2 to 1.3% compressively strained quantum wells, described in [1]. 20 alternating p- and n-doped InP layers each 50 nm thick form the basic structure of sample B. The basic structure of sample C consists of an etch stop layer, a 400 nm undoped InP layer and the alternating p- and n-doped InP layers (same as B). The basic layer of sample D is similar to C, however, instead of the alternating p-n-doped layers, a 1000 nm thick insulating InP layer (Fe-doped) was used to confine the current flow. For A and B the grooves were etched by ECR/RIE. For C and D the grooves were etched using the chemical wet etching technique, described above.

The epitaxy of A,B and C was carried out on 2°off oriented 2" n:InP substrates, whereas sample D was grown on an exactly oriented one. For all samples the grooves were parallel to [011] direction. The growth temperature was 540 °C.

III. Buried 6 QW structures: Characterization

Starting with the exponential dependence of threshold current density (J_{th}) and cavity length (L) (see (1) and (3)), we fitted the measured threshold current densities to extract the extrapolated threshold current density for infinitely long cavity $(J_{th,\infty})$. The internal loss (α_i) and the internal differential quantum efficiency (η_i) were obtained by measuring the external differential quantum efficiencies for different cavity lengths. Fig. 2 shows the LI-diagrams for lasers of same geometry for each sample, demonstrating the improvement of laser performance from A to D. Table 1 summarized the characteristics of these samples. For 3 µm wide structures the minimal achievable threshold current $(I_{th,min})$, is calculated from exponential dependences.

Comparing the broad area lasers in sample A and B, in B a lower extrapolated threshold current density and a higher internal quantum efficiency were measured. This is mainly because of the higher strain in all quaternary MQWs and the step graded SCH structure in B (see (1)). Nevertheless the threshold currents for narrow grooves of 3 µm width were in both samples still high. The measurements showed also large spread of data for narrow grooves, which makes a reliable fit to data, in case of sample B problematic. This is due to the lateral growth on the side walls, which forms sporadically electrical shorts.

Using wet chemical etch techniques for sample C and D, reduced the lateral growth on the side walls and prevented the
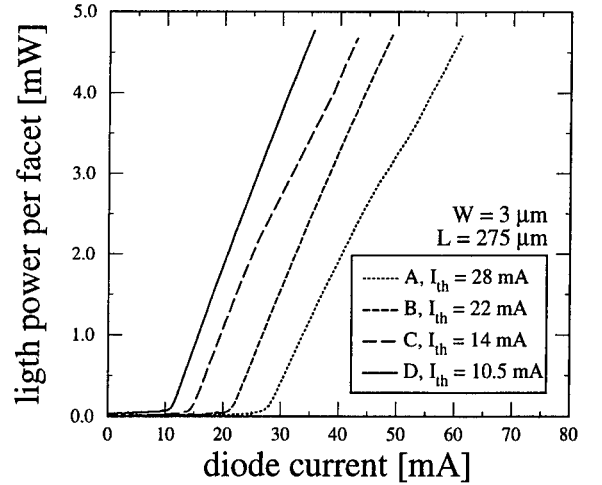
Fig. 2: Comparison of ligth output for different buried 6 QW lasers. The cavity geometry is for all four sample identical.

Table 1: Comparison of laser characteristics for sample A to D.

Sample	A	B	C	D
quantum well	T/Q	Q/Q	Q/Q	Q/Q
substrate	2° off	2° off	2° off	exact
basis	not doped	p-n-doped	p-n-doped	Fe-doped
process	RIE	RIE	Wet	Wet
$J_{th,\infty}$ broad area	620* A/cm²	500 A/cm²	430 A/cm²	420 A/cm²
α_i broad area	17* cm⁻¹	16 cm⁻¹	12 cm⁻¹	26 cm⁻¹
η_i broad area	35%*	80%	70%	85%
$J_{th,\infty}$ 3 µm wide	1980 A/cm²	1900* A/cm²	740 A/cm²	670 A/cm²
α_i 3 µm wide	24 cm⁻¹	23* cm⁻¹	26 cm⁻¹	29 cm⁻¹
$I_{th,min}$ 3 µm wide	24 mA	15* mA	12 mA	9.5 mA

* evaluation problematic due to electrical shorts

electrical shorts. The spread of data was negligible. Fig. 3 shows the cross section of sample C and D. Sample D, grown on an exactly oriented substrate in Fe-doped basic structure, showed perfectly symmetrical growth. For 3 µm wide 220 µm long buried lasers at 20°C a threshold current of 9.5 mA and an external differential quantum efficiency of 55% were measured

(Fig. 4). Pulsed and cw operation were identical.

For grooves wider than 10 μm, e.g. material imigration length, the growth follows the direction induced by substrate. The growth in narrower grooves yet seems to follow the [100] direction for both substrate orientations. This is related to the step bunching in the narrow grooves (see (2)). For the 2° off oriented substrates (samples A,B and C) this yields a slight tilt of growth plan against the substrate surface, which in worst case can cause parasitic current paths. Futhermore for samples A, B and C the optical losses decrease gradually with the increasing groove widths (from 25 to 15 cm^{-1}). For sample D though, it remains rather constant (around 27 cm^{-1}), approving
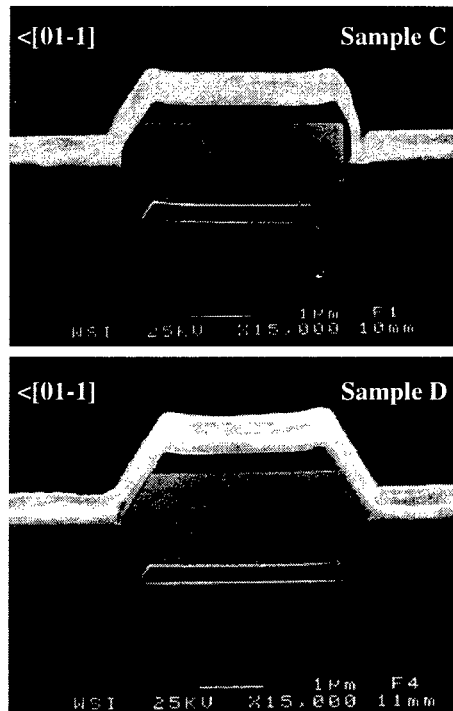
Fig. 3: Cross section of 3 μm wide lasers for samples C and D. The tilt against [100] direction for sample C corresponds to the 2° off orientation of the substrate.
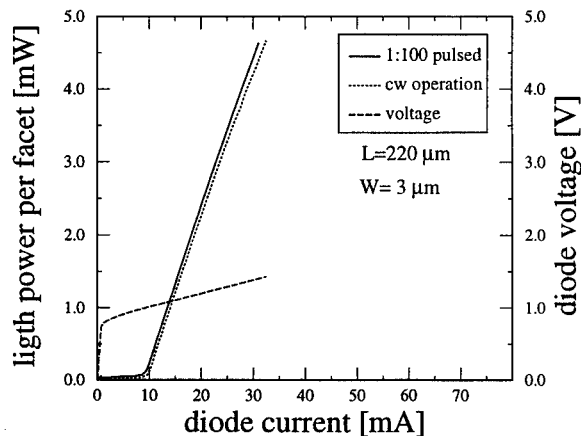
Fig. 4: The LI-diagram of a 220 μm long buried 6 QW lasers. Pulsed and cw operation are identical.

the change in growth mechanism for narrow grooves in off oriented substrates. A similar difference in optical losses were also measured for broad area lasers grown planarly on 2° off and exactly oriented substrates.

IV. Butt joint structures: Fabrication

Fig. 5a shows schematically the laser/waveguide butt joint structure. The laser and waveguide were designed to achieve a high overlap of optical fields. We used a combination of both ECR/RIE and wet chemical etch techniques to etch broad area grooves in basic waveguide structures. A 30 nm GaInAsP (1.2 μm), grown ahead of the waveguide, ensured the homogenous etch depth and was removed before the second growth step. Subsequently the 6 QW step graded SCH laser structure were grown selectively in these grooves, forming the laser/waveguide butt joint. To achieve the lateral confinement of optical mode, ridges in [01-1] direction were etched in laser and waveguide areas, simultaneously. The 50 nm thick GaInAsP (1.1 μm) on the laser section and the waveguide core on the waveguide section were used to control the ridge height. P-contacts were patterned to the laser sections. Samples were cleaved giving modules with a MCRW laser section and a waveguide section, coupled through the butt joint. Reference lasers without the waveguide section were cleaved for comparison. Fig. 5b shows the cross section along such a module. The
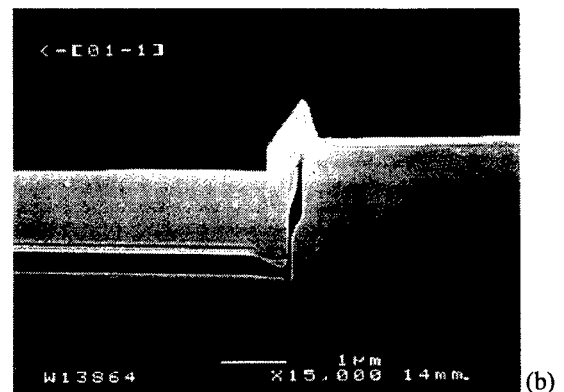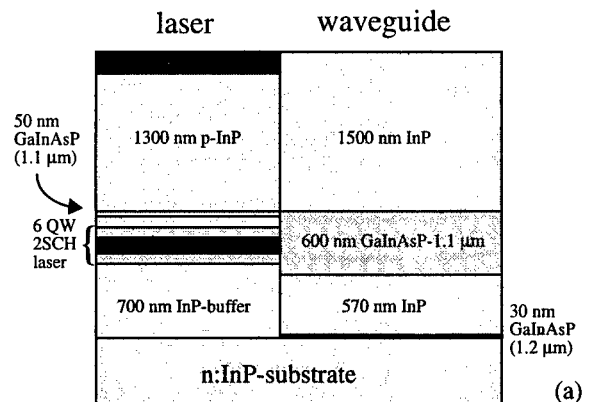
Fig. 5: Schematic diagram and the cross section of laser/waveguide butt joint. Butt joint plan is perpendicular to the picture plan.

663

etch stop layer under the waveguide core (right side) and the active layers and the etch stop layer on the laser section (left side) are well distinguishable. The disturbed growth region is at most 1 μm thick.

V. Butt joint structures: Characterization

The additional optical losses at the butt joint (e.g. scattering), increase the threshold current for a coupled laser/waveguide resonator, comparing with a reference laser of the same laser length. Fig. 6 compares the LI-diagrams of such a module (threshold current 18 mA) and a reference laser (threshold current 15.5 mA), both with 4 μm ridge width. The waveguide section is 450 μm long. The reference laser and laser section are both 220 μm long.

The coupling efficiency can be expressed in terms of butt joint transparency (T), that is the part of optical power which remains in the resonator and is not scattered at the butt joint. Assuming negligible waveguide losses (1.1 μm GaInAsP core) and back reflection of optical power at the butt joint, only an additional optical loss, $ln(1/T)$, should be added to mirror losses, $ln(1/R)$, to describe the exponential dependence of new threshold current density (J^*_{th}) and laser section length (L):

$$J^*_{th} = J_{th,\infty} \cdot exp\left(\frac{ln\left(\frac{1}{R}\right) + ln\left(\frac{1}{T}\right)}{\Gamma_N \cdot g_0 \cdot L}\right)$$

$J_{th,\infty}$ is the threshold current density for infinitely long cavity, Γ_N the confinement factor for N (= 6) quantum wells, g_0 the gain constant and R the facet reflexivity (≈ 0.3). This suggests an increase in optimal length (L^*_{opt}) for the laser/waveguide modules:

$$L^*_{opt} = \frac{ln\left(\frac{1}{R}\right) + ln\left(\frac{1}{T}\right)}{ln\left(\frac{1}{R}\right)} \cdot L_{opt}$$

Fig. 7 depicts the threshold current density of laser/waveguide modules and reference lasers with 7 μm ridge width as a function of reciprocal laser section length. The optimal length is proportional to the slope of the curves. With this method a coupling coefficient of 70% (± 10%) for 4 and 7 μm wide ridges was estimated. For broad area lasers (30 μm) this is higher (80%).

VI. Conclusion

Buried SCH lasers with 6 quantum wells and laser/waveguide butt joints were grown selectively by CBE, using the in-filling concept. Independent of the substrate misorientation, the growth in the narrow grooves follows the [100]-direction. Suppressing the disturbing effects of lateral growth, buried SCH lasers with threshold currents less than 10 mA with very good performance were fabricated. From the dependence of threshold current densities on laser length for laser/waveguide modules and reference lasers, butt joint coupling coefficients up to 80% could be estimated.

We conclude that CBE fulfills the main requirements for monolithic integration of optoelectronic devices.
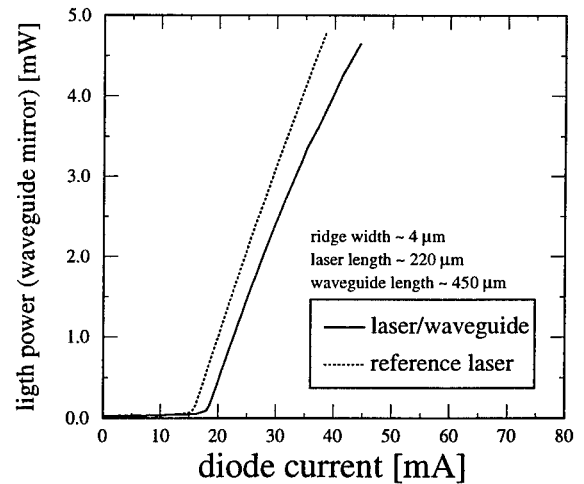
Fig. 6: Comparison between LI-diagrams of a laser/waveguide module and a reference laser. The laser section and the reference laser are both 220 μm long.
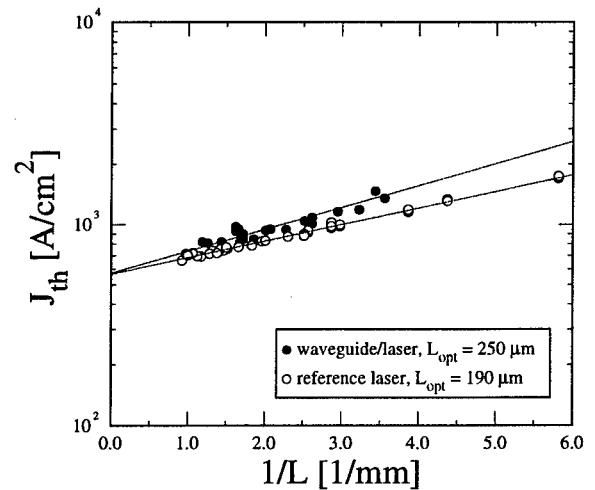
Fig. 7: The threshold current density (J_{th}) of 7 μm wide laser/waveguide modules and reference lasers as a function of inverse of laser section length (L).

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Two-Section InGaAsP DBR-lasers at 1.55 μm wavelength with 31 GHz Direct Modulation Bandwidth

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Abstract

The small signal modulation response of two-section InGaAsP DBR-lasers at 1.55 μm wavelength was investigated. The response was fitted to a general transfer function and it was found that for almost all lasers the response could be described by a three pole model consisting of the laser response from the standard rate equations and an additional first order low pass roll-off. The lasers exhibited reduced damping and increased resonance frequency due to what we believe is detuned loading. This led to a maximum bandwidth of 30 GHz for lasers described by the three pole model. Some lasers exhibited an additional effect which we believe is cavity resonant enhancement of one of the modulation side-bands. This effect increased the maximum -3dB bandwidth to 31 GHz but could not be described by a three pole model.

I. Introduction

The directly modulated laser is a simple and reliable source for high speed optical information transmission. It is especially useful in medium to short distance applications (e.g. local area networks and optical interconnects) where the excess pulse broadening due to laser chirp is not a critical issue.

The laser modulation response can in most cases be described with a three pole transfer function. The modulation bandwidth is then usually determined by the maximum achievable resonance frequency (f_r), the damping of the resonance peak (Γ_r) and possible additional parasitic-like roll-off due to contact parasitics or diffusion-limited transport through the separate confinement layers [1]. For FP-lasers and single section DFB-lasers it is found both theoretically and experimentally that the damping of the resonance peak is approximately proportional to the square of the resonance frequency. This relation leads to a limit of the modulation response, K-factor limit, that is mainly determined by the ratio between the nonlinear gain coefficient and the differential gain coefficient of the active material [2]. However, this is not true in DBR-lasers or inhomogenously pumped multi-section DFB-lasers in which the dispersive effects of the Bragg grating, detuned loading [3], can alter both the frequency of the resonance peak and its damping.

II. Design and Fabrication

We have investigated two section InGaAsP DBR-lasers. The lasers were designed to utilize detuned loading effects, i.e. the length of the sections and the coupling coefficient were chosen to obtain large mode spacing compared to the width of the Bragg reflection peak so that lasing could occur far down on the slope of the reflection peak. The lasers had 100-200 μm active sections and 300 μm passive Bragg-sections with a coupling coefficient estimated to 80 cm⁻¹, Fig. 1. Bragg and active sections were connected by butt-joint regrowth. The active structure consists of 12 $In_{0.74}Ga_{0.26}As_{0.85}P_{0.15}$ wells, 7 nm thick with 1 % compressive strain, separated by $In_{0.46}Ga_{0.54}As_{0.85}P_{0.15}$ barriers, 8 nm thick with 0.9 % tensile strain. The active structure is surrounded by a symmetrical box of 22 nm InGaAsP λ=1.3 μm on each side. The grating section consists of a 10 nm InP buffer layer, a waveguide consisting of 20 lattice-matched 10 nm thick wells, with corresponding bulk bandgap wavelength of 1.45 μm, and InP barriers of 10 nm thickness. On top of the waveguide is an InP spacer layer of 50 nm thickness followed by a lattice matched grating layer, with a bandgap wavelength of 1.45 μm.

Two different transverse structures were used for current confinement: the semi-insulating buried heterostructure (SI-BH), Fig. 1, and the Semi-Insulating Flat-surface Buried Heterostructure (SI-FBH) with Ground Source Ground (GSG) contact configuration, Fig. 2. All the epitaxial layers were grown by MOVPE except the semi-insulating which was grown by Hydride Vapor Phase Epitaxy (HVPE). To obtain low chip capacitance both SI-FBH and SI-BH structures were

etched into 5 μm high mesas by reactive ion etching (RIE), and thereafter regrown with semi-insulating iron doped InP. In addition, the metal on the epi-side was made only 50 μm wide. Electrical isolation between the two sections was obtained by removing the contact layer in between and ion implantation (H⁺). The rear facets were AR-coated to reduce reflections.
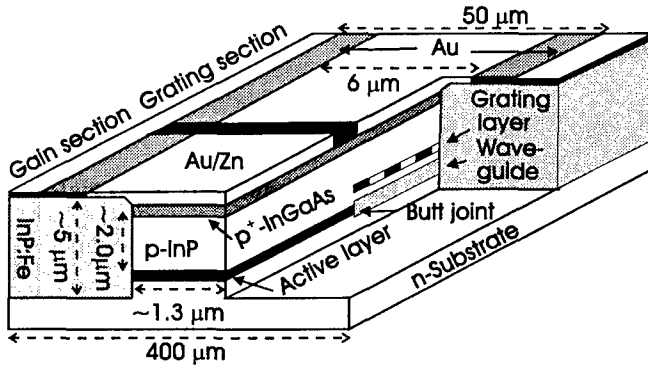
Fig. 1. Schematic of the SI-BH DBR-laser.
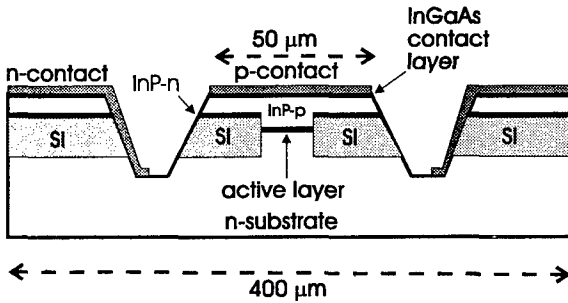
Fig. 2. Cross-section of the transverse structure of the SI-FBH structure with GSG contact configuration.

III. Measurements and Results

A Wiltron 360 Network Analyzer together with a New Focus 1014 detector and a Picoprobe coaxial probe were used for the response measurements. The measurements were calibrated for the detector response. However, the intensity dependence of the detector response and probe losses were not taken into account (~ -1dB@30 GHz). Calibrated data, both magnitude and phase were fitted to a general model. For almost all lasers a three pole model could well describe the response and the resonance frequency, the damping factor and the parasitic-like roll-off frequency were extracted.

The best laser in this investigation that could be described by a standard three pole model exhibited a -3dB small signal modulation bandwidth of 30 GHz at room temperature and 130 mA bias current, Fig. 3. This is to our knowledge the highest reported value for direct modulated single mode 1.55 μm lasers.
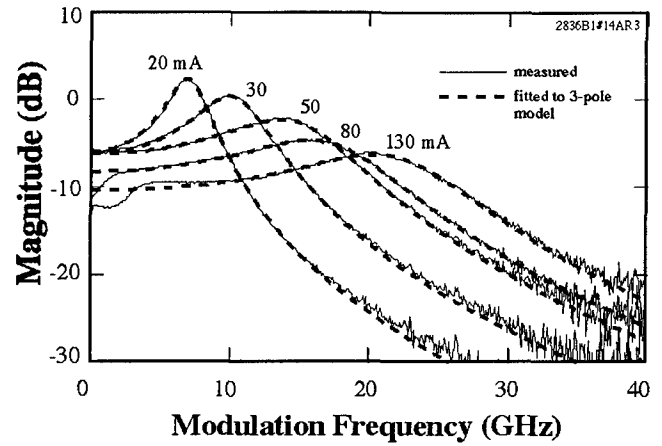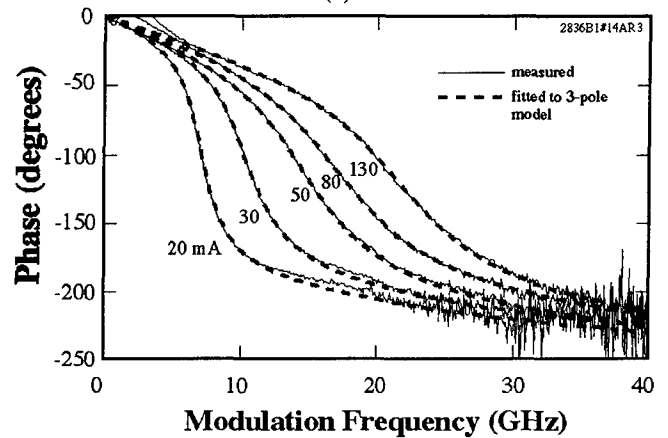
Fig. 3. Small signal modulation response at different bias currents. The response is well described by a three pole model and has a -3dB bandwidth of 30 GHz. a) Magnitude. b) Phase.
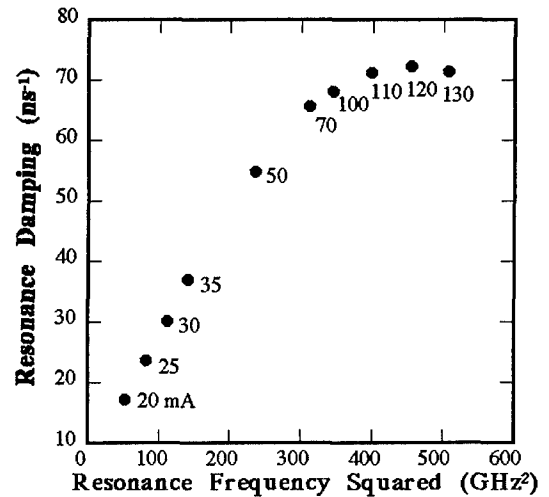
Fig. 4. Damping factor plotted versus the square of the resonance frequency for different bias currents for the same laser as in Fig. 3. The sublinear behavior can be attributed to detuned loading effects.

Several lasers exhibited a sublinear relationship between the damping factor and the square of resonance frequency especially at higher currents, Fig. 4. In some lasers the damping of the resonance peak even decreased as the current and resonance frequency increased which in a few cases ultimately led to self-pulsation at the resonance frequency [4]. Similiar self pulsations has also been observed in multi-section DFB-lasers [5].

(a)

(b)
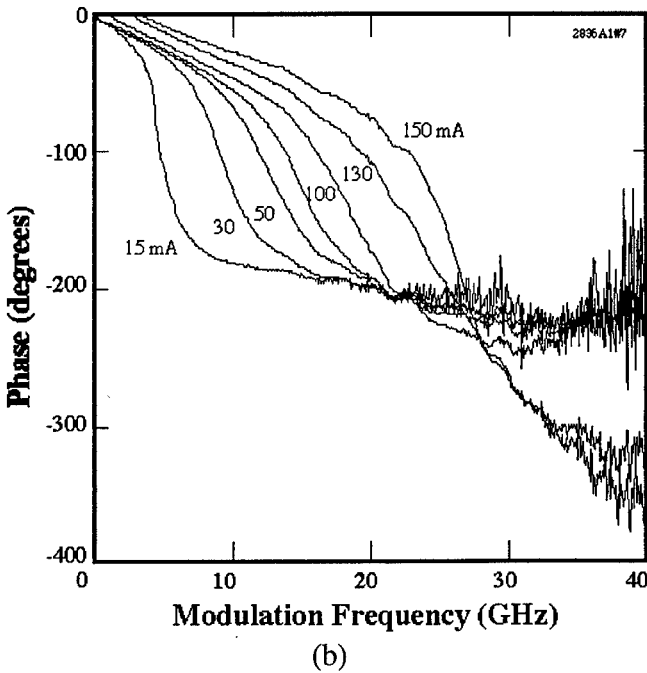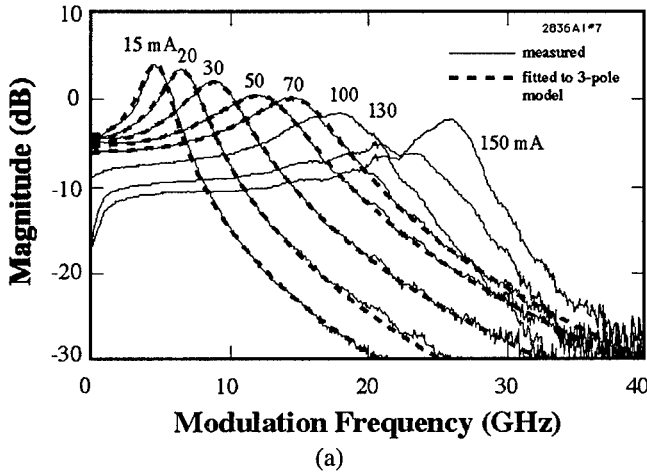
Fig. 5 Small signal modulation response for a laser with 31 GHz bandwidth which exhibits modulation enhancement at high frequencies for bias currents more than 70 mA. This effect can not be described by a three pole model . a) Magnitude. b) Phase.

In a few lasers we observed at high bias an additional resonance-like peak which lifted the modulation response and increased the bandwidth. The highest bandwidth measured for a laser with this kind of behaviour was 31 GHz, Fig. 5. At

frequencies beyond this peak, the response fell off considerably faster than for a three pole model. For lasers where the extra peak almost coincided with the resonance frequency or was at slightly higher frequency like in Fig. 5 this peak lifted the response and increased the bandwidth. In lasers where the peak appeared at much higher frequency than the resonance, the bandwidth was not increased since the response fell below -3dB between the resonance frequency and the extra peak.

IV. Discussion

For multi-section lasers, where the photon distribution and the mirror loss change during modulation, the standard rate equation for photons has to be modified [6].

$$\frac{dS}{dt} = (\Gamma(N)G(N,S) - \gamma_i - \gamma_m(N) + \frac{1}{2}\frac{d\ln(K_z(N))}{dt})S \quad (1)$$

Here, S is the photon number and N is the carrier number, $\Gamma(N)=\Gamma_{xy}\Gamma_z(N)$ is the fraction of S that occupies the active layers (confinement factor), G(N,S) is the material gain in the active section times the group velocity, γ_i and $\gamma_m(N)$ are the internal loss rate and mirror loss rate, respectively. Finally, $K_z(N)$ is the longitudinal excess spontaneous emission factor. The last term in (1) should be included when a time dependent mode expansion is used and it is this term that can explain the observed reduction of the damping. Physically this term represents the net optical energy that is produced during the short but finite time it takes for the optical mode, and hence $\gamma_m(N)$ and $\Gamma_z(N)$, to respond to a change of the carrier density [6].

A small signal expansion of the rate equations, using the modified rate equation (1) for the photons, yields the expressions (2) and (3) for the resonance frequency and damping factor respectively.

$$f_r = \frac{1}{2\pi}\sqrt{(\gamma_m + \gamma_i)S\frac{\partial}{\partial N}(\Gamma G - \gamma_m)} \quad (2)$$

$$\Gamma_r = \frac{1}{\tau_d} + \left(\frac{\partial(\Gamma G)}{\partial N} - \Gamma\frac{\partial G}{\partial S} + \frac{1}{2}(\gamma_m + \gamma_i)\frac{\partial\ln(K_z)}{\partial N}\right)S \quad (3)$$

From these expressions we can see that the derivatives on N can either enhance or decrease f_r and Γ_r. These derivatives depends critically on the detuning of the lasing mode with respect to the Bragg peak. When the laser is lasing on the long wavelength side of the Bragg peak they will increase f_r and decrease Γ_r. The sublinear relationship between Γ_r and the square of f_r seen in Fig. 4. can be explained with an increase of the detuning with increasing bias.

The observed reduction and in some cases even cancellation of the damping factor in the examined DBR-

667

lasers show that the damping limit governed by the K-factor can be overcome by using a multi-section design. How much the bandwidth can be increased by detuned loading effects remains, however, to be investigated.

A possible explanation for the extra resonance peak seen in Fig. 5. could be that one side-band of the modulated signal coincides with a side mode of the cavity and becomes resonantly amplified. In DBR-lasers unlike FP lasers the cavity modes can be spaced much closer in optical frequency than the length of the device implies. The strong dispersion of the Bragg grating can cause the total round trip phase to decrease with optical frequency in a limited frequency interval. The result is a kink in the round trip phase versus optical frequency curve so that three wavelengths can fulfill the phase condition with the same round-trip phase. This leads to two stable and one unstable mode where the unstable and one of the stable modes can be arbtrarily close in wavelength [7].

V. Summary

We have observed a record high modulation bandwidth of 30 GHz for 1.55 μm single mode lasers. The bandwidth was obtained by a two-section InGaAsP DBR lasers where the response can be well described by a three pole transfer function. We attribute this bandwidth to detuned loading. We also report a bandwidth of 31 GHz for lasers where the response is increased by an additional effect which we believe is resonant enhancement of one of the modulation side-bands due to coincidence with a cavity mode.

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MONOLITHIC INTEGRATION OF LASER AND WAVEGUIDE USING A TWIN-GUIDE STRUCTURE WITH ABSORPTION LAYER

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Abstract We demonstrate for the first time the use of absorption layer to achieve mode control in an InP/InGaAsP integrated twin-guide (TG) laser structure. The $In_{0.53}Ga_{0.47}As$ layer eliminates the even mode and makes characteristics of the integrated device insensitive to laser cavity length and structure variations, without degrading performance. A record high coupling efficiency of 45% from the TG laser to the integrated passive waveguide is obtained.

Introduction

The Twin-Guide (TG) structure is attractive for photonic integration because of its simplicity, and the fact that only one growth step is needed to prepare a structure on which various active and passive devices can be fabricated. Suematsu, et al. [1] demonstrated the first TG laser consisting of vertically integrated active and passive waveguide layers which were phase-matched in a manner similar to a directional coupler [5]. The resulting periodic coupling of light between the two waveguides unfortunately makes the etched facet feedback a function of the cavity length [2]. Therefore the threshold current and the amount of power coupled into the passive waveguide in conventional TG structure are extremely difficult to control. [4]

Here, we demonstrate for the first time the use of an $In_{0.53}Ga_{0.47}As$ absorption layer to suppress lasing on the even mode of the TG structure. This results in the laser facet feedback and coupling efficiency independent of cavity length. We used this novel structure to demonstrate the monolithic integration of a 1.55 µm wavelength, InP/InGaAsP MQW laser with a passive waveguide.

Figure 1 shows the refractive index profile and the two modes of the TG structure. The InGaAs absorption layer is placed midway between the waveguides to introduce additional loss for the even mode, with negligible effect on the odd mode. Therefore the odd mode is favored in this structure.
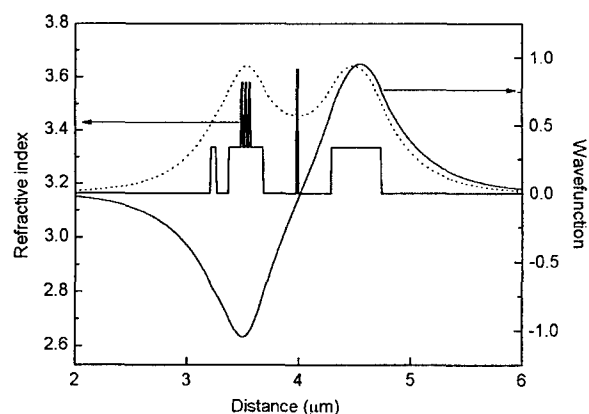
Figure 1. Refractive index profile and two modes of the TG structure.

Fabrication

The twin-guide structure, designed to operate at 1.55 µm wavelength, was grown by gas-source MBE on a (100) n-type InP:Si substrate in a single growth run. It has two stacked waveguiding layers separated by a 0.6 µm thick coupling layer. The upper waveguide contains a multiple quantum well (MQW) active region, and the lower

waveguide is passive. The growth sequence is as follows. First, a 1 μm buffer layer of n-InP is grown, followed by a 430 nm thick, lightly doped (2×10^{17} cm^{-3}) InGaAsP layer with E_g=1.0 eV, which forms the large-bandgap passive waveguide. Next, a 600 nm thick InP:Si (n=5×10^{17} cm^{-3}) spacer layer is grown. For devices with an absorption layer, the spacer contains a 100 Å thick In$_{0.53}$Ga$_{0.47}$As ($E_g \approx$ 0.75 eV) layer centered between two 300 nm InP layers. The second, upper waveguide consists of a MQW active region surrounded by confinement layers. The active region has three, 13 nm thick InGaAsP QWs (bandgap $E_g \approx$0.77 eV, with 1% compressive strain to InP) separated by 20 nm InGaAsP barriers with a bandgap of 1.0 eV. InGaAsP with E_g=1.0 eV was also used for the two 113 nm separate confinement layers. On top of the active guide, a 110 nm thick layer of Be-doped InP is grown, followed by a 51 nm thick InGaAsP (E_g = 1.0 eV) etch stop layer. Finally a ~1 μm thick layer of heavily p-type InP:Be (p=5×10^{17} to 5×10^{18} cm^{-3}) is grown, followed by a 70 nm InGaAs:Be cap which serves as the p-contact layer.

The structure was designed such that the two optical eigenmodes (even and odd) have equal propagation constants and optical confinement factors in the QW region. This ensures that in the absence of the loss layer, both modes have equal gain and propagate at the same velocity, and the exchange of power between the guides can be nearly complete [4]. The calculated mode intensity and index profile for this twin-guide structure is shown in Figure 1. At the center of the InP spacer layer separating the two guides, the field intensity of the odd mode is zero while that of the even mode is comparable to the intensity in the guide layers. For a 100 Å thick InGaAs loss layer centered at this point, the confinement factors of the even and odd modes in this layer are calculated to be 0.3% and 4×10^{-4} %, respectively. Assuming an absorption of 10^4 cm^{-1} in In$_{0.53}$Ga$_{0.47}$As at a wavelength of 1.5 μm [6], the additional loss due to this layer for the even and odd modes is 30 cm^{-1} and 0.04 cm^{-1}, respectively. Since both modes have approximately the same confinement factor (4.06%, 4.08%) in the QW region, the odd mode will reach the lasing

condition well before the even mode, and hence will dominate. With the above-mentioned symmetric design criterion, the intensity of light in both guides is nearly the same for the remaining odd mode. Thus we can achieve an output coupling coefficient at the etched facet of ≈50%, while maintaining a reasonably low threshold current density. Since only the odd mode effectively propagates in the structure, periodic light coupling between the waveguides is removed, and the etched facet feedback is independent of the device length.
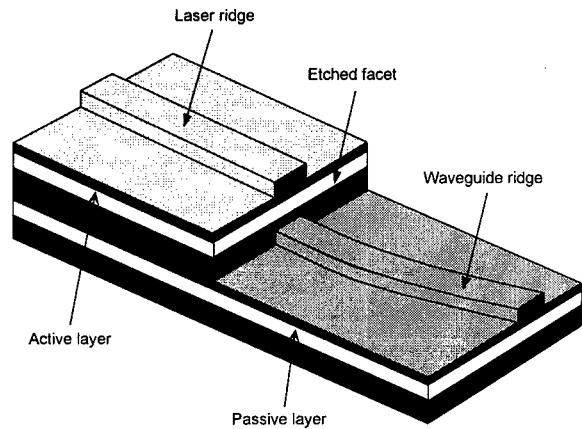
Figure 2: Schematic view of the integrated twin-guide device. The active layer has 3 quantum wells.
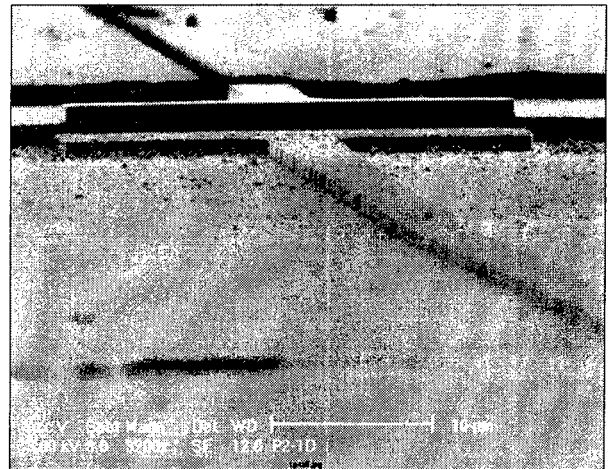
Figure 3. A scanning electron micrograph of the vertical dry-etched laser facet.

We fabricated several integrated laser/waveguide devices using the twin-guide structure, with one cleaved facet and the second facet formed by dry etching. The device fabrication

670

procedure is as follows. First, the laser region is protected by a ~300 nm thick SiN$_x$ mask, and RIE with 1:7 CH$_4$:H$_2$ mixture is used to form the laser facet [7]. The facet etch is stopped midway between the two waveguides. A scanning electron micrograph in Fig. 3 shows a vertical, smooth dry-etched laser facet. Next, the surface is protected with a second SiN$_x$ layer, used to define the ridge. This mask has a T-shape, seen in the SEM image, to protect the laser facet during ridge etching. Both wet (5 Citric acid: 1 H$_2$O$_2$ for InGaAs and 3 HCl:1 H$_2$SO$_4$ for InP) and dry (CH$_4$:H$_2$ plasma) etching are used to simultaneously form the laser and passive waveguide ridges. The passive waveguides (either single or Y-branch) are angled at 7° from normal to the cleaved facet in reduce reflections back into the laser cavity. The p-contact is E-beam deposited Ti/Pt/Au (200Å/ 500Å/ 2000Å). The wafer is thinned to ~100 μm, and a Ge/Au/Ni/Au (270Å/ 450Å/ 215Å/ 1000Å) n-contact is deposited on the substrate and annealed at 362 °C for 90 seconds. Finally, devices with different active region lengths are formed by cleaving from the side opposite the etched facet. Several double-cleaved (without an etched facet) devices were also made to study the threshold current density of the TG structure.
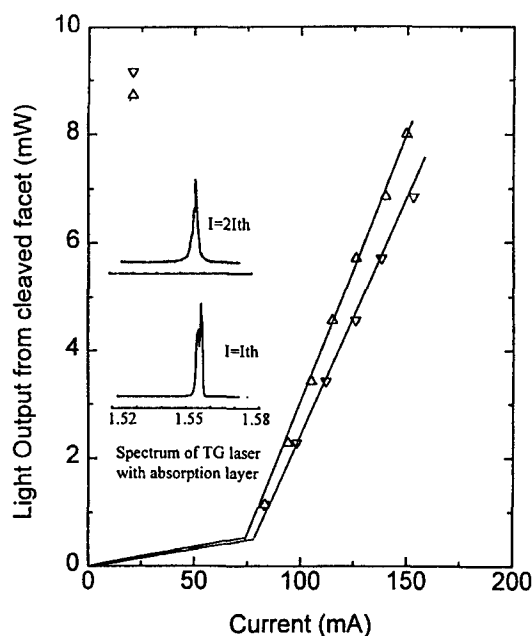
Figure 4. Typical L-I curves and spectra of double-cleaved TG lasers

Results

Figure 4 shows typical light-current characteristics of double-cleaved (without an etched facet) TG lasers. A detailed study of threshold current density and efficiency versus length has shown that the absorption layer does not appreciably degrade laser performance [8]
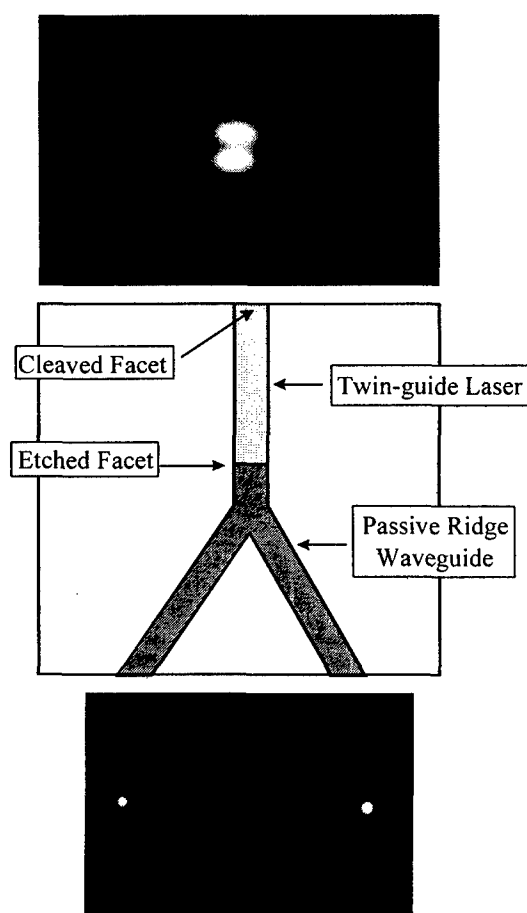
Figure 5. Near-field intensity for the integrated laser/waveguide device with loss layer.

The near field pattern from the cleaved facet of an integrated TG device (fig. 5) shows that the light intensities from the upper and lower waveguides are approximately equal. As much as 45% of the light is coupled from the laser into the passive waveguide (Fig. 5). This represents a significant increase in TG coupling as compared with previously reported values of ≤13% [3] for a TG laser integrated with Y-branch waveguide, and is close to the theoretical maximum of 50%.

671
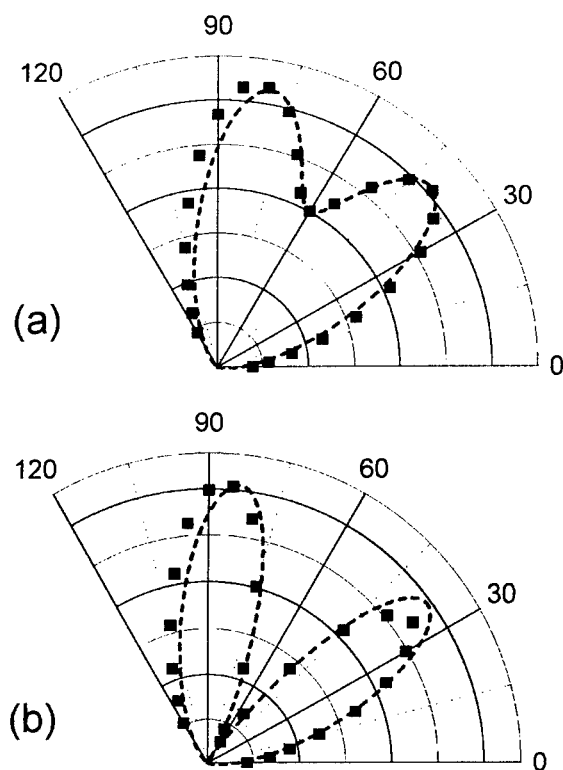
Figure 6. Calculated (lines) and measured far-field intensity profiles for integrated devices: (a) without loss layer, (b) with 100Å InGaAs loss layer.

The transverse far field intensity patterns from the cleaved facet for TG lasers with and without the loss layer are shown in Fig. 6. They clearly show that without the loss layer lasing occurs on both modes, while the device with the loss layer preserves only the odd mode.

Conclusion

We have demonstrated an InP/InGaAsP MQW laser monolithically integrated with a passive waveguide using a modified Twin-Guide structure. This device is free of limitations inherent in the conventional TG structure, and represents an important step on the way to achieving fully monolithic photonic integrated circuits.

Acknowledgments

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1.55μm InGaAsP/InP PHASE-LOCKED DIODE LASER ARRAYS OF HIGH COHERENT POWER

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Introduction

We have obtained 2.5W peak-pulsed power in a 2.6° wide beam (6.4×diffraction-limit), with 1.2W in the central lobe, from 40-element, 250μm aperture, 1.55μm antiguided laser arrays. The InP-based devices have a compressively-strained InGaAsP double-quantum-well active region and are fabricated by creating a near-resonant antiguided array via a two-step self-aligned MOCVD growth. The width of the central lobe remains constant from 4 to 15×threshold.

I. Background

High-power, narrow-beam diode lasers emitting at 1.5μm wavelength and beyond are particularly attractive as eye-safe sources in areas such as free-space communication, range-finding and marking. Monolithic, leaky-wave-coupled arrays of diode lasers, have demonstrated high brightness output with reliable operation at high power from GaAs-based devices at λ=0.85 and 0.98 μm[1]. There has been however very limited research into InP-based high-power coherent arrays at longer wavelengths: Dong et al. [2] demonstrated 60mW peak-pulsed power in a beam 2.5-3×diffraction-limit (D.L) from an 18μm aperture, 5-element, evanescent-wave-coupled array using a DFB grating for spatial-mode selectivity. To obtain diffraction-limited operation, a complex grating-filter-array structure involving 4 MOVPE growths was needed[2], and the D.L. power was still limited to only about 100mW.

Antiguided arrays have exhibited superior performance characteristics compared to coupled positive-index waveguide laser arrays. Being strongly index-guided and hence insensitive to carrier- or thermally-induced index variations, they are ideally suited for high-power operation. Laughton et al. [3] achieved phase-locked operation to 2.25×threshold from a 75μm aperture, 5-element, 1.48μm antiguided array structure in a beam 4.6×D.L, but the peak power was only 25mW.

"Long-wavelength" laser diodes have typically depended on strained $In_xGa_{1-x}As$ quantum-well active regions, which require different well thicknesses for different strain to obtain a particular wavelength. The use of $In_xGa_{1-x}As_yP_{1-y}$ for compressively strained quantum wells allows for a much wider scope for laser structure

design[4]. In particular, the possibility of independent variation of well width and strain for a given emission wavelength has led to the recent development of low-threshold current density material with high differential quantum efficiencies[5], leading to record CW output power[6]. We present here preliminary results from antiguided, near-resonant 1.55μm-wavelength diode laser arrays using a compressively strained $In_xGa_{1-x}As_yP_{1-y}$ quantum-well structure.

II. Experimental

A schematic lateral cross-section of the array structure is shown in Fig. 1. The material is grown by low pressure (20mbar) MOCVD at a substrate temperature of 655°C on exact-oriented (100) n:InP substrates in an Aixtron A-200 reactor. No special substrate cleaning procedure is used prior to growth. Trimethylgallium and trimethylindium are used for the group III sources, while arsine and phosphine supply the group V elements.
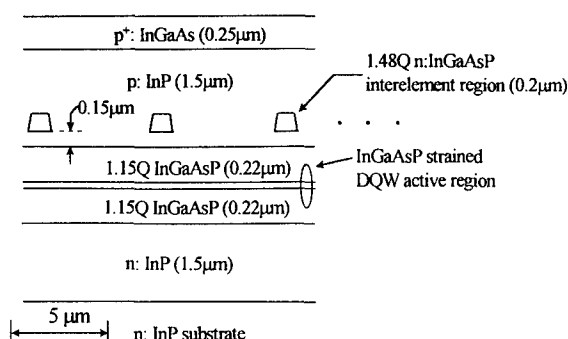
Fig. 1. Lateral cross-section of 1.55μm-emitting 40-element antiguided array
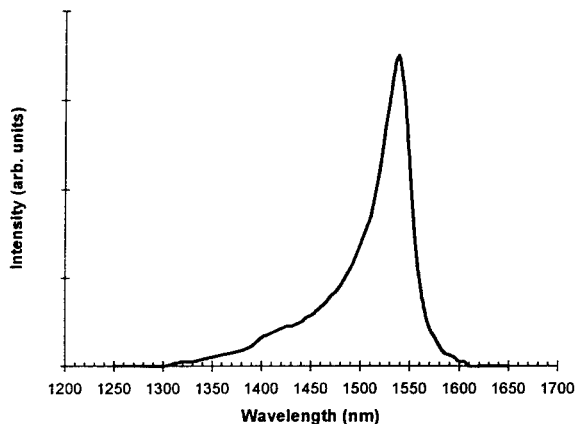
Fig. 2. Room-temperature photoluminescence spectrum from a double quantum-well structure with 1.15Q InGaAsP barriers and 1% compressively strained InGaAsP wells.

Diluted silane and diethylzinc are used for the n- and p-type dopants respectively. The active region has two compressively strained (~1%) 115Å-wide InGaAsP quantum wells, in a 0.45μm-wide, lattice-matched, 1.15Q InGaAsP optical-confinement layer. Room-temperature photoluminescence from such a double quantum-well structure is shown in Fig. 2. The half-width of the PL spectrum is 22meV. To further test the material quality, 100μm stripe "broad-area" lasers with such an active-region structure were fabricated and tested. The devices have threshold-current densities, J_{th}, as low as 185A/cm^2 for 2mm-long, and 235A/cm^2 for 1mm-long devices at room-temperature. Differential quantum efficiencies, η_d, are 48% for the 2mm and 61% for the 1mm-long devices respectively.

The array is made up of 40 elements, each 5μm wide, separated by 1.25μm-wide interelement regions, thus forming a 250μm aperture. The effective-index difference between interelement and element regions, Δn_{eff}, is ~0.07, corresponding to near-resonant operation on the high-Δn side of resonance[7,8] of a leaky-wave coupled resonant optical waveguide (ROW) array. This permits the oscillation not only of the resonant in-phase mode of the array but also of a few adjacent modes, which improves efficiency while also easing fabrication tolerances at the same time. An intracavity Talbot filter[8] is used to suppress the oscillation of out-of-phase modes.

The devices are fabricated by a two stage self-aligned etch-and-regrow process. The n:InP cladding layer, SCH active-region, p:InP etch-stop layer and a 1.48Q n:InGaAsP layer are grown in the first step. In addition a 50nm p:InP capping layer is grown on top of the InGaAsP guide layer which serves both as a hard mask for later processing and also for ease of surface

passivation during heatup for the regrowth. The array pattern is then etched in the 1.48Q n:InGaAsP layer, which defines the high-index interelement regions after the MOCVD regrowth of the p-InP cladding and p$^+$-InGaAs contact layers. Since the n:InGaAsP guide layer also serves to restrict current flow to the element regions only, no further isolation is required for current confinement and metallization on the p- and n-sides completes the fabrication sequence.

III. Results and Discussion

1mm-long devices, LR/HR (3%/95%) coated, mounted junction-down on copper heatsinks were tested under pulsed conditions (5μs pulse width, 300Hz repetition rate) at 15°C. Typical threshold currents for the devices are around 1.5 A with a slope efficiency of ~0.15W/A. Beam pattern measurements were made with the chips mounted on a stepper-motor controlled rotation-stage and a Ge-detector in the far-field. Fig. 3 shows the far-field pattern for a device at an output power of 1W; the full width at half maximum (FWHM) of the central lobe is 1.8° corresponding to a beam 4.4×diffraction-limit. Fig. 4 shows the light-current curve for a device whose far-field patterns, at different drive levels, are shown in Fig. 5. Near threshold, I_{th}, the beamwidth is 3.6×D.L.. The beamwidth increases to 6.4×D.L. at 3.8I_{th}, and remains the same up to 15.5×I_{th}, corresponding to an output power of 2.54W of which 1.2W resides in the central lobe. The beam stability indicates that the available gain across the array is utilized completely by the in-phase and the few adjacent array modes lasing, thus not allowing other modes to reach threshold.

In conclusion, we present the first demonstration of 1.55 μm emitting high-power antiguided laser arrays.

$I = 8.7A = 5.8I_{th}$
$P = 1W$
$\theta_{1/2} = 1.8° = 4.4xD.L$
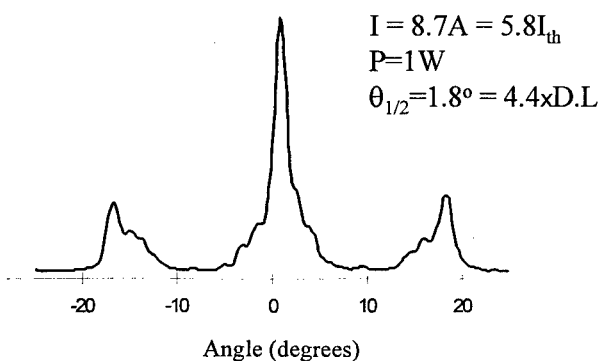
Fig. 3. Farfield patterns of a 1.55μm-emitting diode laser array. I_{th} denotes threshold current and D.L. denotes diffraction limit

674

Near-resonant operation provides 1W in a beam 4.4×D.L., and up to 2.5W in a beam 6.4×D.L., with 1.2W power in the central lobe.
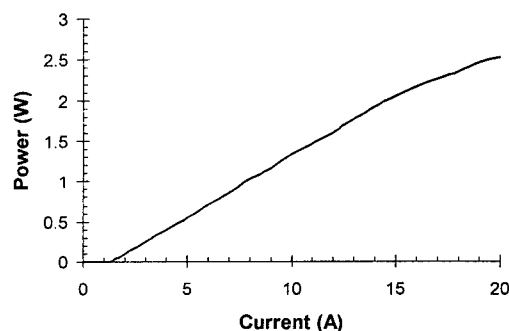
Fig. 4. Light-current curve of a 1.55μm-emitting diode laser array at 15°C. The threshold current is 1.3A. The farfield patterns for this device are shown in Fig. 5
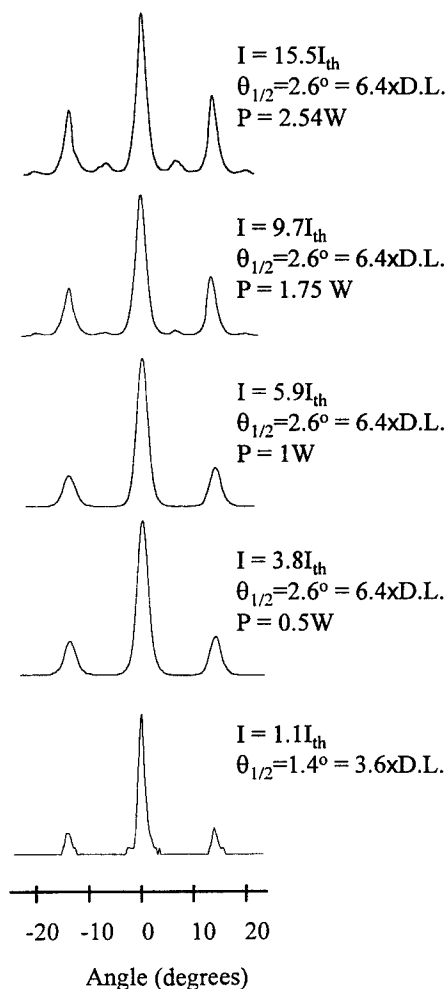
Fig. 5. Farfield patterns of the 1.55μm-emitting diode laser array at different drive levels . I_{th}, the threshold current is 1.3A. D.L. denotes diffraction limit

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676

AUTHOR INDEX